



# Evaluating Three Key Pieces of a SiC Total System Solution

Following a rapid expansion of SiC product options, the industry's next challenge is simplifying the design-in process for end users. Power system developers need holistic solutions that address not only typical design elements individually but which recognize the importance of their interactions.

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**SiC suppliers must not only demonstrate the performance and ruggedness of their SiC MOSFET technology, but must assist with design-in challenges by offering low-inductance power packaging and more sophisticated gate drivers to support, protect, and fine-tune system parameters. Careful consideration of these three key pieces is certain to simplify evaluation and design for those looking to capitalize on the disruptive system-level improvements made possible with SiC.**

#### **Robust and rugged SiC MOSFET**

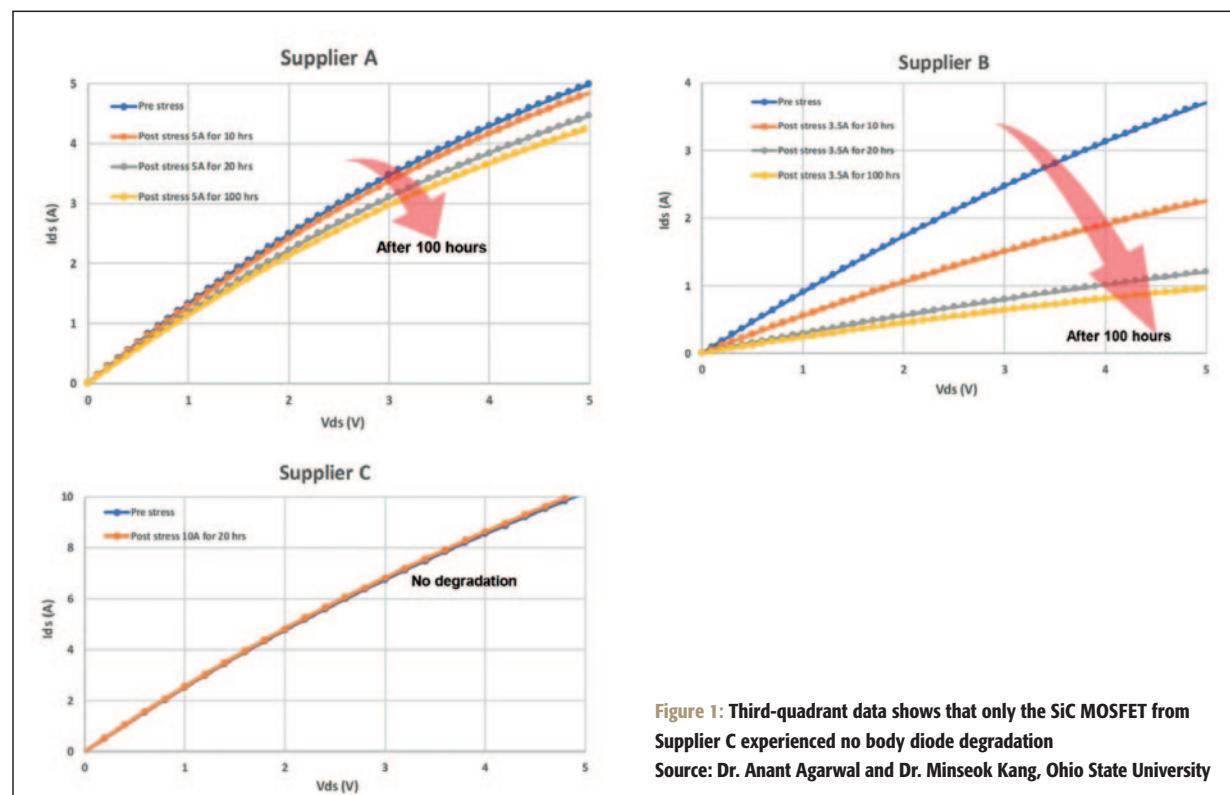
Arguably the most critical link in the power system chain, SiC MOSFETs must demonstrate robustness in several keys

areas where they have traditionally been vulnerable. Like silicon MOSFETs, they too have been challenged with the problem of extrinsic defects such as impurities, charge states and other material defects near the oxide-semiconductor interface, which precipitate a variety of device instabilities and degradation mechanisms. Eliminating these risks requires that production-grade SiC MOSFETs demonstrate a stable threshold voltage, a reliable gate oxide, a robust intrinsic body diode, and ruggedness under avalanche conditions. Each attribute must be validated through qualification testing as parametric stability and lifetime can vary dramatically from one supplier to another.

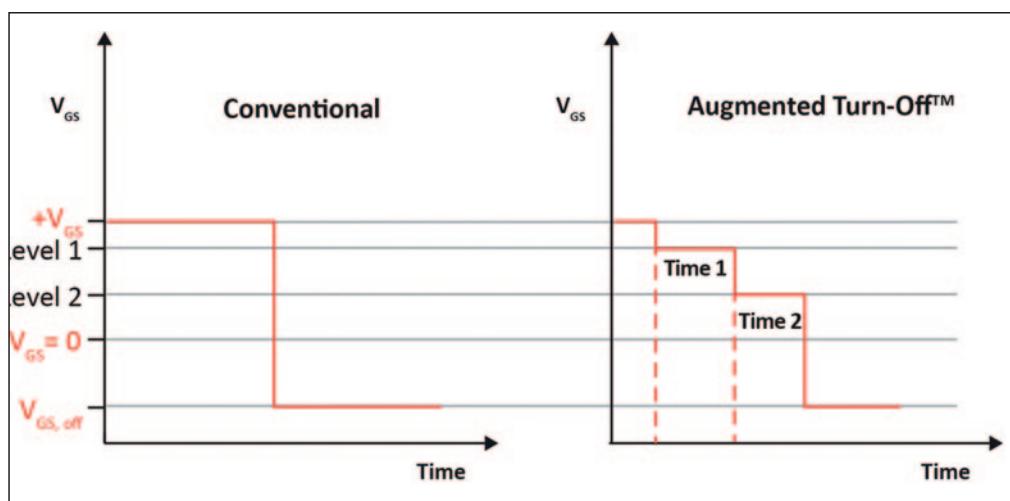
To test the threshold voltage ( $V_{th}$ ) stability

of a SiC MOSFET, it is common practice to apply positive (p-HTGB) and negative (n-HTGB) high-temperature gate bias stresses to a statistically significant number of devices and simply compare the pre- and post-stress  $V_{th}$  of the population. As an example, p- and n-HTGB have been performed on independent sets of sixty-four 1200 V SiC MOSFETs for 1,000 hours. The average change observed in  $V_{th}$  was +59.6 mV following p-HTGB and -22.8 mV following n-HTGB. At this stability level, developers have a predictable threshold voltage around which they can make tighter, longer-term design choices.

High-reliability gate oxides are critical for all applications, especially those requiring long service lifetimes. To determine the



**Figure 1:** Third-quadrant data shows that only the SiC MOSFET from Supplier C experienced no body diode degradation  
Source: Dr. Anant Agarwal and Dr. Minseok Kang, Ohio State University



**Figure 2:** Digital gate drivers that use an augmented switching approach make a simple, straightforward task of identifying the optimal design points and quantifying their value to stakeholders

reliability of the subject SiC MOSFET's gate oxide, charge-to-breakdown ( $Q_{BD}$ ) measurements were made on three populations of 1200 V SiC MOSFETs. All observed failures were intrinsic, indicating a high level of process maturity. Failure-in-Time (FIT) and Mean Time to Failure (MTTF) rates were calculated using a broader population of 192 devices. For p-HTGB, these values were found to be 20 and 5,618 years; for n-HTGB, the FIT was 93 with an MTTF of 1,233 years. End users should find encouragement that these results are consistent with time-dependent dielectric breakdown (TDDB) reports from multiple vendors.

The phenomenon of bipolar degradation in SiC p-n junctions has been heavily studied. Should this occur in the body diode of a SiC MOSFET, increases will be seen in both on-state resistance and the voltage drop across the diode during current commutation (revealed by a detrimental drift in third-quadrant output characteristics). Thankfully SiC MOSFET materials have matured, and the density of preexisting crystal defects has decreased in production-grade materials. Even so, each vendor's SiC MOSFETs must be evaluated. Ohio State University recently contrasted body diode degradation following 100 hours of stress at full-rated current ( $V_{GS} = -5$  V) in 1200 V SiC MOSFETs from multiple vendors, revealing substantial disparities in post-stress on-state resistance. Only Supplier C showed no degradation (Figure 1). Complementary third-quadrant data on the same devices corroborated the presence (or absence, for Supplier C) of body diode degradation.

Another important parameter to assess is avalanche ruggedness, which is done with unclamped inductive switching (UIS). The MOSFET is fed a power surge while in its OFF state, which forces all current to avalanche in the die's periphery since the MOS channel is not enhanced. This differs from a short-circuit withstand test, in which

the MOSFET is in an ON state and the current more uniformly distributes across the device's entire active area. To closely emulate real-life field conditions, SiC MOSFETs are subjected to repetitive UIS (R-UIS) pulses; parametric stability and oxide integrity are compared before and after 100,000 repetitive pulses at two-thirds rated current (per MIL-STD-750).  $V_{BR}$ ,  $V_{th}$  and the body diode's  $V_f$  are unaffected by R-UIS, indicating excellent avalanche ruggedness.

**Low-inductance power packaging**  
With confidence established in the SiC MOSFET, the next instrumental piece of a SiC total system solution is an optimized power package. An effective multi-chip module package should enable designers to leverage SiC's advantages rather than inhibit them.

There are numerous requirements to consider. Because the SiC MOSFET die is comparatively small, many of them must be paralleled to achieve a low on-state resistance. As well, the paralleled MOSFET die must switch with the same timing and uniform current sharing, which means ensuring both symmetry and low inductance through die interconnection schemes.

An example is Microchip's SP6LI package that inserts only 2.9 nH of stray inductance into the power loop, compared to 20+ nH of parasitic inductance in standard module packages. Power loop inductance is reduced by arranging DC link connections in strip line-configured bus bars. Substrate connections are symmetrically distributed and as close as possible to the semiconductor die. With respect to the gate-source loop, independent series gate resistor slots are used for each of the twelve available die spaces in the high- and low-side switch positions to optimize timing and current sharing. The independent gate resistors reduce parasitic inductance inserted into the gate-source loop, protecting against

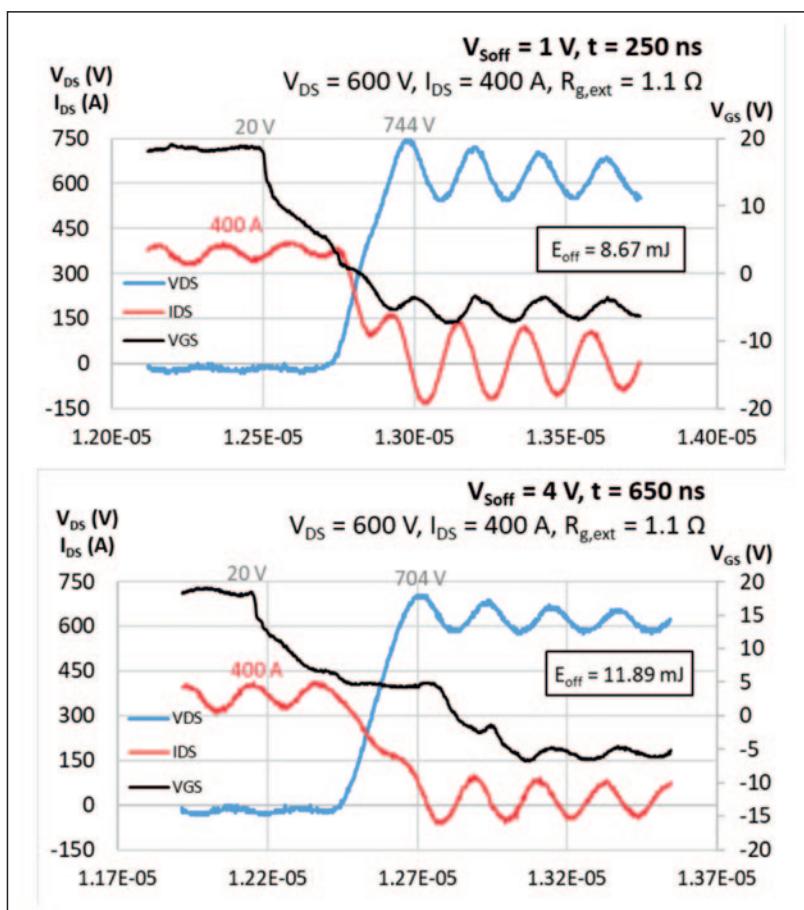
catastrophic shoot-through events while minimizing switching losses.

#### Flexible gate driver technology

A third critical piece required for a total SiC system solution is control. Once again, the fast switching capability of SiC MOSFETs puts a non-optimized system at risk of EMI failure and transient voltage spikes. A new class of gate driver technology is required that allows the designer to manipulate switching dynamics and arrive at optimal tradeoffs. Furthermore, the gate driver must provide rapid detection and response to surge conditions, since SiC MOSFETs have shorter withstand times compared to most Silicon IGBTs.

Using a patented technique called augmented switching (AS), the latest digital gate driver solutions make it possible to pause at a user-specified, intermediate  $V_{GS}$  for the desired duration to discharge the Miller capacitance before proceeding to the off-stage  $V_{GS}$  (see Figure 2). This contrasts with traditional approaches that take  $V_{GS}$  directly from the on-state level to the off-state level, offering the designer no escape route from the system's other, less avoidable pitfalls such as the parasitic inductance of the cable used to connect the load. Indeed, dramatic tradeoffs between voltage overshoot and efficiency may be realized with slight modifications in the Augmented Switching profile ( $V_{GS}$  levels and dwell time).

Figure 3 shows turn-off waveforms using two augmented switching profiles and a 1200 V SiC MOSFET module in a D3 (106 mm x 62 mm x 31 mm) package. One can observe that selecting a lower intermediate  $V_{GS}$  reduces switching losses where efficiency is a priority, while the use of a higher  $V_{GS}$  dampens  $V_{DS}$  overshoot and softens the oscillations of all three waveforms. Using the supplied software configuration tool, the gate driver's settings can be fine-tuned at all stages along the development path with the click of a



mouse, as opposed to hours spent holding a soldering iron.

Digital gate drivers can also offer enhanced intelligence. For example, they can be used to trigger an entirely different turn-off profile in the case of a fault event to better ensure a safe ride-through. Incorporating AS methods into short circuit protection reinforces the use of a low  $R_s$ , as well as guiding the MOSFET through a softer, more controlled transition to the off state with reduced likelihood of avalanche. Still more configurable features include real-time diagnostic measures, such as DC link voltage and temperature monitoring.

As power electronics designers transition from silicon IGBTs to SiC MOSFETs they increasingly rely on component suppliers to provide the critical elements they need to create total system solutions. This includes a SiC MOSFET with proven ruggedness, an ultra-low inductance power package, and a new class of intelligent gate drivers built for ease of optimization. Each is a prerequisite for streamlining the SiC design journey from initial evaluation through field deployment.

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