# A high efficiency, 3 kW capable, 2-phase, 3-level Converter using paralleled eGaN<sup>®</sup> FETs

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# As the revolution of renewable energy as well as transportation electrification progresses, the need for residential energy storage systems is increasing. A high efficiency DC-to-DC converter is usually required to exchange energy generated from renewable sources, such as solar panels, with a battery. The fast-switching speed and low RDS(ON) of gallium nitride (GaN) FETs can help save energy by reducing power consumption inside the DC-to-DC converter[1]. This article shows how to design a high efficiency 100 -250 V to 40 - 60 V DC-to-DC converter taking advantage of the low RDS(on) of the EPC2215. A 3-level flying capacitor topology offering a 2x reduction of voltage and current stresses, which improves

overall efficiency, is employed. Advantages of a 3-level Buck or Boost Converter

The 3-level flying capacitor buck or boost converter is an attractive topology as it allows for a 2x reduction in FET voltage stress and volt-seconds stress on the inductor, as well as 4x inductance reduction compared to a conventional twolevel converter with the same current ripple [2]. Figure 1 shows the operation of the 3-level converter operating in buck mode. One top switch and one bottom switch forms two complementary switch pairs  $Q_1/Q_4$  and  $Q_2/Q_3$ . Top switch  $Q_1$  and  $Q_2$  operate at the same duty cycle but have a 180° phase shift between them, while the bottom switch  $Q_3$  and  $Q_4$  operate at a complementary duty cycle.

The conventional current mode control can still be applied for this converter, as shown in figure 2. In such configuration, the output voltage loop generates the reference for the inner current loop. To ensure the switches have even voltage stress (0.5·V<sup>m</sup>) when the switch is off, an additional flying capacitor voltage loop is added to actively regulate the flying capacitor voltage, this can be achieved by adjusting the charging and discharging period of the flying capacitor [3].

# **Design Validation**

A 3 kW capable experimental 2-phase (1.5 kW per phase) 100 V – 250 V input and 40 V - 60 V output 3-level DC-to-DC



Figure 2: Block diagram of output voltage and flying capacitor voltage balancing control loop.

converter, ideal for battery charger applications in energy storage systems, was built and tested as shown in figure 3. It can supply up to 60 A into a 48 V load. The experimental unit comprises two interleaved phases and each phase employs a 3-level flying cacpacitor converter topology designed using two EPC2215 FETs [4] connected in parallel for each switch position and operated at 150 kHz switching frequency.

Each phase employs three half-bridge



Figure. 3: The experimental unit image with identification of that various function circuits.



Figure. 4: A zoomed in layout of the power stage area showing switches (Q1-Q4 located on the bottom side of the PCB), gate drivers (GD1-3) and capacitor placement.

gate drivers using NCP51820 [5]. The lower FET are driven by a signle gate driver for Q<sub>3</sub> and Q<sub>4</sub>. To drive the upper series of Q<sub>2</sub> and Q<sub>1</sub>, two additional high-side gate driver outputs are used. The gate drivers are powered by a cascaded bootstrap circuit. A zoomed-in layout of the switch and capacitor placement is shown in figure 4, where the FETs are located on the bottom side of the baord. Low ESL ceramic capacitors are placed between switch pair Q<sub>1</sub>/Q<sub>4</sub> and Q<sub>2</sub>/Q<sub>3</sub> which act as high frequency decoupling paths to reduce the parasitic inductances associated with the switch positions.

The experimental unit is digitally controlled using a dSPIC33CK controller on EPC9528. The experimental unit is tested with the input on the high voltage port and output voltage regulated down to 40 V. In this mode, the controller is comprised of one single output voltage loop, two current loops and two flying capacitor balancing loops as shown in figure 2. The two current loops share the same current reference generated by the output voltage side to ensure active current balancing. The two phases are interleaved (180° phase shift) to achieve ripple cancelation on the capacitors.

A measured waveform is shown in figure 5 which shows the switch node of one phase at 24 A output with  $V_{OUT} = 40$  V and  $V_{IN} = 200$  V. Measured, efficiency and power loss at  $V_{OUT} = 40$  V and  $V_{IN} = 200$  V are given in figure 6. In single phase configuration, the converter achieves 97.8% peak efficiency around 14 A output.

The experimental board is equipped with an aluminum heat-spreader and heatsink which can be attached to the back side of the PCB where the FETs are located. The heat-spreader is mounted to the PCB using SMD threaded spacers which are 1 mm tall and use 6 mm long M2 countersunk screws for a flat mounting surface and follow best practice [6]. High performance thermal interface material (TIM) from T-Global (part TG-A1780) is used between the FETs and heat spreader for improved heat conductance. A heatsink

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Figure. 5: Typical switch node waveforms showing several switching cycles when the board is operating from 200 V input and delivering 24 A into a 40 V load.



Figure. 6: Measured efficiency (left axis) and power losses (right axis) with  $V_{out} = 40 V$  and  $V_{in} = 200 V$ 



Figure.7: Thermal image taken from the top side of the PCB when operating from 200V input and delivering 24 A into 40 V load in an ambient of 20°C

is attached to the flat mounting face of the heat-spreader. A two-part gap filler TIM (Bergquist GF4000) is used for the thinnest bond line thickness, and to provide some adhesion between the heatsink and heat-spreader. With this cooling method, figure 7 shows temperature measurements taken from the top side of the PCB with IR camera and only a 30°C temperature rise is recorded. The air flow used is around 1500 - 2000 LFM.

### Conclusion

This article presented the design of a 3 kW capable 2-phase (1.5 kW single phase) DC-to-DC converter reference design using eGaN FETs, EPC2215. A 3-level topology is used which allows for 2x reduction in voltage stresses in the switches. In the experiment, 97.8% peak efficiency is achieved at 200 V input and 40 V output. The temperature rise of the FET is around 30°Cwith top side cooling using a heat-spreader and heatsink.

## References

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