POWER ELECTRONICS EUROPE

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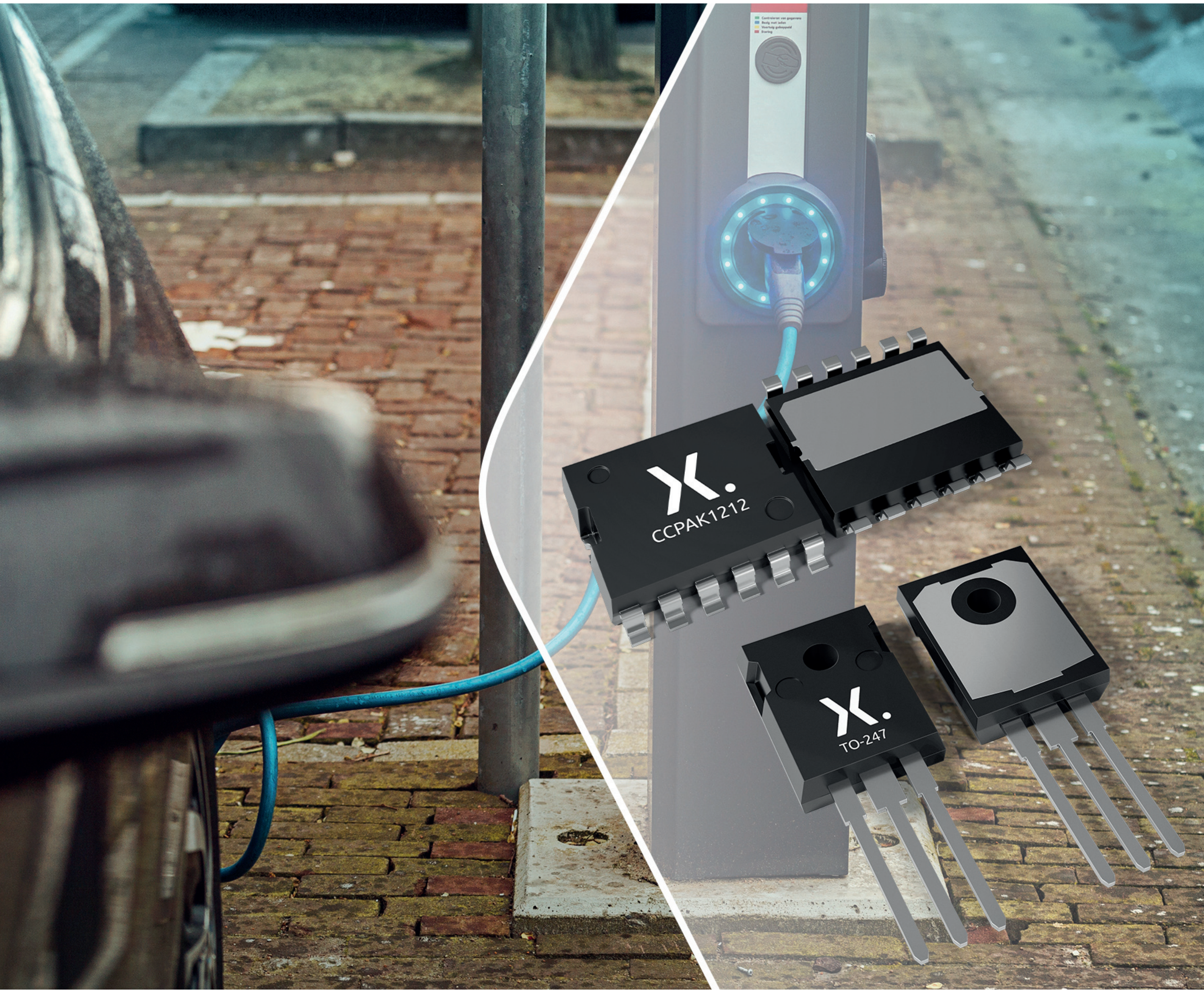
POWER GaN

Proving the Ruggedness of GaN technology in Automotive and Demanding Applications



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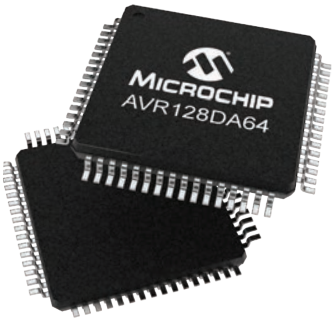

Functional Safety Ready

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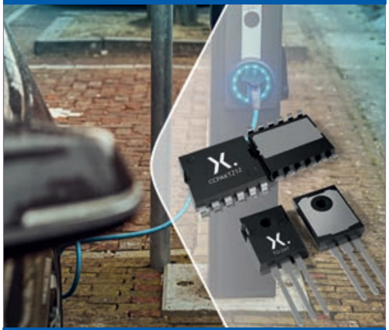
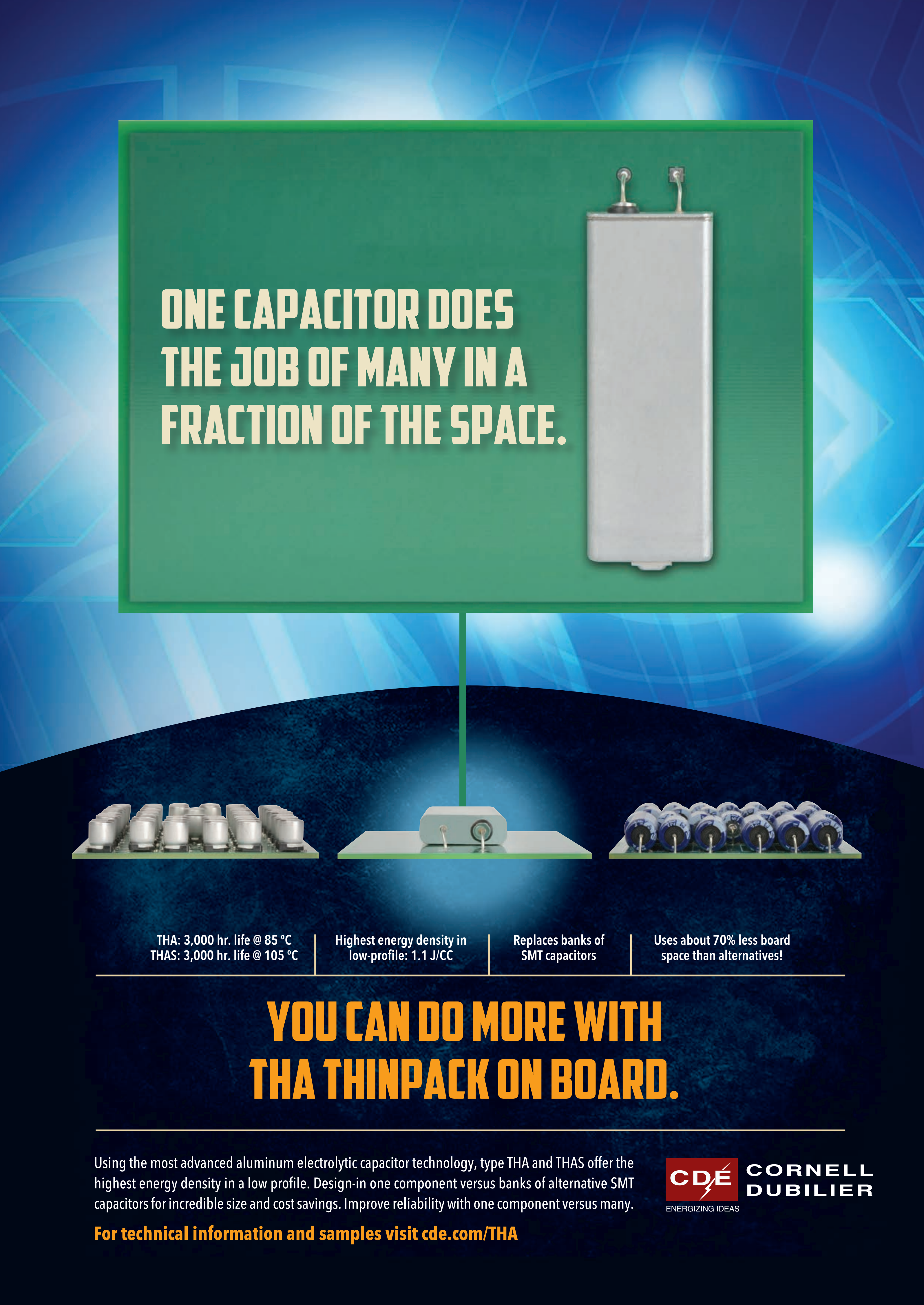
FEATURE STORY



Proving the Ruggedness of GaN technology in Automotive and Demanding Applications

To achieve the most efficient power conversion circuit requires the best semiconductor switch as the fundamental building block. Many people now consider gallium nitride to be a better switch than silicon. This is because GaN transistors feature a very low on-resistance and very high switching speeds; they are also rugged as they do not suffer avalanche breakdown of traditional MOSFETs. GaN is commonly used in RF and LED applications, yet employing GaN as a power technology brings new challenges. This article discusses product robustness, quality and reliability issues at high voltage and high temperatures, for Nexperia's latest 650 V power GaN FET technology which is now qualified in accordance with AEC-Q101 automotive standard. GaN is the preferred switch for these applications as GaN FETs lead to systems with greater efficiencies at lower costs with improved thermal performance and simpler switching topologies. In automotive terms this means that the vehicle has a greater range – the major concern for anyone looking to buy an electric vehicle. GaN is now on the brink of replacing Silicon based IGBTs as the preferred technology for the traction inverters used in plug-in hybrids or full battery electric cars. More details on page 17.

Cover image supplied by Nexperia, Netherlands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The GaN Journey Continues Accelerated

Addressing the wide range of power electronic applications - from mW power needed for the operation of mobile phones up to the GW power for high-speed trains - all looking into power electronic potential for energy efficiency and sustainable reduction of carbon dioxide emission in future power conversion systems. Besides the Si-based devices like IGBT, Super Junction MOSFET SiC and GaN transistors are coming up. But there are several reasons for the argument that Si-based devices still have substantial further development potential, the electrical and thermal performance is outstanding; the reliability is proven because of many years in application, and the cost is low. WBG devices are still at the beginning of their production cycle, the learning in material development and device design is ongoing, the benefits on the system level needs to be qualified, long-term reliability issues needs to be proven and cost down programs will come along with high volume production, expects Leo Lorenz, ECPE President and General Chair of PCIM. The long-term roadmap development driven by ECPE will demonstrate and prepare the movement from Si- devices to WBG technologies, as well as conferences such as PCIM and magazines such as Power Electronics Europe (PEE) have already done for decades.

The 'PCIM Europe digital days 2020' premiered from 7 – 8 July 2020 featuring a virtual lecture program with more than 300 conference and forum presentations with 4,506 participants, according to the organizer.

At PCIM 2020 Digital Days PEE have hosted a virtual panel discussion on 'Power GaN: Past – Present – Future' – ten years after the first power GaN devices have been introduced to the market. This panel discussion attracted 379 PCIM attendees – illustrating the high interest in GaN and the highly qualified panelists from leading GaN vendors such as EPC's CEO Alex Lidow, Infineon's Senior GaN Director Tim McDonald, GaNSystem's CEO Jim Witham, Navitas' VP Corporate Marketing Stephen Oliver, Power Integrations' CEO Balu Balakrishnan, and Transphorm's COO Primit Parikh. According to a timeline of market researcher Yole Developpement the GaN journey started 10 years ago in 2010 with International Rectifier's 600 V cascoded - or depletion mode platform (normally off by cascoded Silicon MOSFET), followed soon after by EPC's lower voltage enhancement-mode (normally-off). Later in 2012 Transphorm released its first d-mode 600 V devices, followed by Panasonic's Gate Injection e-mode Technology in early 2013. Early in 2014 Transphorm used Fujitsu's manufacturing capability as foundry. Canadian GaN Systems entered the market in late 2014 with its novel Island e-mode Technology and switched early 2016 to TSMC's high-voltage GaN Process – as well as soon after Navitas and Dialog Semi with GaN power integrated circuits. In 2015 Infineon Technologies acquired International Rectifier – also due to its GaN portfolio - and soon after partnered with Panasonic to license their e-mode GaN technology – to gain a strong position in the evolving GaN market After Infineon's GaN transactions the market dynamics increased heavily. At APEC 2016 GaN Systems presented the winning inverter of Google's Little Box Challenge – a major milestone for this company since they have supplied the GaN power Transistors. In 2016 Navitas presented its first GaN power IC featuring an integrated drive leading to improved switching waveforms. The latest company joining the GaN community was in 2019 Power Integrations with its 650 V GaN-on-Sapphire approach, extended in 2020 to 750 V. The panelists agreed that existing and new applications will be covered by GaN as shown in our content over recent and coming issues.

And the Power GaN market ramps up according to market researchers – from $9 million in 2018 up to $350 million in 2024 with more and more applications covered – and from consumer/communications over automotive and industrial to space. The recently formed EPC Space will provide high-reliability power conversion solutions for critical spaceborne environments in applications including power supplies, light detection and ranging (lidar), motor drive, and ion thrusters. "This joint venture is taking the superior performance of gallium nitride to the high reliability community offering electrical and radiation performance beyond the capabilities of the aging Rad Hard Silicon MOSFETs," noted Alex Lidow at PEE's Panel Discussion. An other trend is the integration of power and logic on GaN chips such as the newly EPC2152 GaN ePowerStage. The main FETs are controlled by gate drivers within the IC that includes input buffers, a logic interface with Power-On-Reset, Under-Voltage-Lockout functions, a high voltage, high dv/dt capable control signal level-shifter and a synchronous bootstrap that ensures proper high-side voltage for the high-side gate driver. And this is only the beginning of GaN integration. We have to report more in the future.

Enjoy this issue!

Achim Scharf
PEE Editor

Diamond for Future (Power) Electronics

Diamond is an electric insulator with a thermal conductivity 5 times higher than copper – meaning it is the best heat conductor known to man. This makes diamond an ultimate candidate for high power and high temperature electronic applications. While natural diamond stones are too small to be used by the electronics industry, diamond can also be artificially synthesized under certain temperature-pressure conditions.

Claims for creating diamond in a lab date back to the 19th century. First trials involved transforming carbonaceous materials into diamond by recreating the conditions that lead to naturally occurring diamond. Diamond crystals form in limited zones of the Earth's mantle, at about 150 kilometres below the Earth's surface, where temperatures are at least 1500°C and pressure is correspondingly high, mainly under the stable interiors of continental plates.

Natural phenomena such as volcanoes and earthquakes bring these glittering natural marvels to the surface.

Natural vs. synthetic

In 1955, General Electric reported successful synthesis of diamond by replicating these extreme conditions in a high pressure high temperature (HPHT) reactor. In this process, a small natural diamond is bathed in molten graphite together with a metal catalyst at a temperature of 1500°C and pressure of 5 GPa. Carbon precipitates on the diamond seed and slowly crystallizes into a stone only a few mm^3 in volume. Billions of carats of synthetic diamonds are manufactured annually for commercial and industrial applications using this process.

HPHT diamond compares quite favourably with natural diamond. In fact, natural diamonds show a higher density of defects than HPHT diamond! With a thermal conductivity as high as natural diamond, single crystal diamond (SCD) has, at room temperature, the highest-known electron and hole mobility values, when compared to other wide band gap (WBG) materials. However, the area of most available HPHT substrates is limited to a few mm^2, an obvious limitation for electronics applications. Yet, niche applications continue to be served very well by this kind of diamond. 1-inch HPHT diamond substrates recently became available but they are still quite expensive.

In the early 1980s a Japanese group reported successful growth of diamond on various substrates from a mixture of methane diluted in hydrogen. The process was further optimized and chemical vapour deposition (CVD) has been used to grow diamond under highly reproducible conditions. CVD differs fundamentally from the HPHT growth process, since it involves the production of diamond from a gaseous precursor, typically methane. As methane molecules are heated by a high energy source, they form radicals whose carbon atoms bond with atoms at the substrate. This process also creates non-diamond bonds, like graphite. However, these are etched away by the activated hydrogen atoms, leaving behind high quality diamond. The gas phase activation can be done by electric discharge, hot filament (HF) or microwave energy. The deposition chamber is usually made of stainless steel stainless steel with double walls to allow for water cooling and is scalable. The material of the filaments used may vary (the most economic choice being tungsten). A filament temperature around 2500°C, and chamber pressure of 30 bar, in addition to appropriate pre-cursors, are the standard diamond deposition parameters.

Diamond films can be deposited by CVD on diamond (homo-epitaxial) as well as non-diamond (hetero-epitaxial) substrates, such as large-area Silicon wafers, thus overcoming the problem of small area HPHT substrates. However, hetero-epitaxial films are intrinsically polycrystalline, which may compromise carrier mobility, breakdown field, as well as thermal conductivity – which nevertheless remains as high as 1800 $Wcm^{-1}K^{-1}$. 4-inch polycrystalline diamond (PCD) wafers can be purchased from various vendors and they come as a cheaper alternative without necessarily compromising electronic performance.

Current challenges

Most of the challenges with respect to diamond technology lie in the availability of large area, quality wafers. Some specific grades of diamond wafers are commercially available, however, depending on their properties, most remain expensive. The required target properties of a diamond wafer are:

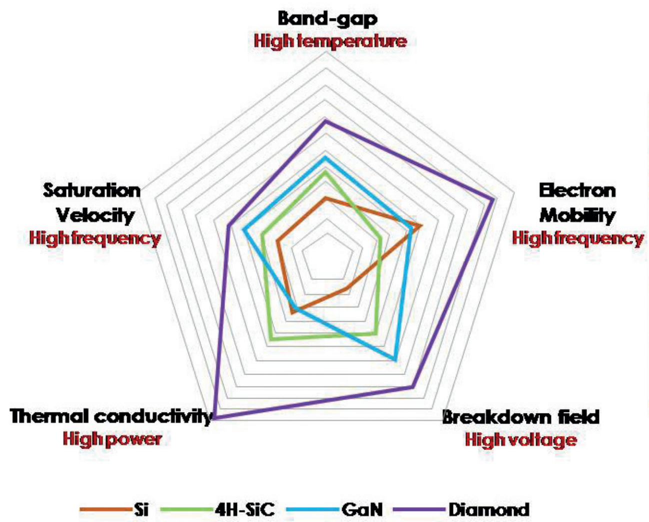
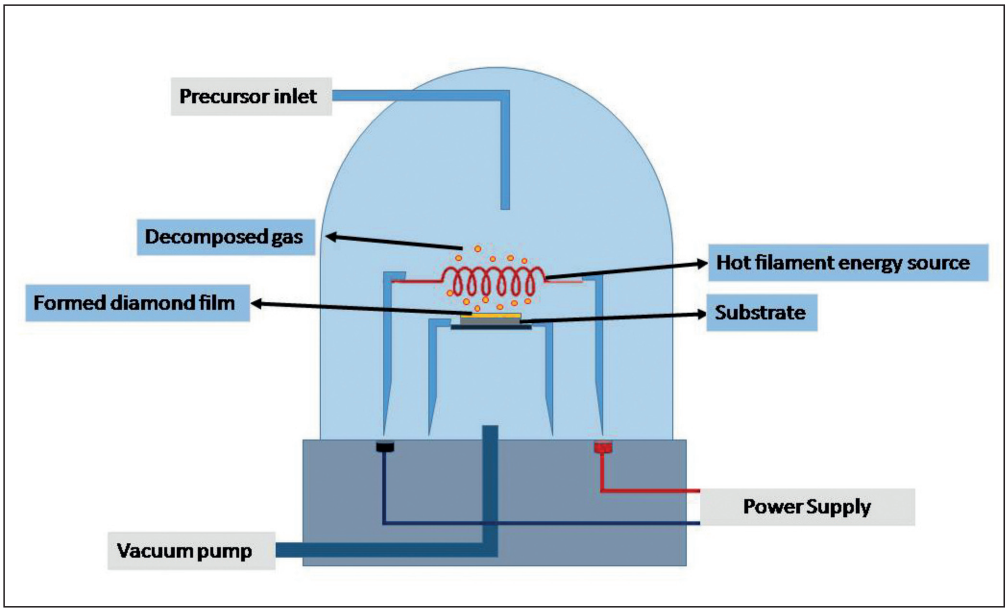


Figure of merit	Si	4H-SiC	GaN	Diamond	Implication for device
Johnson $JFOM = \frac{E_C v_s}{2\pi}$	1	215.1	215.1	81000	Power-frequency product rating
Baliga $BFOM = \epsilon \mu E_G{}^3$	1	223.1	186.7	25106	Unipolar high frequency device rating

Diamond far outperforms other semiconductors in terms of thermal conductivity in particular and other electronic properties as well. The FOMs attest to the advantages of using diamond over other semiconductors



Generic HFCVD system for depositing diamond on a substrate

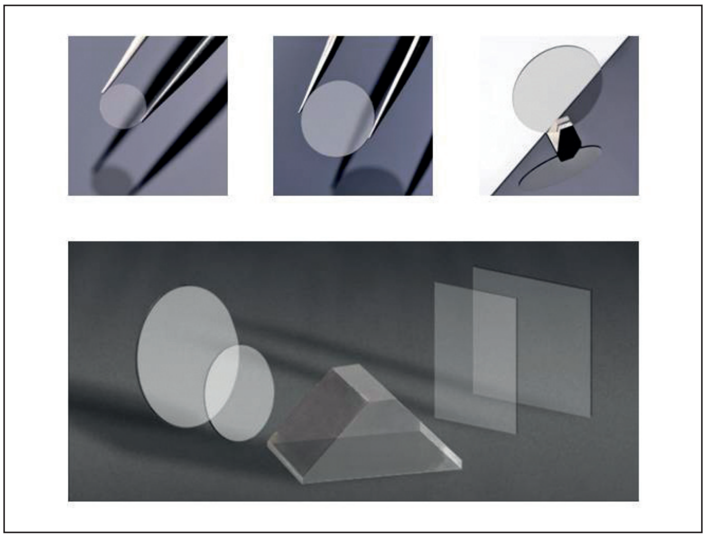
defect density lower than 0.1 cm -2 , resistivity lower than 0.005 Ω cm and a size of 4 inches; only these wafers will truly allow one to exploit the unique properties of diamond for electronics applications.

With respect to size: homo- and hetero-epitaxial diamond growth represent the two competing approaches for the realization of large-area diamond substrates. A disadvantage of hetero-epitaxial techniques is the high dislocation density, which comes from the variation of the substrate material. Promising technologies like epitaxial lateral overgrowth (ELO) technique and mosaic wafer fabrication method are being investigated to address this very problem. For reducing dislocation densities in homo-epitaxial growth, one needs a virtually defect-free HPHT crystal, achieved by reducing the dislocation density of the crystal used as seed for the HPHT process.

With the advances in CVD technology, large-area insulating and semiconducting PCD wafers can now be obtained. The optimization methods for these technologies are directed towards improving the ratio between grain and grain boundaries. Researchers use them to try new device concepts and evaluate the increase in efficiency and life time of the components. This stimulates not only research interest but brings forth interesting and useful characteristics in devices which can then be utilized by the industry.

Another challenge facing the diamond industry is the availability of low resistivity wafers. The fabrication of diamond bipolar devices depends on the capability of providing both n and p carriers in a controlled manner. P-type semiconducting diamond is easily achieved by doping with boron atoms, however obtaining n-type CVD diamond is more difficult because of the rigidity of the diamond lattice. Efficient incorporation of phosphorus has only been achieved on (111) oriented surfaces. However, n-type silicon carbide and p-type diamond are two materials that share a similar lattice structure and form a very unique heterojunction with some of the highest rectification ratios ever reported. These heterojunctions may provide a way to exploit novel bipolar device designs involving diamond.

HPHT boron-doped single crystals have been fabricated already with the largest reported size of 8 mm. By incorporating boron in the precursor gas, it is possible to obtain diamond with a resistivity as low as 0.0012 Ω cm. With these developments, one may expect high quality B-doped diamond wafers in the near future.



Commercially available CVD, poly-crystalline diamond wafers of diameters 5 mm, 8 mm and 25 mm and (bottom) commercially available single crystal, electronic grade diamond with thermal conductivity in the 18-20 W/mK range Source (3): University of Aveiro

Diamond for CMOS

It is widely accepted that CMOS technology and transistor performance improvement can still be sustained in the near future through the development of new materials and transistor structures. In recent years, H-terminated diamond has received a lot of attention. A variety of transistor structures (such as low on-resistance FETs, triple-gate FETS, vertical type with trench gate FET and FETs capable of high RF output power, high temperature and high voltage operation) using primarily the conductive H-terminated diamond surface and oxides such as aluminium oxide, yttrium oxide and high-k zirconium oxide have been fabricated with sub- micron gate lengths. A 50 nm diamond transistor demonstrated the highest transition frequency among diamond FETs of 55 GHz. More recently, H-diamond NOT and NOR logic circuits composed of depletion and enhancement mode MOSFETS have also been demonstrated.

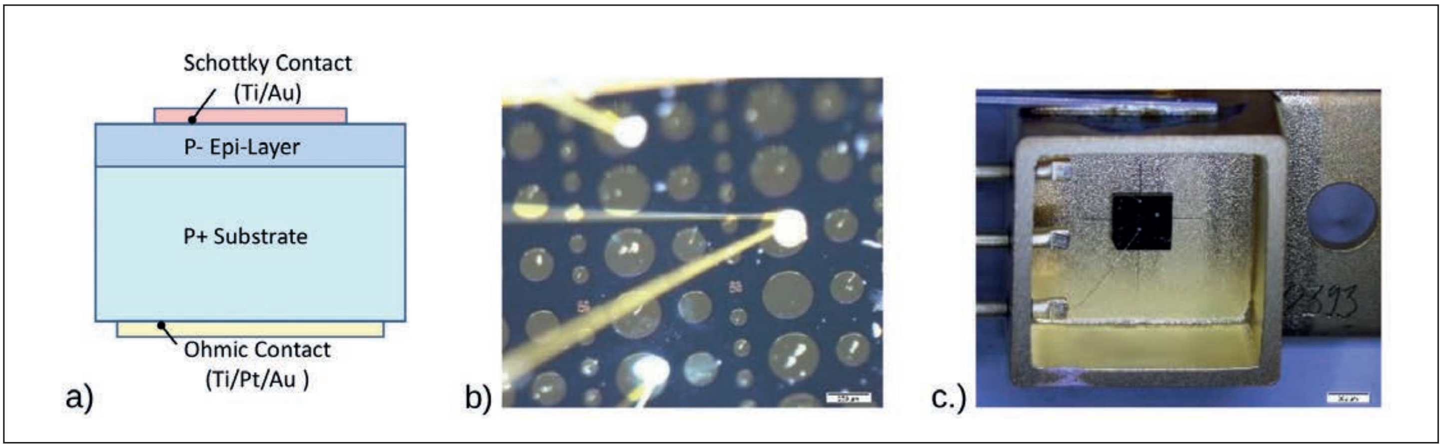
Diamond has exceptionally high thermal conductivity and low thermal expansion coefficient and therefore, can be used as an addendum to the substrate material for CMOS technologies, improving thermal management and enhancing the performance of silicon based transistors by reducing their thermal load. SOI (silicon-on-insulator) substrates are used to reduce parasitic device capacitance in CMOS chips, providing better dielectric isolation in both vertical and horizontal directions, improving performance and enabling harsh environment operation. The integration of diamond and Silicon in order to have SOD (silicon-on-diamond) wafers that serve the same purposes as SOI but are functionally more efficient, is a subject of eager sinvestigation.

Diamond for power electronics

These promising properties are the motivation for ongoing research activities in development of diamond-based power devices. Material quality and device technology is currently improved. Already today diamond Schottky- and PIN-diodes achieve remarkable performance in static- and

dynamic- measurement setups. Still outstanding are investigations in power electronic applications. A diamond Schottky diode in a non-isolated buck converter for LED voltage converter application at mains voltage has already been demonstrated by Fraunhofer IAF, Freiburg/Germany, **(www.iaf.fraunhofer.de)** at PCIM Europe 2019.

For the fabrication of the Schottky-diodes 3×3×0.3 mm^3 Iib HPHT diamond substrates of (001)-orientation with boron concentrations of 2 × 1020 cm-3 were used as base material. On top of those p+ substrates, p-layers were grown by microwave-enhanced chemical vapor deposition with doping concentrations of around 1016 cm-3 as characterized by cathode-luminescence and capacitance-voltage measurements of the Schottky contact.



Diamond Schottky diode: a) schematic device structure, b) top-view of the diamond chip with an array of different size Schottky contacts, c) assembled device in a TO247 package
Source: Fraunhofer IAF

The boron doped p- layer has a thickness of about 5.5 µm. Schottky electrodes of Ti/Pt/Au with diameters of 100 µm, 200 µm and 300 µm were realized on top of the p- layer and an ohmic contact using Ti/Pt/Au was formed on the backside of the p+ substrate. The fabricated device is attached with conducting adhesive in a TO247 engineering package. Three of the 300 µm diameter Schottky contacts are connected to the package-pins by Au wire bonds having a diameter of 25 µm. Furthermore, the pins are interconnected in parallel to achieve a total active device area of 0.0021 cm^2.

The physical properties of diamond are ideally suited for power electronic devices. Current research aims for the improvement of process and material quality as well as device technology. The fabricated diamond diodes in this work show a promising performance with breakdown voltages up to 1250 V at small diameters, forward currents up to 1 A at an area of 0.0021 cm^2 and a very low corresponding reverse recovery charge below 1 nC. But the cost of diamond of 1000 $/$cm^2$ on a 2-inch wafer is very high compared to GaN of 100 $/$cm^2$.

Literature

Debarati Mukherjee, Joana Catarina Mendes, and Luis Nero Alves: "Why Moore might love diamond", University of Aveiro, Portugal **(joanacatarina.mendes@av.it.pt)**

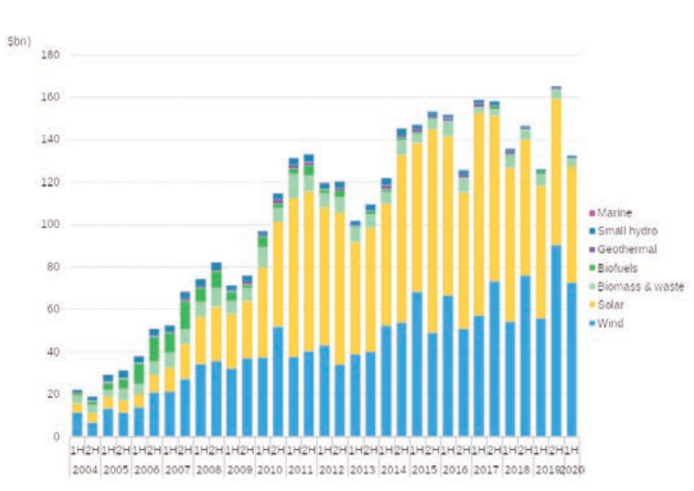
Fraunhofer IAF, Germany: "Diamond Schottky Diode in a Non-Isolated Buck Converter", Proceedings PCIM Europe 2019, pages 212 – 216 **(richard.reiner@iaf.fraunhofer.de)**

Global Investment in Renewables Capacity Rose 5 Percent

Renewable energy capacity investment showed great resilience in the first half of 2020, in the face of the unprecedented economic shock caused by the Coronavirus, according to the latest figures from research company BloombergNEF (BNEF).

Offshore wind financings in 1H 2020 totaled $35 billion, up 319 % year-on-year and in fact well above 2019's record full-year figure (a revised $31.9 billion). The first half of this year saw investment decisions made on 28 sea-based wind farms, including the largest ever, the 1.5 GW Vattenfall Hollandse Zuid array off the coast of the Netherlands, costing an estimated $3.9 billion.

Other major offshore deals included the 1.1 GW SSE Seagreen project of the UK, at an estimated $3.8 billion; the 600 MW CIP Changfang Xidao array of Taiwan at an estimated $3.6 billion; and the Fecamp and Saint-Brieuc projects in French waters, together totaling 993 MW and $5.4 billion. There were no fewer than 17 Chinese installations financed, led by the Guangdong Yudean Yangjiang Yangxi Shapaat 600 MW and $1.8 billion. "Offshore wind is benefitting from the 67 % reduction in levelized costs achieved since 2012, and to the performance of the latest, giant turbines. But the first half of this year also owed a lot to a rush in China to finance and build, in order to take advantage of a feed-in tariff before it expires at the end of 2021. I expect a slowdown in offshore wind investment globally in the second half, with potentially a new spike early next year," said Tom Harries, head of wind analysis. Overall investment in new renewable energy capacity (excluding large hydro-electric dams of more than 50 MW) was $132.4 billion in the first half of 2020, up 5 % from a revised $125.8 billion in the same period of 2019. Onshore wind investment slipped 21 % to $37.5 billion, while that for solar fell 12 % to $54.7 billion.



Global investment in renewable energy capacity, by half year, $ billion

Source: BloombergNEF

UK Lithium-Ion Gigafactory Becomes Reality

UK Britishvolt announced the down selection of two promising sites for the UK's first 30+ GWh gigafactory, from an initial 42 locations, with Bro Tathan in South Wales leading the way.

The battery industry is forecast to be worth £5 billion domestically by 2025, and the demand for lithium ion cells across a number of industries, including vehicle electrification, is already increasing dramatically, and risks becoming constrained as the UK Government strives to meet its Road to Zero targets by 2050. Not only is Britishvolt filling this gap in the market, but is also moving to leverage the UK's world-leading lithium-ion battery research development and academic community. The initial wave of £1.2 billion of investment into the site will eventually lead to around 3,500 jobs.

Britishvolt also announced plans to build a solar park alongside the factory, to support sustainable production of batteries and meet low carbon objectives, ensuring the firm plays a true and active part in the global green agenda. "We aim to deliver a scalable, onshore production and diverse portfolio of world-class lithium-ion batteries, to support the unprecedented transition to electrification – primarily servicing the automotive and energy storage markets. The sheer scale of this project means our gigafactory will have one of the top three largest single footprints in Europe. The plant will be one km long and 30 metres tall, needing 80 plus hectares of land, and the energy intensive nature of producing lithium ion cells means nearby renewable sources are of huge importance. Our state of the art and high efficiency gigaplant will employ at least 3,500 local Welsh people. These will be across a wide range of disciplines and will create a local ecosystem of 10,000 to 15,000 further jobs for the wider supply chain – including material suppliers, contractors and local services. By the third quarter of 2023, we plan for the first stage of our plant to be fully functional, and envision that between 40 and 60 percent of the initial £1.2 billion of investment will be injected directly into the chosen community, representing a real catalyst for growth in the local economy and the UK," commented Lars Carlstrom, CEO at Britishvolt.

On June 15 Britishvolt announced the appointment of seasoned battery industry professional Isobel Sheldon as Chief Strategy Officer (CSO) and Head of the Advisory Board, to support building the gigafactory. Having amassed nearly 20 years of Lithium ion battery industry experience, she joins the company from the Government-backed UK Battery Industrialisation Centre (UKBIC) – which aims to transition the country into a world leader in cell design, development and manufacture for vehicle electrification – where she served as Director of Business Development. Prior to this, she held senior leadership positions within global companies, recently serving as Engineering and Technology Director at Johnson Matthey Battery Systems, where she led the technical strategy and execution within the battery systems business. "As one of the first pioneers to integrate lithium ion batteries in road vehicles, including the first commercially available Plug in Hybrid in the world based on the Toyota Prius hybrid in 2003, I have developed a wealth of knowledge on a wide range of disciplines – from cell technology, chemistries and system integration to how the global industry and supply chain works, as well as the processes involved in manufacturing the cells. This gigafactory is not only one of the most exciting green projects currently taking place in the world, for both the automotive and energy sectors, but will be of huge national importance as the UK Government looks to fulfil its green agenda and meet its Road to Zero targets", Isobel Sheldon stated.

Cheaper Production of Green Hydrogen

By 2030 the production of hydrogen fuel by “splitting” water, which can be carbon-free provided the electricity used in the process is produced by renewables, could become cost competitive with currently predominant methods that require the use of natural gas as a feedstock, according to analysis by the IHS Markit Hydrogen and Renewable Gas Forum.

This so-called “green” hydrogen produced by electrolysis - a process that uses electricity to split water into hydrogen and oxygen - is rapidly developing from pilot to commercial-scale operation in many parts of the world. “Costs for producing green hydrogen have fallen 50 % since 2015 and could be reduced by an additional 30 % by 2025 due to the benefits of increased scale and more standardized manufacturing, among other factors,” said Simon Blakey, IHS Markit Senior Advisor, Global Gas. Investment in so-called “power-to-x” projects, of which hydrogen makes up the large majority, is growing rapidly. Investment is expected to grow from around $30 million in 2019 to more than $700 million in 2023. Economies of scale are a primary driver for green hydrogen’s growing cost competitiveness. The average size for power-to-x projects scheduled for 2023 is 100 MW, ten times the capacity of the largest project in operation today. Hydrogen’s overall share in the energy mix will ultimately depend on the extent of decarbonization that is desired. In Europe, currently the primary market for hydrogen projects, hydrogen could account for as much as one third of the energy mix if the aim was 95 % decarbonization or greater. “In Europe it is now widely agreed that electrification alone cannot deliver the level of emissions reduction that many countries aspire to,” said Catherine Robinson, IHS Markit Executive Director, European Power, Hydrogen and Renewable Gas. “Hydrogen is a highly versatile fuel, both in terms of how it can be transported and the variety of its potential end-use applications. The greater the degree of a decarbonization, the greater the likely role of hydrogen in the energy future.”

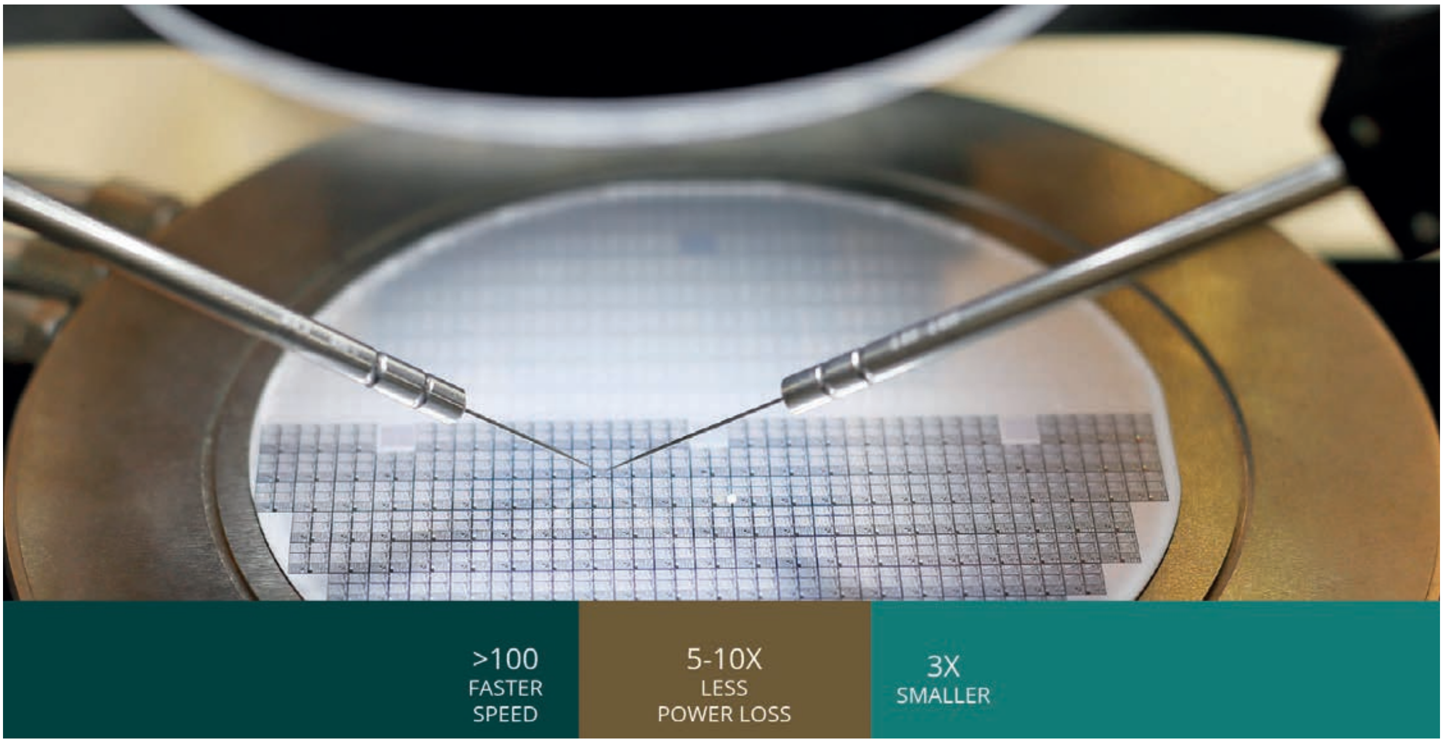
www.ihsmarkit.com

European € 10.3M GaN Project

Cambridge GaN Devices Ltd. (CGD) leads € 10.3M project with 13 European Partners to deliver the most energy-efficient GaN power modules. The GaNext Penta project is undertaken by a powerful consortium with complementary expertise in GaN technology, high-frequency drivers, magnetics, smart controllers and end-user dedicated applications in the diverse field of power electronics. The consortium involves 13 partners from the industry and academia, covering all aspects of power conversion. Cambridge GaN Devices (CGD) was spun out of the High Voltage Microelectronics and Sensors group in the Department of Engineering at Cambridge University in 2016 to develop Gallium-Nitride on Silicon substrate power semiconductors.

CGD is developing GaN devices that can be driven in a similar way to Silicon transistors and are easy to use. The company’s technology allows easy control using standard MOSFET drivers as well as micro-controllers and complements this with additional smart features and protection functions, fully embedded into its product solutions. “Thus the Penta project creates a tremendous opportunity for CGD to engage with leading-edge companies in the area of power electronics. Not only will the project advance the knowledge in GaN technology and provide insights into its complex facets, but will aim at delivering fully-working prototypes in lighting, motor drives, converter blocks for renewable energies and on-board chargers for automotive with record specifications and outstanding performance," said Dr Giorgia Longobardi, CGD's founder and CEO. Prof Florin Udrea, professor in semiconductor engineering, CTO and founder added: "The quality of the Penta consortium is remarkable and I have no doubt that we will deliver on the promises to make GaN technology a great success in the market. There is also a broader impact in adding our contribution to our ultimate quest for better use of energy resources and a cleaner environment."

www.camgandevices.com



World's Smallest Voltage Regulators

Integrated Voltage Regulators (IVRs) featuring three outputs with no discrete components and can also be integrated directly into a SoC package to further reduce the power area and energy consumed.

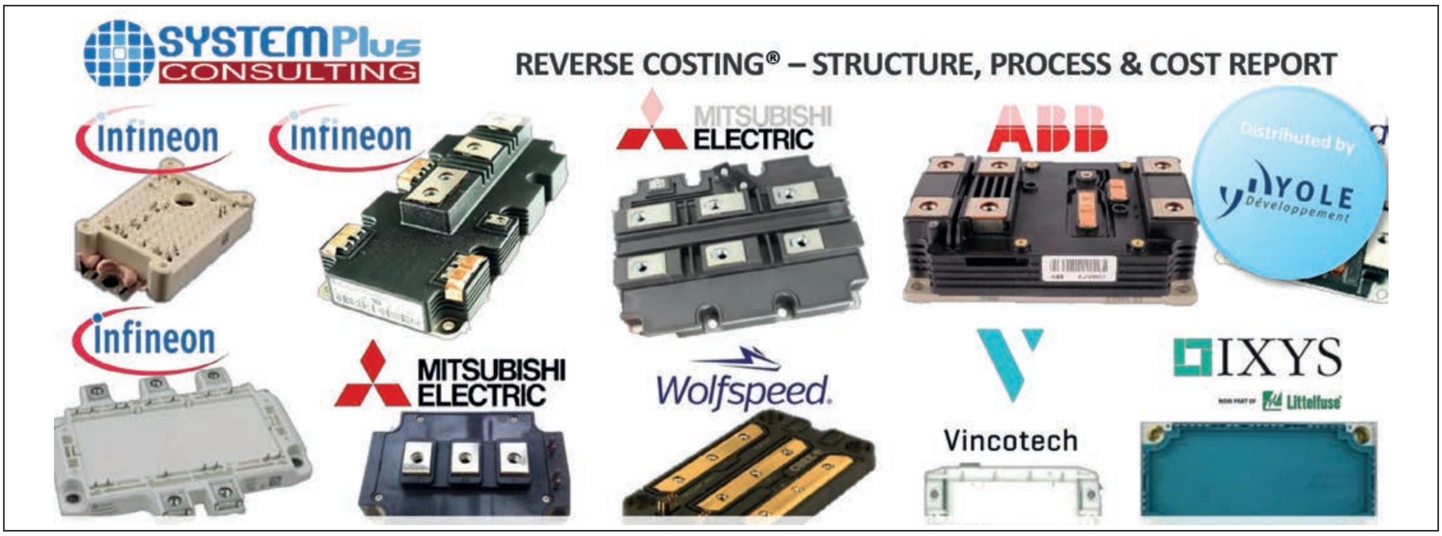
Empower Semiconductor announced on June 23 the EP70xx, a family of a triple output DC/DC power supply with no external components into a single tiny package. With a single footprint, no external components, extensive programmability, a wide range of current and output configurations, power designers can proliferate the EP70xx across nearly all designs and platforms. By having multiple entire power supplies in a single IC package, the usual concerns of component variation and sourcing, synchronization and stability are all either eliminated or reduced significantly. The EP70xx family displays peak efficiencies of up to 91 % with a nearly flat efficiency curve up through 10 A of output current due to its unique architecture. "Our patented Integrated Voltage Regulator technology integrates dozens of components into a single IC increasing efficiency, shrinking footprints by 10x and delivering power with unprecedented simplicity, speed & accuracy and with zero discrete components. This IVR technology addresses a $6B opportunity with a wide range of applications including mobile, 5G, AI and data centers," said Tim Phillips, Chief Executive Officer of Empower Semiconductor - founded in 2014. Other founders include industry veterans such as Gene Sheridan, Executive Chairman and currently CEO of Navitas Semiconductor; and David Lidsky, Strategic & Technical Advisor. These newly IVR products fully integrate all power supply discrete components, thereby simplifying the design process and shrinking the PCB area consumed by power management. By using an advanced CMOS geometry platform, the devices can also be integrated directly into a SoC package to further reduce the power area and energy consumed. Product samples, demo boards, and reference designs of the EP70xx family with input voltages varying from 2.5 V to 16 V are available to qualified customers. "We made it simple to place the EP70xx on the PCB with no discrete components, select settings using the provided GUI, and load the device via the I^2C/I^2C port. Just like that you have three outputs regulating at high currents with wide bandwidth and high efficiency. No input filter design, no output filter design, no feedback resistors, no loop compensation design, no component changes necessary. The devices showcase 1,000x faster dynamic voltage scaling than competing products, enabling fast and lossless processor state changes that can save 30 % or more of processor power", said Trey Roessig, Chief Technology Officer.

www.empowersemi.com

Power Module Packaging Comparison

The market for power modules will be worth $6B by 2024 with a compound annual growth rate (CAGR) of 6.6 %. The power module market plays a key role in several industrial applications,such as motor drives and traction. In 2018, the biggest power module market segment is motor drives at $1.4B.

Module packaging currently faces several challenges, from housings to die attach and connections. To remain competitive, power module makers must deliver high reliability while remaining cost efficiently. In this dynamic context of the power module packaging market, System Plus Consulting provides a deep comparative review of packaging technology and cost, of 10 Industrial Power Modules from the main suppliers on the market: Infineon, Mitsubishi, IXYS, Vincotech, ABB, andWolfspeed. Analyzed are several packaging technologies to provide an insight into their structures, processes and costs. External parts, including cases, covers and baseplates, and their internal structure, including substrates, assembly of the substrates and modules, die and substrate attach andconnections, are examined. The cost of each power module packaging is detailed including external part costs, assembly cost per process step, and yield losses cost.



New CEO for Vincotech

Power module vendor Vincotech has appointed Eckart Seitter, Senior Vice President of Sales and Marketing, as CEO effective October 1, 2020. Eckart Seitter will succeed Vincotech's CEO and Chairman of the Board Joachim Fietz, who will retire after 12 years as CEO.

Eckart Seitter has been with the company for more than 20 years. He became Managing Director Sales and Marketing in 2013, and thus has made a strong contribution to Vincotech's development and success. Yuzuru Saito, Executive Officer of Mitsubishi Electric Corporation, expressed his appreciation to Joachim Fietz for his outstanding achievement. "We are grateful for his professional leadership, which has enabled Vincotech to bring enormous value to customers with the company's strength, speed and flexibility during his 12 years as CEO. We believe that Eckart Seitter, who has been a member of the management team since 2007, enjoys an excellent reputation in the industry and has established a trusting relationship with us, and will continue to expand his contribution and tackle further growth. This CEO change will ensure the long-term success of the Mitsubishi Electric Group's power module business."

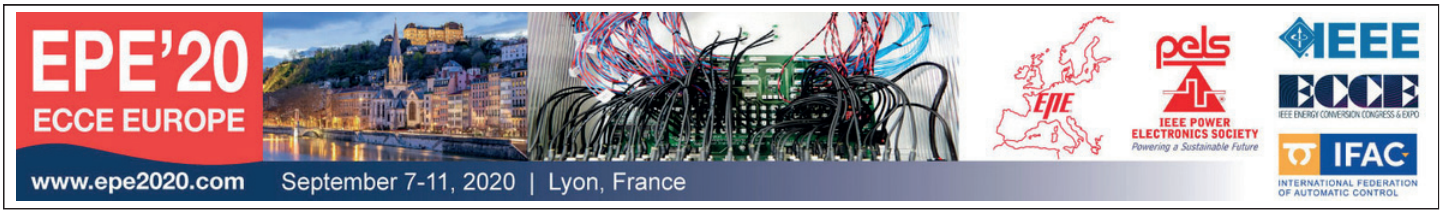
www.vincotech.com

ADI Acquires Maxim

Analog Devices will acquire Maxim in an all stock transaction that values the combined enterprise at over $68 billion.

Under the terms of the agreement, Maxim stockholders will receive 0.630 of a share of ADI common stock for each share of Maxim common stock they hold at the closing of the transaction. Upon closing, current ADI stockholders will own approximately 69 percent of the combined company, while Maxim stockholders will own approximately 31 percent. "Today's announcement with Maxim is the next step in ADI's vision to bridge the physical and digital worlds," said Vincent Roche, President and CEO of ADI. "Maxim is a respected signal processing and power management franchise with a proven technology portfolio and impressive history of empowering design innovation. Together, we are well-positioned to deliver the next wave of semiconductor growth, while engineering a healthier, safer and more sustainable future for all." Upon closing, two Maxim directors will join ADI's Board of Directors, including Maxim President and CEO, Tunç Doluca.

www.analog.com



EPE'20 is Going Virtual

The COVID-19 crisis is present everywhere on the planet, leading to travel restrictions and confinement in many countries and in whole continents. Thus EPE'20 ECCE from September 7 – 11 is going virtual

"Meeting several challenges, our organizing team is working very hard to offer attendees a one of the kind experience. We chose the Whova platform to support our event, offering enhanced discussion and networking capabilities. Zoom channels will ensure large audience discussion stability and smaller meetings will be possible using channels of choice. Participants, guests and organizers, we all are pioneers of this first virtual EPE ECCE Europe conference. On behalf of the organizing committee and myself, I would like to thank you all for your support and invite you, ladies and gentlemen, dear colleagues and guests, to join us from September 7 to 11 at EPE 2020 ECCE Europe, and to make it a real success," said .Abdelkrim Benchaib, EPE's Conference General Chairman.

The EPE ECCE Europe conference is said to be the largest in its field, attracting experts from numerous different countries every year to join in the discussions. With the objective to exchange and meet fellow professionals and academics, the EPE ECCE Europe conference brings together researchers, engineers, etc. working at the forefront of power electronics technologies. For this type of event, where the future role of power electronics in this ecological revolution will be explored, the EPE ECCE Europe conference is one of the privileged places. There will be the opportunity to discuss a vast number of subjects during EPE '20 ECCE Europe, not only during the virtual lecture and dialogue sessions of the conference, but also at the virtual exhibition, industrial forums and tutorials.

www.epe2020.com

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Radiation Hardened GaN by EPC Space

EPC Space, a joint venture company, will provide advanced, high-reliability, gallium nitride (GaN) power conversion solutions for critical spaceborne and other high reliability environments

Efficient Power Conversion (EPC) Corporation and VPT, Inc., A HEICO company announced the establishment of EPC Space LLC, a joint venture focused on designing and manufacturing radiation hardened (Rad Hard) GaN-on-Silicon transistors and ICs packaged, tested, and qualified for satellite and high-reliability applications. EPC Space will provide high-reliability power conversion solutions for critical spaceborne environments in applications including power supplies, light detection and ranging (lidar), motor drive, and ion thrusters. These GaN-based components offer superior performance advantages over traditional Silicon-based solutions. "This joint venture is taking the superior performance of gallium nitride to the high reliability community offering electrical and radiation performance beyond the capabilities of the aging Rad Hard Silicon MOSFETs," noted Alex Lidow, CEO and Co-founder of EPC at PEE's Panel Discussion 'Power GaN: Past – Present – Future' within PCIM's Digital Days early July.

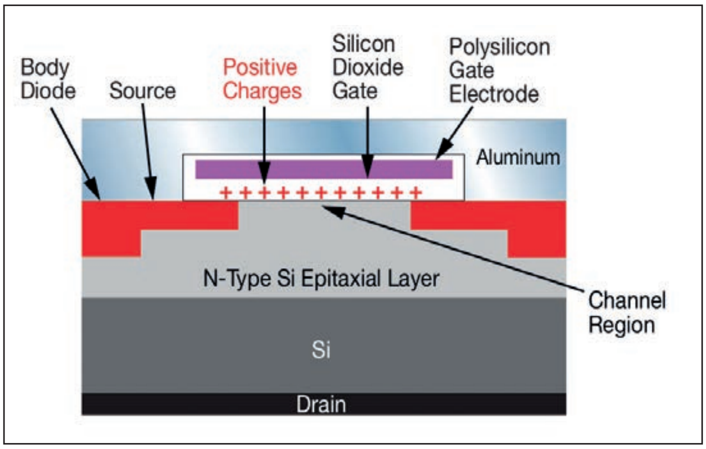
EPC's Space Rad Hard GaN discrete devices (40 V – 300 V / 4 A – 30 A) have been specifically designed for critical applications in the high reliability or commercial satellite space environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low on-resistance values.

An energetic particle can cause damage to a semiconductor in three primary ways; it can cause traps in non-conducting layers, it can cause physical damage to the crystal – also called displacement damage, or it can generate a cloud of electron-hole pairs that will cause the device to momentarily conduct, and possibly burn out in the process. In eGaN devices, energetic particles cannot generate momentary short-circuit conditions because mobile hole-electron pairs cannot be generated.

Gamma radiation

Gamma radiation consists of high energy photons that interact with electrons. In a Silicon based MOSFET, the gamma radiation knocks an electron out of the Silicon dioxide layer leaving behind a positively charged 'trap' in the gate oxide. The positive charge reduces the threshold voltage of the device until the transistor goes from normally off – or enhancement mode – to normally on – or depletion mode states. At this point the system will need a negative voltage to turn the MOSFET off. Typical ratings for Rad-Hard devices range from 100 kilo Rads to 300 kilo Rads. In some cases, devices can be made to go up to 1 M Rad, but these tend to be very expensive.

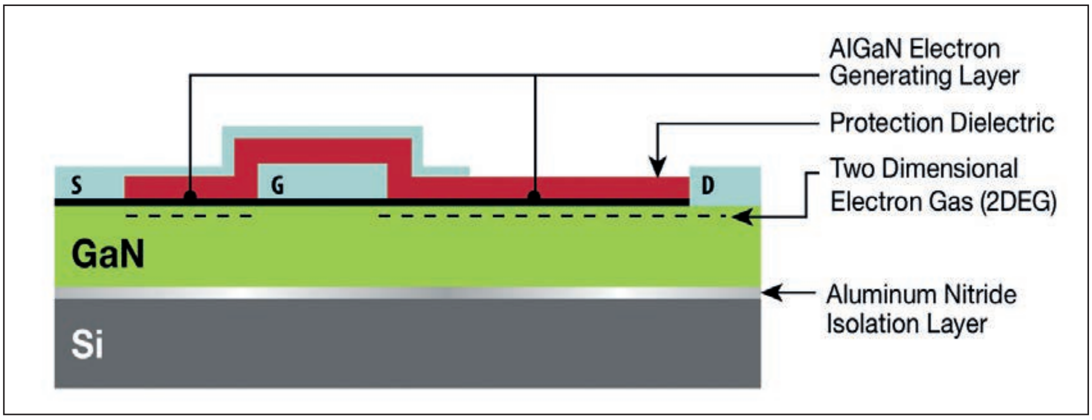
Enhancement mode GaN (eGaN®) devices are built very differently from a Silicon MOSFET. All three terminals; gate, source, and drain, are located on the top surface. Like in a Silicon MOSFET, conduction between source and drain is modulated by biasing the gate electrode from zero volts to a positive voltage – usually 5 V. The gate is separated from the underlying channel by an aluminum gallium nitride layer. This layer does not accumulate charge when subjected to gamma radiation.



Cross section of a typical Silicon MOSFET

To demonstrate the performance of eGaN devices, EPC Space's 100 V family of eGaN transistors were subjected to 500 kRad of gamma radiation. Throughout the testing, leakage currents from drain to source and gate to source, as well as the threshold voltage and on-resistance of the devices at various checkpoints along the way were

Gallium nitride FETs and ICs have been specifically designed for critical applications in the highreliability or commercial satellite space environments.



Cross section of a typical enhancement mode GaN device

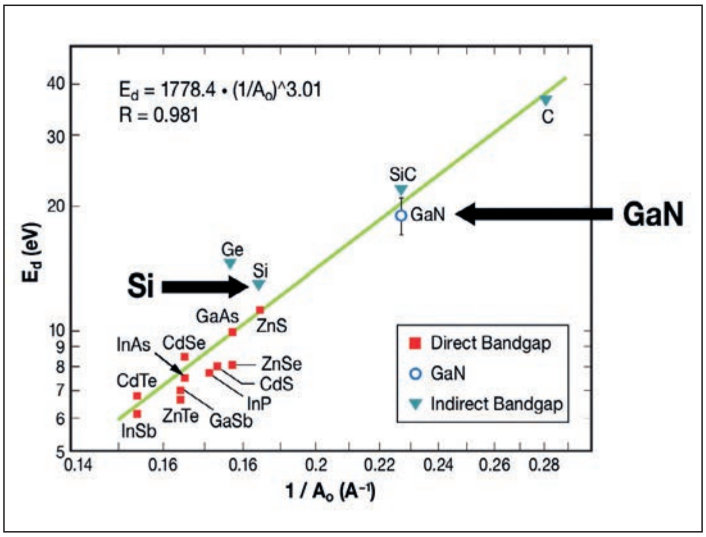
measured, confirming that there are no significant changes in device performance.

Since the initial testing, eGaN devices have since been subjected to 50 Mrads, confirming that eGaN devices will not be the first part to fail due to gamma radiation in any space system.

Neutron radiation

The primary failure mechanism for devices under neutron bombardment is displacement damage. High energy neutrons will scatter off atoms in the crystal lattice and leave behind lattice defects. As with gamma radiation, the impact of neutrons on the GaN crystal and the entire device structure is minimal.

The reason for GaN's superior performance under neutron radiation is that GaN has a much higher displacement threshold energy compared with Silicon.



Displacement energy compared with the inverse of the lattice constant for various crystals

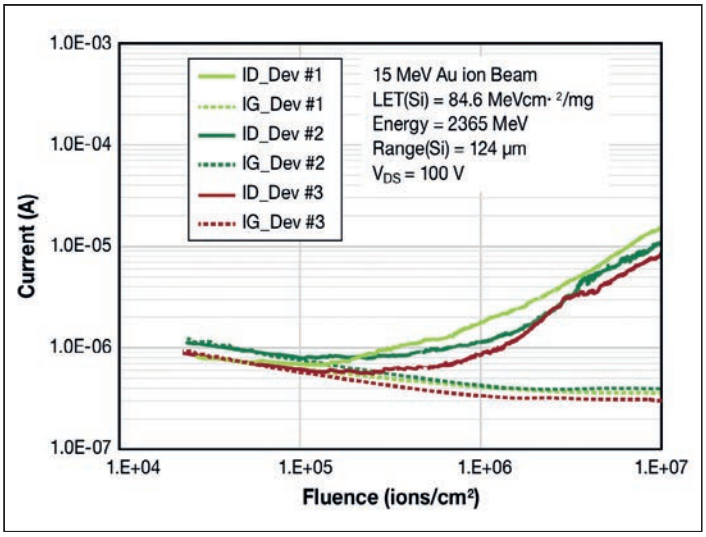
Single event effects (SEE)

SEE are caused by heavy ions generated by the impact of galactic cosmic rays, solar particles or energetic neutrons and protons. This can be simulated terrestrially by using a cyclotron to create beams of different ions. Two of the most common ions used to evaluate radiation tolerance of electronics components are Xenon, with a linear energy transfer (LET) of about 50 MeV·cm?/mg, and Gold, with an LET of about 85 MeV·cm?/mg.

In a Silicon MOSFET there are two primary failure mechanisms caused by these heavy ions, single event gate rupture, or SEGR, and single event burnout, or SEB. Single event gate rupture is caused by the energetic atom causing such a high transient electric field across the gate oxide that the gate oxide ruptures. Single event burnout, or SEB, is caused when the energetic particle transverses the drift region of the device where there are relatively high electric fields. The energetic particle loses its energy while generating a large number of hole electron pairs. These hole electron pairs crossing the drift region cause the device to momentarily short circuit between drain and source. This short circuit can either destroy the device, called a single event burnout, or the device can survive, appearing as a momentary short circuit that can cause damage to other components in the system. This latter case is called single event upset, or SEU.

Since eGaN devices do not have a gate oxide, they are not prone to single event gate rupture. Since eGaN devices to not have the ability to conduct large numbers of holes very efficiently, they are also not prone to single event upset. The primary failure mechanism for eGaN devices is heavy ion bombardment. The conditions are about the maximum conditions possible, with an 85 LET beam of gold atoms pummeling the device biased at the maximum data sheet limit.

EPC Space has tested many specially produced Gen 4 products for SEE under varied conditions. 40 V and 100 V product did not fail under any conditions up to full rated voltage and 87 LET. The first failures occurred at 85 LET and 190 V. The 300 V device failed at 85 LET and 310 V.



SEE primary failure mechanism for eGaN devices under heavy ion bombardment

eGaN devices for space

In summary, GaN power transistors and ICs are the best choice for power conversion applications in space-based systems. eGaN devices have proven to be more rugged than rad hard MOSFETs, when exposed to various forms of radiation. In addition, the electrical performance of eGaN devices is many times superior to the aging silicon power MOSFET.

Literature

EPC.Space, Application Note AN001, 'Radiation Performance of Enhancement-Mode Gallium Nitride Power Devices'

http://epc.space/, www.epc-co.com

Proving the Ruggedness of GaN technology in Automotive and Demanding Applications

To achieve the most efficient power conversion circuit requires the best semiconductor switch as the fundamental building block. Many people now consider gallium nitride to be a better switch than silicon. This is because GaN transistors feature a very low on-resistance and very high switching speeds; they are also rugged as they do not suffer avalanche breakdown of traditional MOSFETs. GaN is commonly used in RF and LED applications, yet employing GaN as a power technology brings new challenges. This article discusses product robustness, quality and reliability issues at high voltage and high temperatures, for Nexperia's latest 650 V power GaN FET technology which is now qualified in accordance with AEC-Q101 automotive standard. **Dr. Dilder Chowdhury, Dr. Jim Honea, Nexperia, Nijmegen, Netherlands**

Wide bandgap (WBG) materials offer a combination of higher critical electric field performance and greater electron mobility which together result in devices with lowest RDS(on) (source drain on state resistance) at higher voltages and significantly better switching FOM (Figure of Merit). Unlike the various different Silicon transistor implementations – vertical, lateral, super-junction etc –, GaN technology reduces both switching and conduction losses, resulting in a very significant improvement in switching efficiency. Therefore, for most designers the argument as to which technology results in the best power switch is over – it's GaN. However, proving the robustness of GaN switches in operation, plus the quality and reliability of the technology and its scalability raises different questions.

GaN devices are beginning to become generally available on the market. Many show significant promise and do not suffer from the limitations of Silicon IGBT and super-junction (SJ) devices. For example, some of the hard-switched topologies where Silicon SJ FETs cannot be used due to the reverse recovery diode losses can easily use GaN FETs, thereby benefiting from reduced component count and higher efficiency with simpler control schemes.

Currently GaN FETs are produced in two main types: Enhancement (E)-mode normally-off single die products; and Depletion (D)-mode normally-off two die, often termed cascode styles. While a single die solution would seem to offer obvious size and cost advantages, driving E-mode devices is complex, especially for high-voltage high-power applications. The stability and leakage current of E-mode devices can also be a concern. To avoid gate-bounce and harmful shoot-through, a high gate threshold voltage and stable gate drive is necessary. Currently existing E-mode technologies have a gate threshold of only around 1 V. In contrast, Nexperia's new H2 cascode GaN HEMTs achieve a gate threshold equal to 4 V, and the gate drive is relatively simple. To achieve a normally-off operation, Nexperia packages a small Silicon MOSFET on top of the HEMT source. Dynamic matching of the

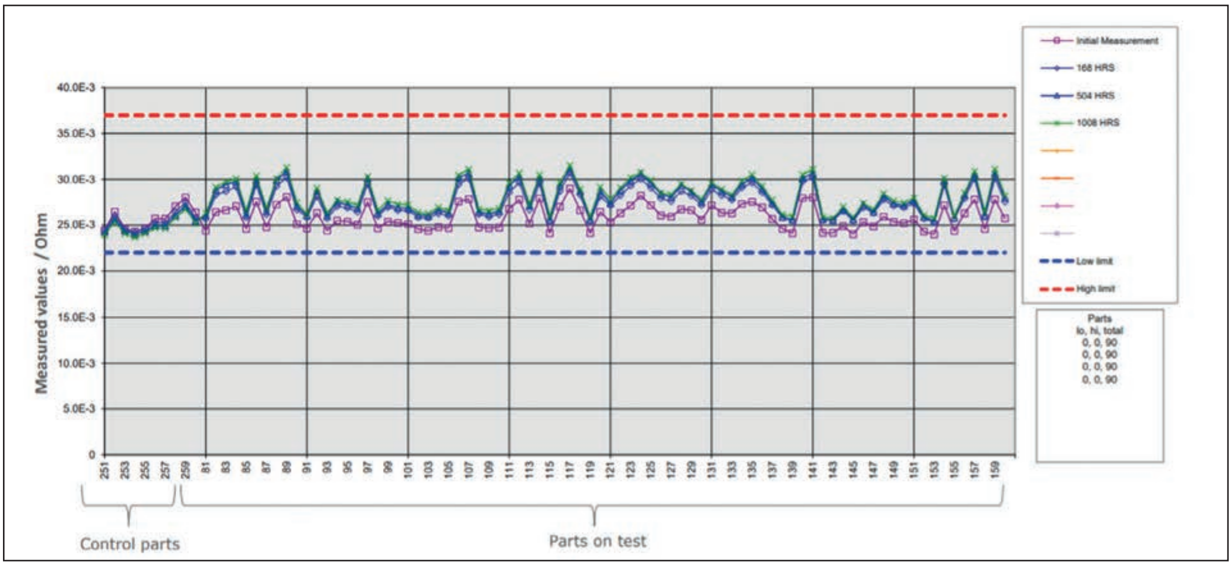


Figure 1: Dynamic RDS(on) measurement during 650 V 175°C HTRB tests

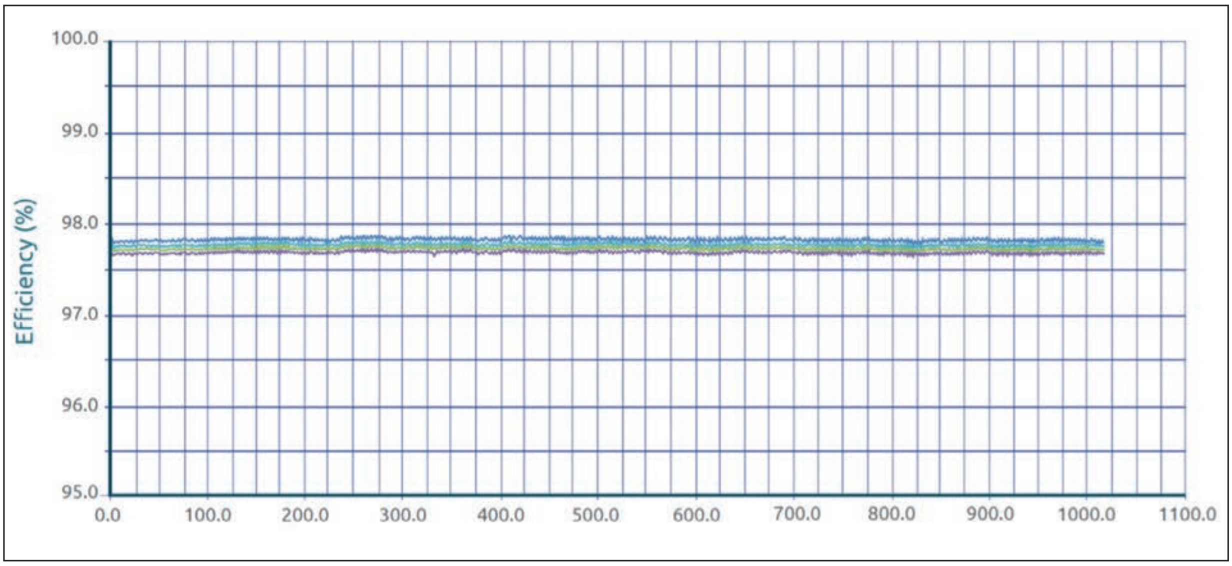


Figure 2: Efficiency of boost converters (HTOL) over 1000 hours

pair is ensured because Nexperia makes both the GaN transistor and the Silicon MOSFET in-house. This structure means that the switch is simply a Silicon MOSFET gate, which engineers have been used to driving for two decades.

Nexperia buys in GaN-on-Silicon wafers and is able to scale up production at its existing fabs by bringing on more lines and utilizing increased wafer sizes from 150 mm to 200 mm as part of a planned expansion program that is already in progress.

Robustness

H2 650 V GaN FETs have an operating temperature of -55°C to +175°C with T_{jmax} of 175°C. As mentioned, devices have a high 4 V threshold voltage which provides a wide safety margin against gate-source transients. Gate structure is also very reliable (± 20 V), and the 650 V rated parts handle switching transients of up to 800 V reliably. Body diode characteristics include a very low V_f of 1.3 V, enabling a Silicon-like freewheeling current capability without complex dead time adjustments (parameters from the 50 mΩ GaN FET @ 25°C).

Quality qualification

Nexperia's latest generation GaN FETs are qualified in accordance with AEC-Q101 Rev D. High Temperature Reverse Bias (HTRB) tests (1000 hrs) and dynamic $R_{DS(on)}$ shift tests were performed on 50 mΩ (typ @ 25°C) 650V device. 'Dynamic' $R_{DS(on)}$ is used to emphasize that $R_{DS(on)}$ measurements are taken from a dynamic, switch-mode test - this is important for GaN FETs to detect any short-term change due to charge trapping. Temperature cycling tests (1000 cycles) were performed over the range of -55°C to 150°C. High temperature (175°C) Gate positive (+20 V) and negative (-20 V) bias tests plus high temperature biased and unbiased humidity tests and operating life tests were also performed.

The condition for passing AEC-Q101 HTRB testing is that $R_{DS(on)}$ must not shift by more than 20 %. Figure 1 shows that the maximum shift in dynamic RDS(on) is less than 15 %. An additional HTRB test was performed and passed at 800 V for 10 hours. This voltage is well above the DC rating, but does correspond to the repetitive transient voltage rating.

High Temperature Operating Life (HTOL) tests are not part of the AEC-Q101 standard, but are useful in validating reliability of the parts under actual operating conditions. This is particularly important for new materials, like GaN, to ensure that any new or unfamiliar failure modes are uncovered. A basic half-bridge operating in continuous conduction mode provides the most fundamental exercise of switching behavior. For this test, a number of identical half-bridge circuits were prepared using two each of the GaN063-650WSA. These were operated continuously as synchronous-boost converters with the following conditions:

- Vin = 200 V
- Vout = 480 V
- Pout = 800 W
- Tj = 175°C
- Frequency = 300 kHz

Figure 2 shows the efficiency of all samples during the 1,000 hour test. As may be seen, there is no indication of degradation in any of the sample circuits. Following the tests, all devices were tested for shifts in dynamic RDS(on), leakage current, and threshold voltage. All parameters were found to be stable, with

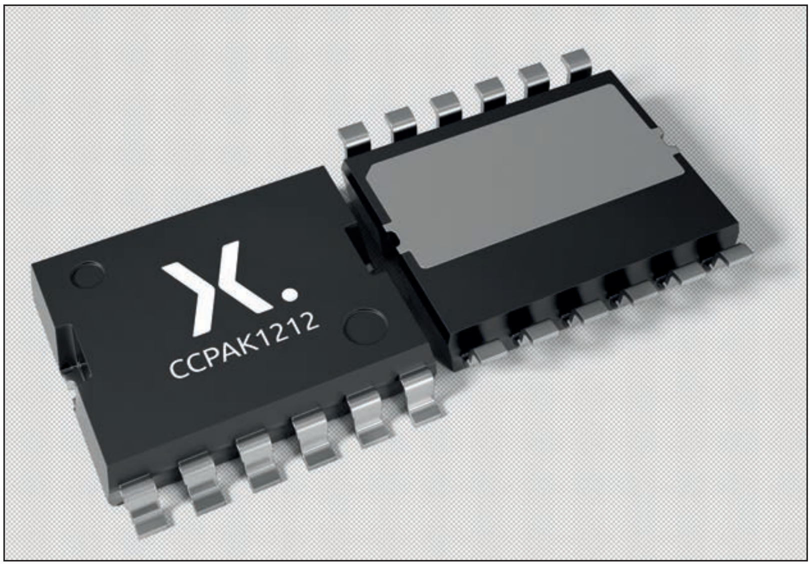


Figure 3: CCPAK copper-clip surface-mount packaging also for power GaN

any parametric shift within allowed levels. The HTOL test results also indicate excellent product quality.

Packaging

Packaging affects both device performance and reliability. Nexperia offers two package options for its H2 GaN FETs: the conventional TO-247 which has a thermal resistance ($R_{th(j-mb)}$) of 0.8 K/W and an operating temperature of up to 150°C at the junction; and a surface mount copper clip CCPAK version with an $R_{th(j-bm)}$ of <0.5 K/W which will operate up to 175°C. The CCPAK surface-mount packaging, shown in Figure 3, adopts the company's copper-clip package technology to replace internal bond wires. This reduces parasitic losses, optimizes electrical and thermal performance, and improves reliability. CCPAK GaN FETs are available in top- or bottom-cooled configurations making them very versatile and help further improving heat dissipation. As gull-wing devices, the CCPAK allows some flex to reduce the stress from thermal cycling and eases automatic optical inspection – important for automotive use.

Conclusion

Power GaN technology is being used in applications such as on-board chargers, DC/DC converters and traction inverters in electric vehicles, and industrial power supplies in the 1.5- to 5-kW range for titanium-grade rack mounted telecoms, 5G and data centres. Nexperia's latest devices have the proven product and technology robustness, quality, reliability and volume manufacturability necessary for these applications. Current devices offer industry-leading $R_{DS(on)}$ performance down to 39 mΩ. In the near future this will reduce to <20 mΩ and even <10 mΩ, enabling the parts to address higher power applications up to 150 kW with the sub-10 mΩ transistors.

Demonstrator for GaN EV Inverter

Nexperia partners with renowned automotive engineering consulting company, Ricardo, to produce a technology demonstrator for an EV inverter based on GaN technology.

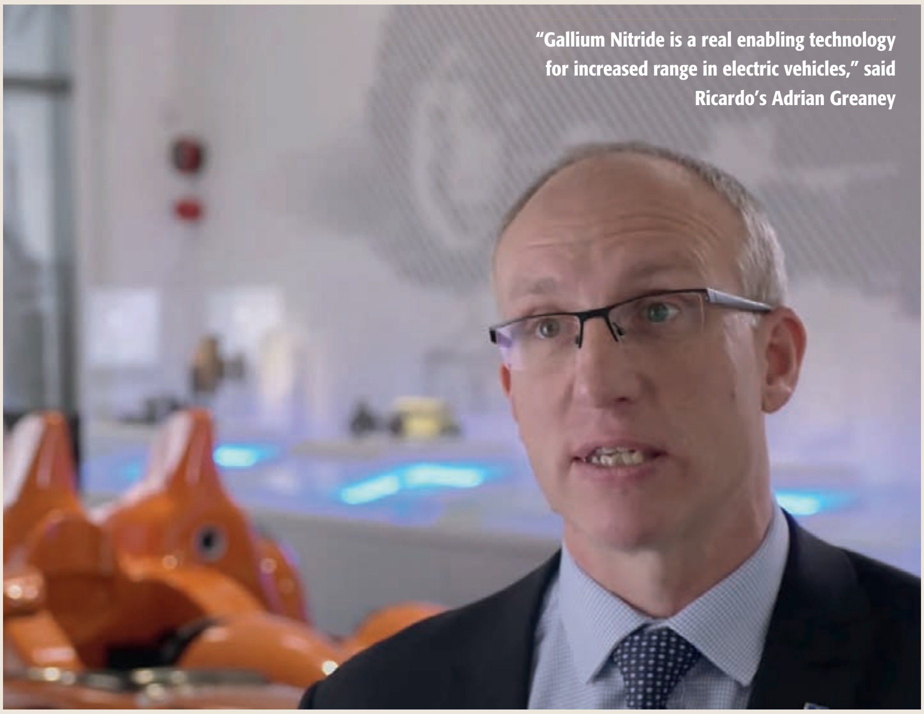
With every gram of CO2 exhaust being vital in today's cars, it is driving the move to vehicle electrification. From hybrids through to full electric vehicles, electrification of the powertrain is expected to dominate power semiconductor market growth in the next two decades. The power density and efficiency of GaN-on-Si will play a leading role in this space, specifically for on-board-chargers (EV charging), DC/DC converters and motor drive traction inverters (xEV traction inverters).

GaN is the preferred switch for these applications as GaN FETs lead to systems with greater efficiencies at lower costs with improved thermal performance and simpler switching topologies. In automotive terms this means that the vehicle has a greater range – the major concern for anyone looking to buy an electric vehicle. GaN is now on the brink of replacing Silicon based IGBTs as the preferred technology for the traction inverters used in plug-in hybrids or full battery electric cars.

Nexperia announced a range of AEC-Q101-approved GaN devices as shown above, providing automotive designers with a widening portfolio of reliable devices in this high-efficiency technology, providing the power density required for electrification of the powertrain. Ricardo is very well regarded in the automotive industry, the Global engineering innovation company designs and consults on concepts within the automotive industry, including the manufacture of prototypes and demos, and boast collaborations with high-profile leading brands such as McLaren and Bugatti. Thus Ricardo was the perfect partner for Nexperia for this project.

Michael LeGoff, General Manager GaN, Nexperia: "By designing our GaN devices into an inverter and trialing them through Ricardo, we will be able to better understand how a vehicle can be driven safely and reliably. We are developing a real solution that I think a lot of automotive designers will be interested in having a look at and will find extremely advantageous." Adrian Greaney, Director Technology & Products, Ricardo: "Semiconductor technology is key to the efficiency of the inverter system and the role that it plays in the performance and efficiency of an electrified vehicle. By delivering significant benefits in terms of the switching speed and efficiency, gallium nitride is a real enabling technology. As well as leading to increased range, it allows us to reduce the package size and weight of the inverter, which provides greater powertrain design flexibility as well as contributing to vehicle mass reduction. There are also many associated benefits that when we look at the design from a system level, and Ricardo is therefore pleased to be collaborating with Nexperia on GaN devices."

www.ricardo.com



"Gallium Nitride is a real enabling technology for increased range in electric vehicles," said Ricardo's Adrian Greaney

New Inverters for Efficient EV Battery Charging and Solar Energy Generation

The race for power conversion efficiency over 99 % continues. New innovative topologies are competing with the standard half-bridge topology using SiC and GaN semiconductor technologies. Requirements for high-efficient power conversion both unidirectional and bidirectional are getting standard in the wide field of applications ranging from EV battery chargers, solar inverters and UPS to industrial drives with built-in or separate PFC. **Temesi, Erno, Chief Engineer and Michael Frisch, Head of Product Marketing, Vincotech, Hungary/Germany**

In order to be able to make further cutting on the remaining losses of the power conversion, the process requires deep analyses on the loss composition. The main sources of the losses originate from the non-ideal static and switching characteristics of the power semiconductors. The second highest contribution to losses comes from the parasitic of passive components like inductors, transformers and capacitors. Finally, but not with less importance, the applied control strategy plays a definitive role in the overall efficiency of the whole conversion process. The strategy of Power Sink / Source Inverter (PSI) control shows improvement compared to Voltage Source Inverter (VSI) and Current Source Inverter (CSI) solutions widely used in three-phase systems.

State of the art

With more conversion steps in the applications - like EV battery charging - the total efficiency at full load is hardly reaching an overall efficiency of 95.5 %.

Typical distribution of losses in state of the art VSI PFC + LLC three-phase AC to the isolated DC converter for a EV charger using advanced SiC components (Figure 1) looks like 2.9 % semiconductor losses (97.1 % semiconductor efficiency) and 4.5 % total losses (95.5 % total efficiency) including the losses of passive components for the three conversions. (P=22.5 kW, ACin=400 V, DCout=450 V).

The analysis of losses in the three conversion stages of VSI PFC, LLC resonant inverter and LLC resonant rectifier shows that for higher efficiency both the conduction and switching losses of the VSI PFC and the conduction losses of the LLC stage need to be improved.

The major technical barrier against higher efficiency in PWM systems is the fact that a tradeoff must be made between conduction and switching performance of the used semiconductors, which will lead to a minimized loss at the optimal switching frequency only. However, with extra components and/or control efforts the tradeoff limits can be extended and the way for higher efficiencies can be widened.

Such examples are the single-phase totem pole PFC for low power supplies or the three-phase ANPC topologies for high-power high-voltage solar inverters, in which a mixture of semiconductor technologies allows single-stage switching power converters to reach or exceed the efficiency of 99 %.

AutoPFC and SRC in SRTE mode

The minimum configuration for three-phase AC to HF isolated DC conversion for an EV charger application should include a rectifier, an HF inverter and a HF rectifier. The simplest control is no control for the rectifier (called autoPFC) and a fix frequency control with 25% fix duty cycle for the SRC (Figure 2).

The frequency of the control is selected to be half of the self-resonance of the SRC, so that the converter is working in ZCS

PFC semiconductor losses	1.3% (0.75% conduction + 0.55% switching)
PFC passive losses	0.6%
LLC semiconductor losses	1.6% (1.3% conduction + 0.3% switching)
LLC passive losses	1%

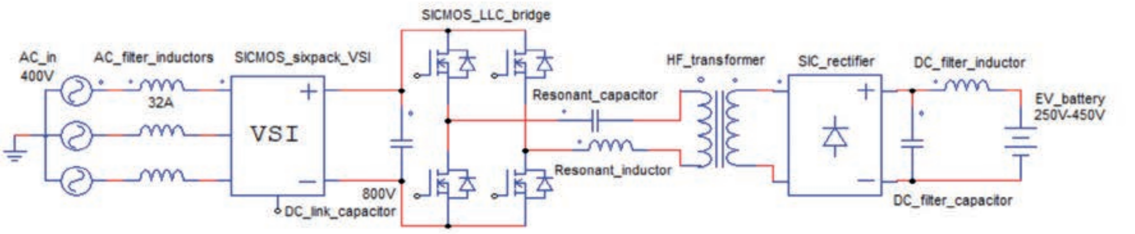


Figure 1: **VSI PFC + LLC SiCMOS EV charger and losses**

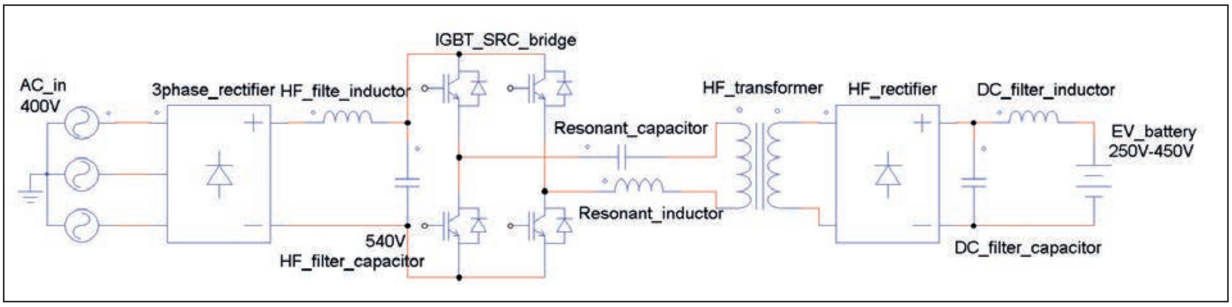


Figure 2: AutoPFC and fix frequency control

(mode SRTE). This allows the selection of low drop semiconductors for both the IGBT and the output rectifier. The input three-phase rectifier bridge is handling 50 Hz only, so also standard rectifiers with low drop can be used. The expected efficiency can be calculated from the losses.

As both the input rectifier and the SRC are free from hard-switching, the switching losses on the first estimation can be considered close to zero. Efficiency can be estimated by static losses.

The drop of rectifiers (1 V+1 V) while losses of the IGBTs (1.3 V+1.3 V) are to be related to the same 540 V DC average voltage on the HF filter capacitor. The drop of output HF rectifier (1.1 V+1.1 V) are to be related to battery voltage (450 V). Total losses: autoPFC (rectifier) semiconductor 0.37 %; autoPFC passive 0.2 %; SRC semiconductor 0.97%+ (0.48 % IGBT + 0.49 % HF rectifier); SRC passive losses 0.8 %.

The three conversion steps come to > 98.6 % semiconductor and > 97.6 % total efficiency. The SRC in fix frequency mode delivers an output current proportional to the input DC voltage.The three-phase mains rectified voltage has about 15% fluctuation, so the output PF will be close to 1.

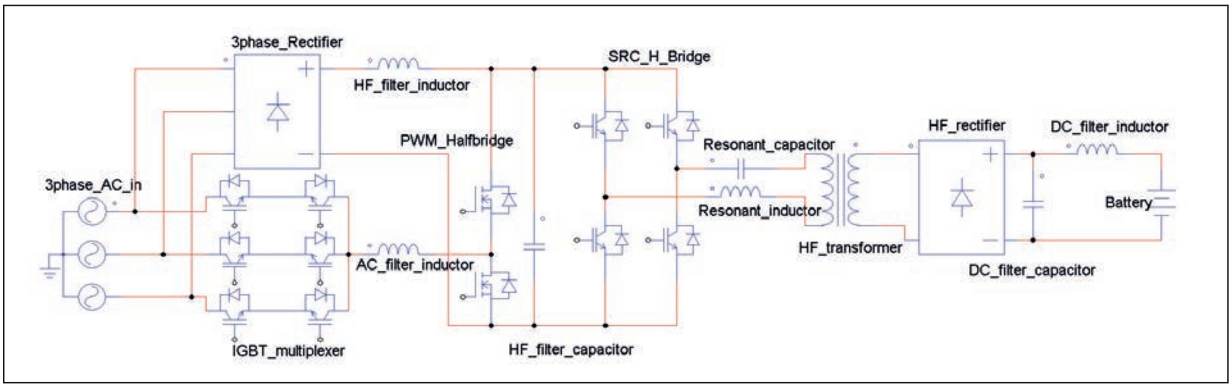
The input PF will be limited to about PF>0.95 due to the fact that the three-phase rectifier current can flow in two phases at a time only. This conforms to the PF>0.9 requirement of the standards, but it conforms to THD requirement only under specific conditions of the threephase net (IEC 61000-3-12).

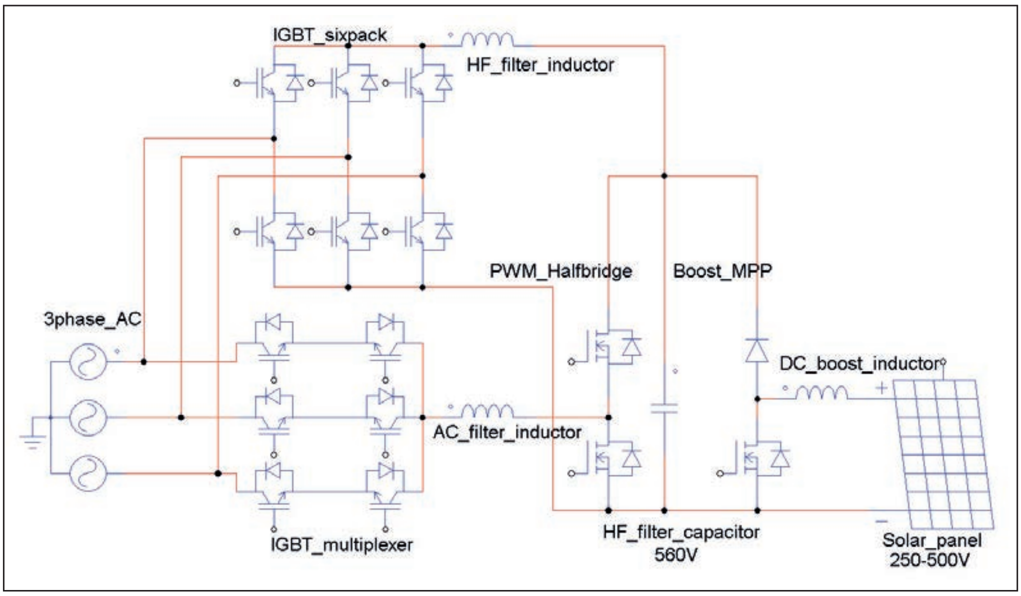
The system has no energy storage, but the HF ripple of SRC have to be filtered both towards the three-phase input and towards the battery.

If the frequency of the SRC is modulated inversely to the input voltage of the SRC (HF filter capacitor voltage), the current into the battery will be constant in time, so the constant power mode results PF=1 for the battery and PF>0.95 for the three-phase input.

CSPFC in EV charger and solar applications

The THD can be significantly improved by





ABOVE Figure 3: CSPFC + SRC

LEFT Figure 4: CSPFC + solar MPP

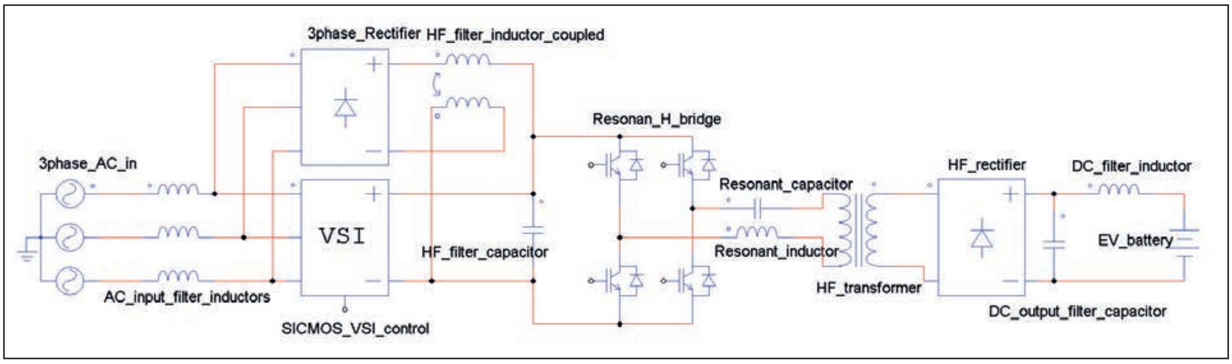


Figure 5: UHPFC + SRC

injecting a regulated current into at least one phase of the three phases. The idea is based on two laws of physics. The first is the Kirchhoff's law and the second is the law of conservation of energy.

According to Kirchhoff's law the sum of currents of the three-phase mains must be equal to zero in each moment. $I_1(t)+I_2(t)+I_3(t) = 0$ where I_1,I_2,I_3 are the phase currents of the three-phase system.

On the other hand according to the law of energy conservation, if there is no significant energy storage in the power converter, then the energy entering or leaving the three-phase AC must follow the energy leaving or entering on the DC side. For the battery charger:

$U_1(t)*I_1(t)+U_2(t)*I_2(t)+U_3(t)*I_3(t)=V_{BATT}*I_{BATT}(t)=P(t)=V_{BATT}*I_{BATT}=P$ where U_1, U_2, U_3 are the phase voltages of the three-phase system.

By controlling the output current so that it is constant in time, that is $I_{BATT}(t)=I_{BATT}$, the three-phase input power has to be also constant in time. So in case of a symmetric threephase network it is enough to control the current in one of the input phases at a time. The other two phase currents will follow for a symmetric load. This type of inverter is called Power Sink / Source Inverter (PSI).

There are several methods to select one from the three phase currents to control. The simplest control can be realized by a single PWM current controller, so that its current is multiplexed into the phase always with the smallest amplitude. The multiplexing is done at 50Hz repetition rate. The phase currents are synthesized from the controlled current by the half-bridge through the IGBT multiplexer and from the indirectly controlled currents of the rectifiers. The topology for EV charging results in a Current Synthesizing PFC (CSPFC) followed by an SRC controlled for constant power (Figure 3).

As the PWM control leg has only ? of the three-phase currents in amplitude and as the control per phase must be done in only 1/3 of the total time (2* -30 DEG to +30 DEG), the power to be handled by the half-bridge is only 1/6 of the total power through the converter, so the losses associated to the PWM stage are also only about 1/6 compared to traditional three-phase VSI inverter losses.

Total losses will come to 2.74 % (0.97 % PFC and 1.77 % SRC), that is, the expected power efficiency is about 97.26 % for the three conversion steps. Compared to autoPFC that has a poor THD on the AC side, even though the effort to reach PF=1 on both ports is relative high (8 additional gate control), the overall efficiency is only about 0.4 % lower.

It can be stated that the PWM current shaping and multiplexing stage is bidirectional, so if the direct power path through the rectifier is extended to a CSI type IGBT sixpack with LF switching, only then the power flow can be opposite as well. A typical solar energy regeneration system with a boost MPP can be seen on Figure 4. The MPP can be of any type of buck, boost or buck-boost hard-switched or resonant, but it must be controlled for constant power. This will ensure PF=1 on both AC and DC ports and close to 100 % MPP efficiency. Total power efficiency of the system will be about 99 %, as semiconductor efficiency will be dominated by the IGBT sixpack static efficiency and the MPP stage efficiency.

UHPFC in EV charger and solar applications

There is another option to inject the sine wave PWM control currents into the appropriate phases through a three-phase VSI inverter. In this solution a standard VSI sixpack (MOS1MOS6) is driving the current control signals into the three-phase utility. As discussed before the sixpack is sized for ⅙ times of the full power only. The rectifiers will take the majority of the currents at a very high efficiency, dominating the losses. This is for the name

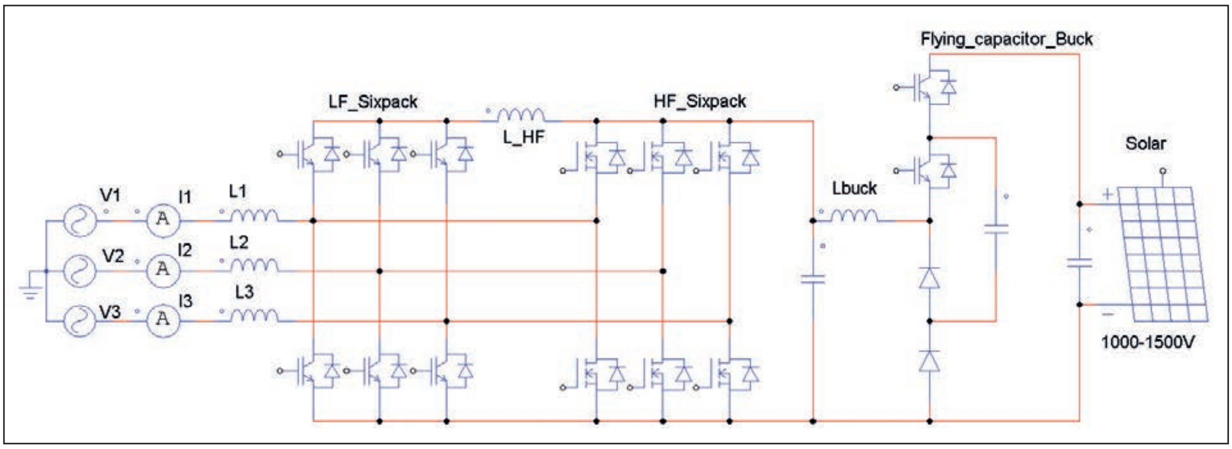


Figure 6: UHPFC in solar application

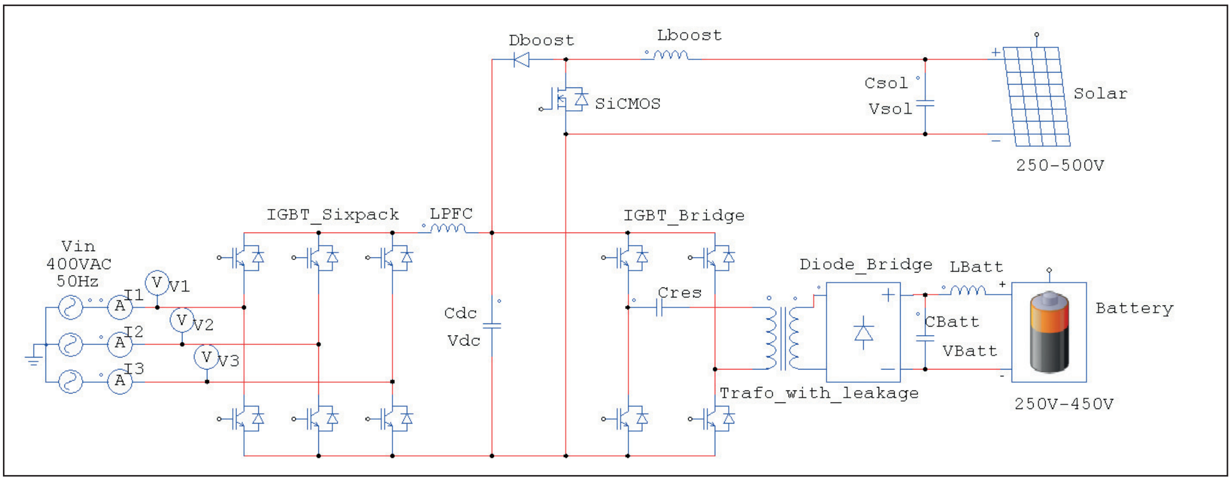


Figure 7: AutoPFC + solar + EV charger triport

of Ultra High Efficient PFC (UHPFC) as depicted in Figure 5.

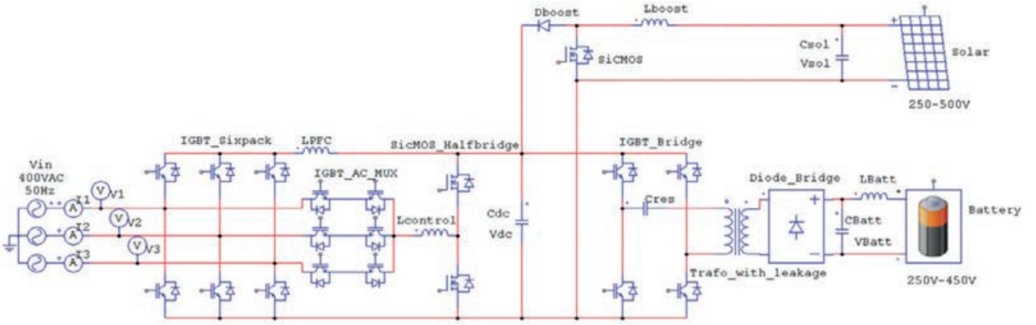
Because of the missing IGBT multiplexer the UHPFC will reach about 0.2 % higher efficiency (99.2 %) than CSPFC solution (99 %) and so it finally results in an overall efficiency of about 97.45 % for the three conversion steps of the UHPFC+SRC battery charger. The UHPFC can handle limited reactive power without significant distortion in the input currents. This can be an extra benefit for solar inverters without DC link energy storage capacitors.

The same way as CSPFC, the UHPFC can also be used for solar energy generation applications as shown on Figure 6. In this solution only one phase of the HF sixpack is operating at a time and only for the -30° to +30° and 150° to 210° parts of the sine-waves. Approximately ⅚ of the power passes through the LF Six-pack without chopping, thus, resulting in very high efficiency. The power sourcing feature is added by the Flying Capacitor Buck converter.

Three-phase autoPFC-solar-EV charger triport

Solar energy is often used for EV charging. For the best efficiency and the minimum cost the power conversion steps in this case should be kept at minimum. However, solar energy generation and EV charging require different control methodologies. Solar energy generation should be kept at Maximum Power Point (MPP) whenever solar energy is available. On the other hand EVs need electricity for charging in a controlled manner dependent on the state of the EV battery and independent from solar power availability.

It is evident to use the AC utility net for backup of the electrical energy to serve best for both needs. Symmetric three-



Distribution of losses:

Solar boost losses (boost switch, diode, inductor)		0.8 %
PFC rectifier semiconductor losses	$^5/_6$*0.37%=	0.31 %
PFC passive losses	$^5/_6$*0.2%=	0.17 %
IGBT sixpack semiconductor losses	$^5/_6$*0.48%=	0.4 %
IGBT multiplexer losses	$^1/_6$*1%=	0.17 %
PWM inverter losses	$^1/_6$*1.9%=	0.32 %
SRC semiconductor losses		0.97 %+ (0.48% IGBT + 0.49% HF rectifier)
SRC passive losses		0.8 %

Figure 8: CSPFC + solar + EV charger triport

phase net is preferred, as it is capable for sourcing or sinking constant power in time. However, DC/AC and AC/DC conversions are always less efficient than DC/DC conversions.

Furthermore, charging the EV battery and generating solar energy at the same time requires two conversion steps involving one DC/AC conversion for the energy flow from the solar panels to the three-phase net, and one AC/DC conversion for the energy flow from the three-phase net to the EV batteries. Direct DC/DC conversions should be used in this case.

The Power Source/Sink Triport of Figure 7 allows the optimum power flow at all conversion cases from the three-phase net to the EV battery (isolated AC>DC); from solar panels to the three-phase net (non-isolated DC>AC); and from solar panels to the EV battery (isolated DC>DC).

The three-phase net is used to sum up the powers of the sourcing solar panel and of the sinking EV battery charger on a virtual power junction of Vdc.

The bidirectional IGBT sixpack ensures that Vdc for low frequency is the difference of the most positive and most negative phase voltages independent from the direction of the power flow through it.

As the C_{dc} is of a low capacitance value (only for HF filtering of the solar boost output current the EV charger input current), it does not store significant energy. Therefore, the power sourcing/sinking of the net is equal to the difference of the power sourcing of the solar panel and power sinking of the EV battery charger.

Each of the power flows are set independently by their controllers (Solar MPP and EV Battery Charge). The power that have to be sunk by the three-phase net through the IGBT sixpack will be the maximal power of the solar source. The power that have to be sourced by the three-phase net will be the maximal power of the EV battery charger.

If the solar panel power is higher than the EV battery charging power necessity, then the Triport will transmit the difference of power to the three-phase net automatically. If the required EV battery charging power is higher than the solar panel power, then the triport will take the difference from the three-phase net automatically. The transition between sourcing and sinking is also automatic in both directions.

Solar-EV charger triport with bidirectional current synthesizing PFC

The THD on the three-phase line can be significantly improved by injecting a regulated current into at least one phase of the three phases. The power factor can be adjusted to unity (PF=1). As the injection of the PF=1 control current is bidirectional, the current injecting PWM halfbridge of Figure 3 is inherently suitable for both AC>DC and DC>AC power conversions. This Triport can be seen on Figure 8.

It has all the advantages as triport of Figure 7, but with undistorted sine-wave currents on the three-phase net for both directions of power flow. Total charging losses will come to 2.74 % (0.97 % PFC and 1.77 % SRC) resulting in 97.26 % efficiency. Total solar generation losses 1.86 % (0.8% booster and 1.06 % PFC) resulting in 98.14 % efficiency. However, if EV charging is needed when solar power is also present, then a DC/DC direct conversion with 2.57 % losses (0.8 % booster +1.77 % SRC) will improve the efficiency of triport to 97.43 % in respect of solar power utilized for battery charging.

MPPT IC Li-Ion Battery Charger System

In an era characterized by the internet of things (IoT), more connectivity means more outdoor devices are now battery-powered and constantly communicating. In particular, an increasing number of outdoor devices are being powered through solar panels. The charger should be suitable for maximum power point tracking (MPPT) in outdoor designs with a solar panel. This article illustrates design tips for a solar panel charger with a Lithium-ion battery, suitable for applications such as outdoor solar surveillance cameras or outdoor lighting. **Alex Jiang, Senior Technical Marketing Engineer, Monolithic Power Systems, San José, USA**

This reference design is developed based on the MP2731 IC from MPS with an MC96F1206 controller (a low-cost 8051 MCU). It is suitable for small and medium solar-powered charging solutions. Compared to a conventional MPPT system, the MP2731-based system integrates a VIN connection switch, ADC, and voltage/current-sensing circuitry, which significantly reduces the system cost. The system design uses the perturb-and-observe (P&O) algorithm for MPPT to achieve 98 % or greater tracking accuracy.

Features of the MP2731 include up to 93 % efficiency in a 9 V input 5 W system, 98 % MPPT accuracy, a small 25 mm x 25 mm core circuit area, fully integrated power switches with built-in robust charging protection including JEITA and programmable safety timer, and an I?C interface for flexible system parameter setting and status reporting (see Figure 1).

MPPT theory and implementation

The output power from a solar panel is determined by several factors: the irradiance level, the operating voltage and current of the panel, and the load. There exists a maximum power point where solar panel is outputting optimal power to the system (see Figure 2). Maximum power point tracking techniques like P&O or incremental conductance methods are used to actively keep the solar panels operating at MPPT during changing irradiance conditions.

In the power-based P&O MPPT algorithm, the derivative of power to voltage dP/dV of a PV panel is used as a tracking parameter. Calculate when MPP is reached using Equation (1):

$$\frac{dP_{\text{in}}}{dV_{\text{in}}} = 0 \qquad (1)$$

A DC/DC converter is generally used to ensure MPP optimization inside the system. A highly integrated switching charger - the MP2731 from MPS in this reference design (Figure 3) - is connected between the PV panel and battery load.

A reverse-blocking FET Q1 is used to block the path from the battery load to the PV panel when the panel is under low irradiance. The input voltage/current and output voltage/current of the IC are sampled through an 8-bit ADC. The IC

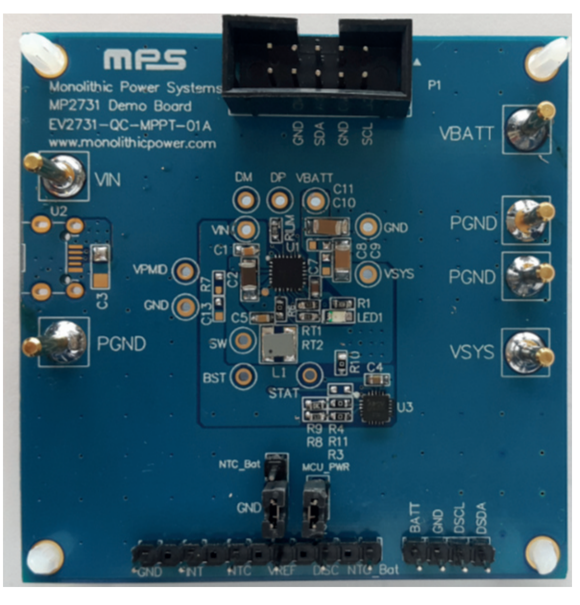


Figure 1: PCB of the MPPT control system

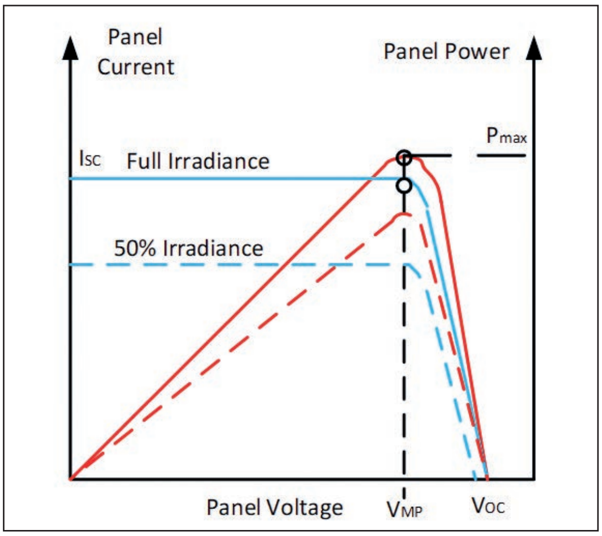


Figure 2: Solar panel P-V and I-V curve

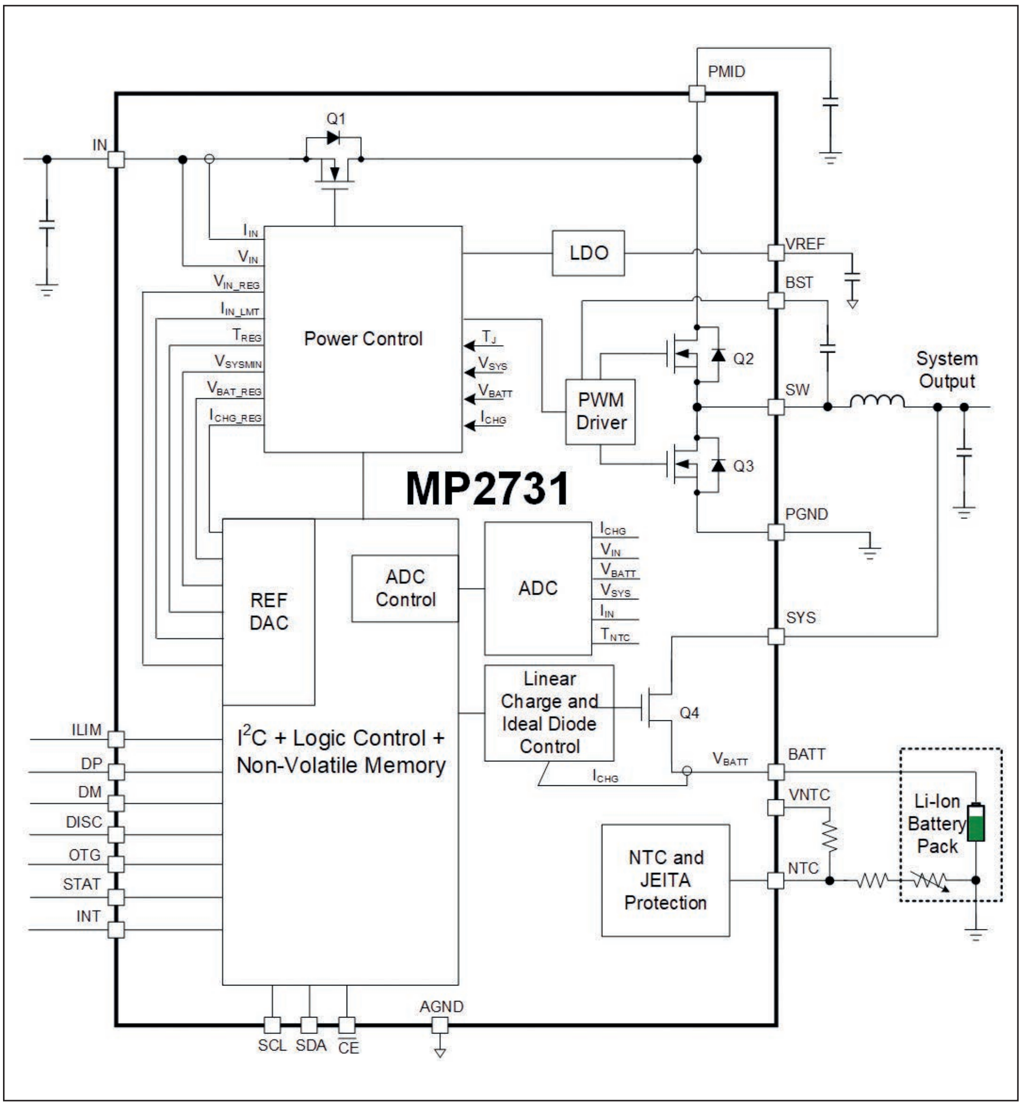


Figure 3: Functional block diagram for the MP2731

supports I?C communication, so the digitized current and voltage information can be easily communicated to the external MCU.

The P&O MPPT algorithm is implemented in a 20-pin, 8-bit MC96F1206 MCU from ABOV Semiconductor. To communicate with the MP2731, the I?C peripherals in the MCU are activated.

Figure 4 shows the system-level software flow. The MCU is in sleep mode when VIN drops below the under-voltage threshold. When VIN recovers, it sends an interrupt (INT) to wake the MCU. Then the MCU reads the MP2731 registers and initiates those registers.

By setting the input current limit to its maximum value, the panel voltage is controlled only by the input voltage limit loop. By adjusting the input voltage limit loop reference, the PV panel's voltage can be adjusted. After initializing the MP2731, read the ADC initial value, then enable charging.

Check if VIN_STAT is equal to 1. If it is not equal to 1, increase VIN_REG by one unit, and then go back to the previous value for VIN_STAT. When VIN_REG reaches its maximum limit, VIN_STAT is still not equal to 1. The charging current gradually decreases, and returns to the previous value set by VIN_STAT. When VIN_REG set has reached its limit, the ICC is set to a minimum. If VIN_STAT is still not equal to 1, the MCU enters sleep mode, and the MP2731's charging functionality is disabled until the INT interrupt function wakes the MCU.

In case the PV panel is partially covered and a local MPP can be tracked using a conventional P&O MPPT algorithm, the MCU initiates an scan every time the input voltage flag changes. The MCU adjusts the input regulation voltage reference of the MP2731 with a 100 mV step from 50 % of the panel open-circuit voltage (VOC) to 80 % VOC to scan the optimum power point. After the initial scan, the PV panel is set to operate at the maximum power point. To continue tracking the optimum point under varying load and irradiance conditions, the P&O algorithm runs in every 256 ms on the MCU (see Figure 5).

Experiment results

Figure 6 shows the MPPT process for a PV panel with (8 V, 500 mA) MPP. Before t0, with no load, the PV panel outputs 12V at open-circuit voltage. After the MP2731 IC and MCU power up, the PV panel runs at the preset 6 V input voltage, configured by the MCU. From t0 to t2, the MCU scans for MPP.

At t1, the MPP is located but the scan algorithm keeps sweeping the input voltage until the power falls to 85 % of the recorded peak power at t2. After t2, the MCU sets the panel voltage to the scanned peak power voltage, then activates the real-time P&O algorithm.

Figure 7 shows the complete charging behavior for a Lithium-ion battery. From t0

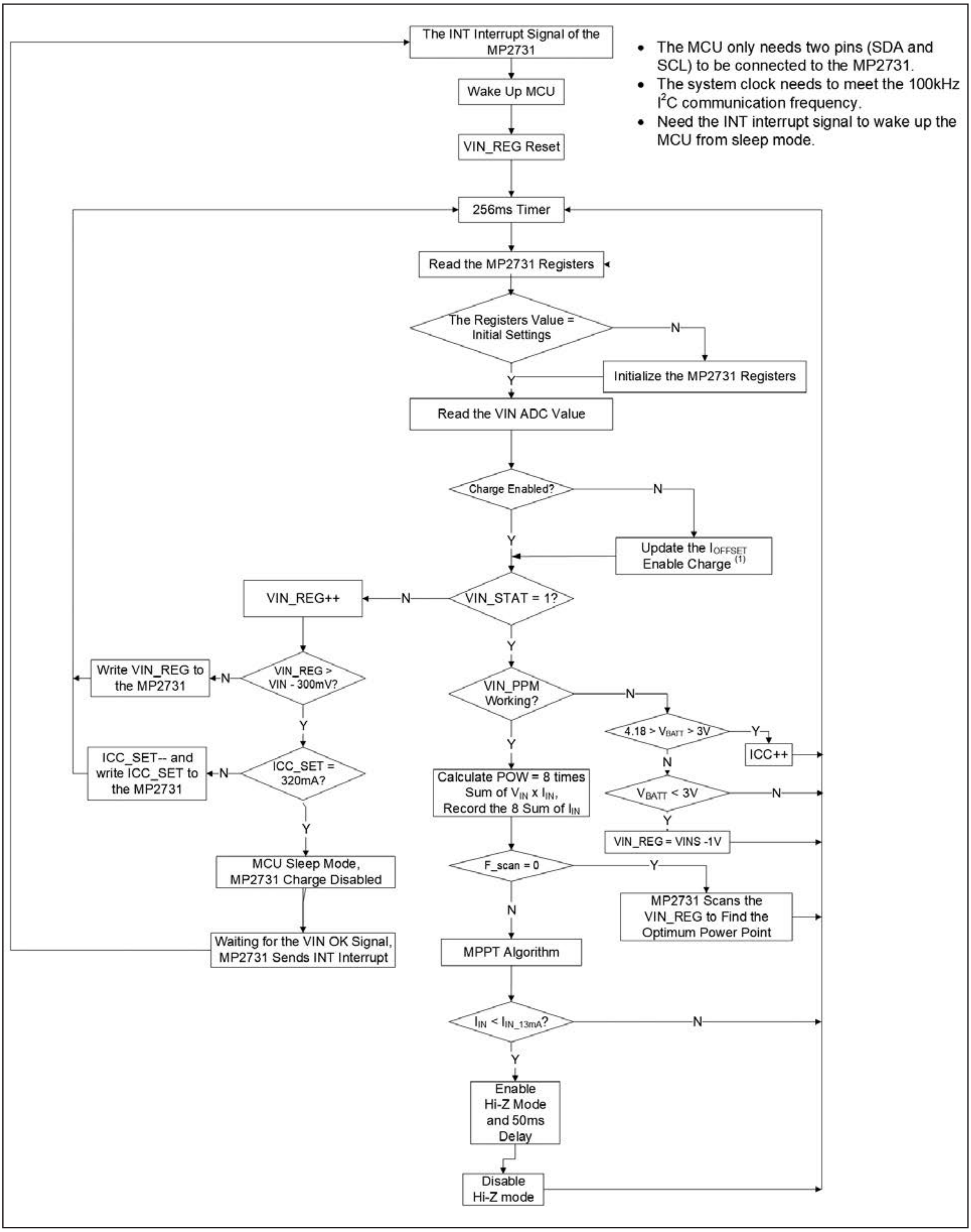


Figure 4: System-level software flowchart

to t1, the system powers up and scans MPP. From t1 to t2, the battery goes through the CC and CV stages as the battery charge current changes from constant current to lower values. When the battery is close to fully charged, the PV panel voltage starts ramping up to the open-panel voltage again. There is a light-load condition because the battery consumes a lower load current when fully charged.

With low-resistance, integrated MOSFETs, the MP2731-based MPPT system also achieves high efficiency above 95 % under various conditions.

Conclusion

The MP2731 lithium-ion battery charger IC effectively reduces the cost for outdoor IoT systems by eliminating discrete voltage and current-sensing circuitry from the BOM. Highly integrated low RDS(ON) allows for a high-efficiency system with a compact PCB area. Future product development projections include accommodating design in higher power, higher voltage applications, further reduction in system quiescent power consumption, and developing solutions for multi-panel systems.

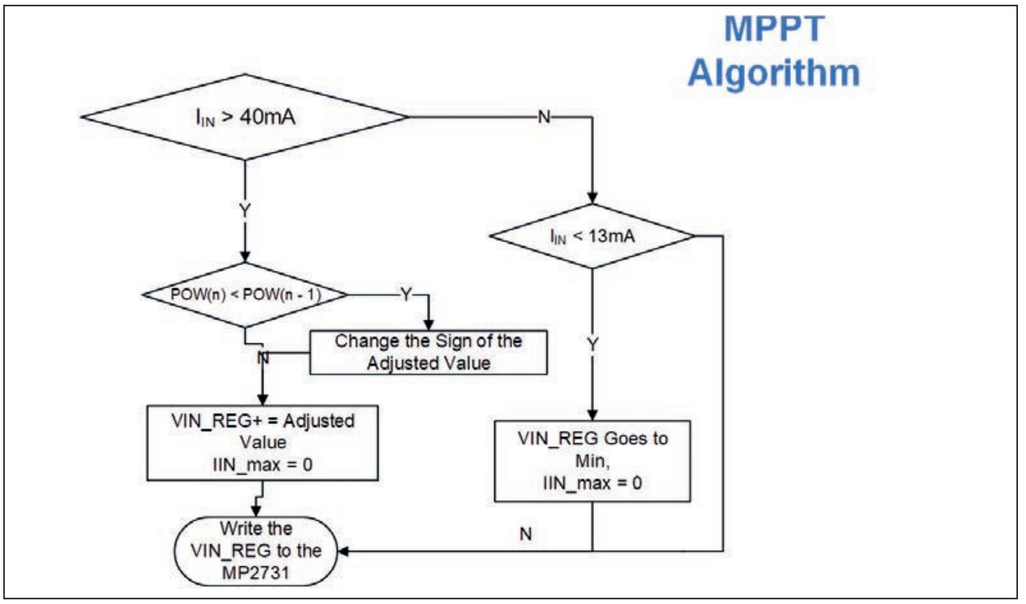


Figure 5: P&O MPPT algorithm

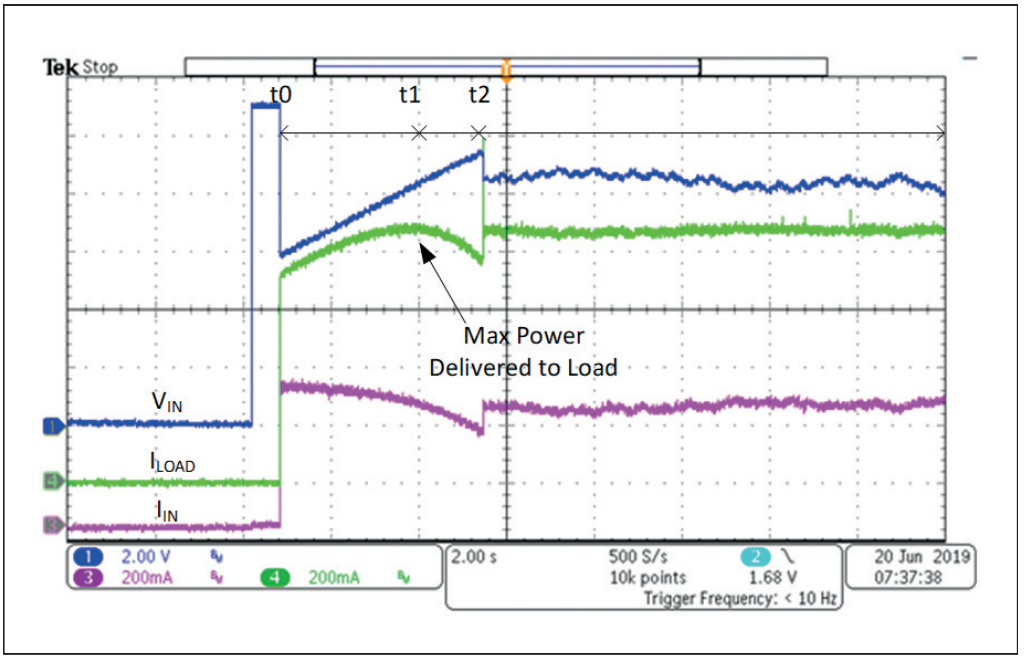


Figure 6: MPPT process for PV panel from power-up to steady state

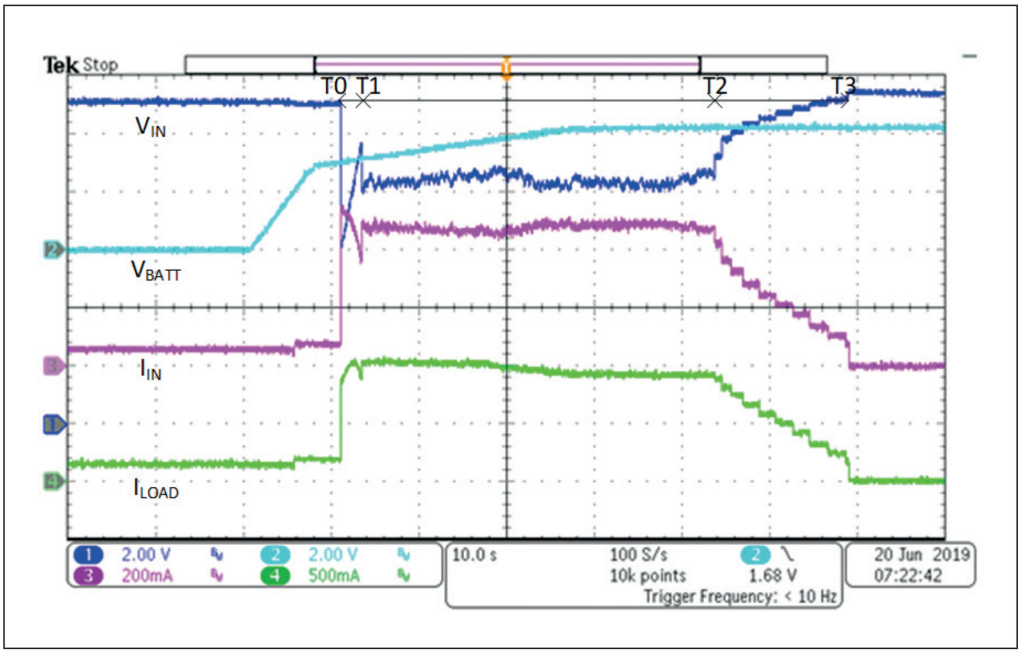


Figure 7: MPPT behavior during charging cycle

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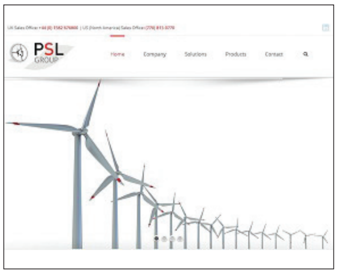

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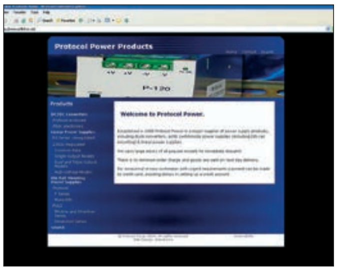

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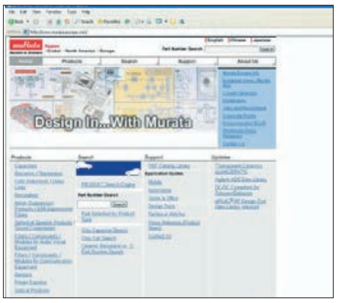

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