POWER ELECTRONICS EUROPE

ISSUE 1 – JANUARY/FEBRUARY 2010

AUTOMOTIVE POWER Improvement of New Automotive Power

Semiconductor Packages



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ONICS
GY-----Opinion | Market News | Events | Energy Harvesting |
Renewable Power | Battery Monitoring | Power Modules |
Power Diodes | Website Locator

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PAGE 6

Market News

PEE looks at the latest Market News and company developments

PAGE 14

Events

The Applied Power Electronics Conference and Exposition (APEC) celebrates its 25th anniversary from February 21 - 25 in Palm Springs (California/USA).

CIPS stands for the 6th International Conference on Power Electronics Systems Integration. It will be held from March 16 to 18 at Nuremberg's Maritim Hotel.

The power electronics sector is further growing. Additionally, the overall economic climate brightens up. This positive trend can be recognised at PCIM Europe 2010. From May 4 - 6 this year.

COVER STORY



Power Density and Performance Improvement of New Automotive Power Semiconductor Packages

Steadily but surely automobile manufacturers are looking to design out the engine-driven auxiliary loads such as fuel, water, brake and power steering pumps with electric driven ones. Here MOSFETs are the devices of choice to power such applications. The ability to drive more current through a smaller space, at higher efficiency and increase power density is going to become of greater importance as the electrification of the automobile unfolds. The replacement of fuel tanks and spark plugs of the past with batteries, IGBTs and MOSFETs of today will not happen by default. The new power electronic drive trains will not noly have to meet but exceed the performance of the traditional internal combustion engine powered solution. With such demanding goals the use of next generation power semiconductor power packages which interfere less with the operation of the semiconductor will be key to ensure next generation efficiency, power density and performance goals are met. With Automotive DirectFET 2, the lead frame, wire bonding and molding are eliminated all together leading to further performance and reliability improvements. Full story on page 20

Cover supplied by International Rectifie

PAGE 24

Energy Harvesting Gets a Boost

A wide range of low-power industrial sensors and controllers are turning to alternative sources of energy as the primary or supplemental means of supplying power. Ideally, such harvested energy will eliminate the need for wired power or batteries altogether. Although energy harvesting has been emerging since early 2000 (its embryonic phase), recent technology developments have pushed it to the point of commercial viability. In short, in 2010 we are poised for its "growth" phase. Building automation sensor applications utilising energy harvesting techniques have already been deployed in Europe, illustrating that the growth stage may have already begun. **Tony Armstrong, Director of Power Product Marketing, Linear Technology, USA**

PAGE 28

Design Concept for a Transformerless Solar Inverter

Vincotech is able to offer a wide spectrum of power modules for solar applications. For transformer-less single phase solar inverter the power module FZ06BIA045FH-P897E is able to carry a output power of 6kW but for efficiency optimisation a nominal power of 3kW is recommended. **Michael Frisch and Temesi Ernö, Vincotech Germany and Hungary**

AGE 31

Monitoring Batteries Improves UPS Reliability

Systems from mobile telecommunications to data centres must operate with minimal downtime, making the reliability of the electrical mains supply a key concern. Uninterruptable power supplies (UPSs), which provide back-up power in the event of mains failure, are therefore widely used to ensure critical electronic systems continue to function normally in the event that the mains power goes down. Sentinel III; a set of components for a battery monitoring addresses the needs of UPS OEMs and battery providers. These components are used to create a simple to install and intuitive solution for continuous battery monitoring within mission critical installations. **Loic Moreau, LEM SA, Geneva, Switzerland**

PAGE 34

Thermal Behaviour of Three-Level Trench Gate IGBT Modules in PFC and PV Operation

The control of the power semiconductors in a three-level NPC topology employs a set of 12 control signals in total. A back-to-back two-level/three-level inverter has been built to circulate power performing arbitrary load conditions to analyse the thermal dissipation of the power semiconductors. This thermal analysis utilises an IR camera to perform an in-situ measurement and allows precise modelling of thermal and electrical parameters. Once this experimental platform has been calibrated, the loss on each semiconductor chip can be acquired and compared with the simulated results. Hence, tuning of the model parameters becomes possible. **Marco Honsberg and Thomas Radke, Mitsubishi Electric Europe, Germany**

PAGE 38

Intelligent Doping Leads to Success

Switched power supplies are everywhere today; it is the only technology capable of delivering high efficiency. Power factor correction supposedly can keep sine wave distortion and noise low in the power grid, but also creates additional power losses. New, specially designed Silicon diodes can reduce the costs for such circuitry easily. **Wolf-Dieter Roth, HY-LINE Power Components, Unterhaching, Germany**

PAGE 41

Website Product Locator

Power Electronics Europe





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Since the early 1980's research has been ongoing into the possibility of using Gallium Arsenide (GaAs) as an efficient semiconductor material to make power rectifiers. The potential attractions of using GaAs to make power rectifiers are derived primarily from several attractive factors in its atomic makeup. Having a combination of very high electron mobility and high relative dielectric constant value shows potential for less internal resistance and energy dissipation whilst also offering higher breakdown voltages. This also leads to a product which naturally has a high temperature capability whilst demonstrating a high level of immunity compared to the characteristic degradations observed in Silicon rectifiers as temperature increases. Historically the roadblock to realising these potential advantages has been the inability to increase voltages to levels useful in today's power market such as the need for higher DC-link voltage. Directly associated with this were the difficulties in creating a controlled capable fab process within a viable cost model.

Liquid Phase Epitaxy overcomes these issues with the fab process which resulted in lower maximum breakdown voltages and varying yields. The result is a stable and economically viable process which makes GaAs high voltage diodes a possibility for use in new mainstream power applications today. In terms of enabling the technology as an economic viability the technology developed for growing epitaxial structures is original, simple and relatively inexpensive in contrast with techniques employed for Silicon Carbide (SiC) or Gallium Nitride (GaN) wafer manufacture. LPE technology uses conventional furnaces and due to this is easily scalable with high production capabilities. The process of making diode mesa structures wafers also uses conventional methods of manufacture. Newly developed highvoltage GaAs diodes (over 1200V/150A) show that at higher junction temperature forward voltage is lower as compared to SiC Schottky diodes or power ultrafast recovery Si diodes.

Since the advent of commercially viable Si power FETs, introduced some 30 years ago, enabled the widespread adoption of switch-mode power supplies, replacing the linear

Momentum for Gallium in Power Semiconductors

regulator as the dominant power architecture, the Si power FET has become the dominant power device. The Si IGBT, combining the ease of charge control with the benefits of conductivity modulated drift resistivity, has been another mainstay, especially in the lower frequency conversion systems, e.g. motor drive inverters. Of course, the same minority carrier injection that provides for lower ohmic losses also increases switching losses through the effects of subsequent tail currents. Over the last 3 decades significant engineering efforts have driven the improvement in the performance figure of merit (FOM) of these devices by more than an order of magnitude. However, as this technology approaches maturity, it becomes increasingly expensive to achieve even modest improvements in the device FOM.

GaN on Silicon also gains more attention since International Rectifier has launched a product roadmap in 2008. GaN based power devices already provide a factor of 2 to 10 in specific onresistance improvement over state-of-the-art silicon based devices, especially for unipolar, non-compensated devices. GaN devices represent very early stage devices as was the case in silicon power device development over the last 30 years. Even though the basic GaN HEMT transistor was invented some 15 years ago, significant development efforts on practical power devices using GaN-on-Si technology have been fairly recent, predominantly in the past 5 - 7 years. GaN based power devices are expected to improve rapidly over the next 10 years.

Recently Belgium-based research center Imec presented an innovative GaN-on-Si double heterostructure FET architecture for GaN-on-Si power switching devices. The architecture meets the normally-off requirements of power switching circuits and is characterised by low leakage and high breakdown voltage, both essential parameters to reduce the power loss of high-power switching applications. Imec obtained a high-breakdown voltage of almost 1000V combined with low on-resistance by growing an SiN/AlGaN/GaN/AlGaN double heterostructure FET structure on a Si substrate. Within its industrial affiliation program on GaN-on-Si technology, Imec and its partners (i.e. National Semiconductor) focus on the development of GaN technology for both power conversion and solid state lighting applications. An important goal of the program is to lower GaN technology cost by using large-diameter GaN-on-Si wafers and hence by leveraging on the scale of economics. Imec invites both integrated device manufacturers and compound semiconductor industry to join the program and to benefit from sharing of cost, risk and talent.

Read more on the following pages!

Achim Scharf PEE Editor

Isabellenhütte and Wiedemann Cooperate in HEVs

The German companies Sensor-Technik Wiedemann and Isabellenhütte have joined forces to develop a battery management solution for utility vehicles featuring hybrid drive technology. The two firms have now signed a cooperation agreement that will pave the way for further joint efforts in development and production of key components for electric drives.

The current trend in hybrid drive technology is the focus on efficient electrical energy storage systems. An increasingly important energy storage system is the Lithium-ion battery, which boasts high energy density coupled with high power density. "For a Lithium-ion battery to work efficiently, a well functioning battery management system with precision voltage and current sensors is needed. By joining forces with Isabellenhütte, we are now working with one of the key leaders in the field of automotive current measurement. The joint development work will open up new possibilities for us", comments Wolfgang Wiedemann, CEO of Sensor-Technik Wiedemann, who also took over as Chair of the AMA Association for Sensor Technology in mid 2009. The company has many years of experience in the development of battery management systems for automobiles, i.e. a host of utility vehicles such as compact delivery vans, small-sized lorries and buses have been fitted with hybrid drives and Lithium-ion batteries.

Isabellenhütte was the first company to achieve the ultraprecise measurement of current, voltage and temperature in automobiles using its ISA-ASIC sensor. The battery management system is based on a sensor module that is able to measure a minimum voltage drop across a shunt in the busbar of the traction network. "Our sensor modules are 100% configurable to the user's individual needs. Thanks to cooperation with Wiedemann in the early product development phases, we were able to fully exploit this advantage", adds Felix Heusler, member of Isabellenhütte's management board.



"Our sensor modules are 100% configurable to the user's individual battery management needs", said Isabellenhütte's Felix Heusler

www.isabellenhuette.de

Breakthrough in Li-ion Battery Technology

Nexeon - a company formed following a breakthrough discovery made at Imperial College London - has revealed its plans to commercialise Lithium-ion battery technology, a development which will lead to batteries with significantly higher energy density and longer lifetime between charges. Longer operating times and brighter screens for laptops and smart phones, and cordless tools with more power on tap are just some of the benefits expected.

Lithium-ion batteries have come to dominate the rechargeable batteries market as a result of their higher performance for a given cell size and weight, their low selfdischarge rate and the absence of a 'memory effect'. Silicon has been known to offer potential as a superior anode material, but until now, it has suffered from physical instability when repeatedly charged and discharged. Nexeon's approach solves this problem by changing the physical form ('morphology') of the silicon, allowing it to realise its full potential as a battery anode. The use of Silicon anodes instead of the Carbon-based anodes allows greater charge to be stored within the battery. Silicon provides far higher

performance as an anode material, offering charge densities around ten times that of carbon.

Many potential applications for this technology exist, from consumer electronic products to medical devices and power tools. From an environmental viewpoint, increased use of rechargeable Lithium-ion batteries is preferred over their single-use equivalents. One of the highest profile applications has to be electric vehicles, where a high capacity and power to weight ratio is critical. Batteries made by using silicon anode material would deliver these benefits and allow

increases in vehicle range between charges.

Nexeon is based in Oxfordshire, and has a fully automated and instrumented pilot plant. The pilot plant closely represents a commercial manufacturing facility, and allows an accurate understanding of the processes and costs associated with making anode materials. The technology has been conceived with a 'drop in' approach, requiring the minimum of changes to an existing Li-ion battery manufacturing operation.

www.nexeon.co.uk

LED Lighting will Expand

Multiple retailers around the world are actively promoting LED lights for indoor and outdoor decorative illumination applications. Meanwhile, LED lights with the Edison sockets used for replacing conventional light bulbs are starting to appear on the shelves of many of these same stores, making them a viable choice for general illumination applications.

"The LED industry is on the threshold of a new expansion phase, a phase that will be characterised by growth rates in the high double digits during the next three years", said iSuppli analyst. "This growth will be driven by the increased adoption of high brightness and high flux, also referred to as high power or ultra high brightness LEDs into a new range of next-generation lighting applications".

Global LED revenue will expand by 11% percent in 2009 to reach \$7.4 billion, up from \$6.7 billion in 2008. This comes in stark contrast to the overall semiconductor market, which is expected to contract by more than 12% in 2009 because of the slowdown in the global economy. By 2013, the global LED market will reach \$14 billion, nearly



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Ideal for noise-sensitive applications, the LMZ series of power modules provide excellent radiated EMI performance and comply with CISPR22 Class B radiated emissions standards.

Superior Thermal Performance

Thermal performance with no airflow required, combined with low operating temperature and low system heat generation, make the power modules reliable and robust. Efficient heat dissipation technology eliminates the need for external heat sinks or fans that can add complexity and cost.



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national.com/switcher



double from 2009.

Beyond general illumination, this growth is being driven by the rising

penetration of LEDs as the lighting source of choice for a myriad of existing lighting applications, including automotive, traffic and street lighting, the backlighting of small LCD displays and keypads in

Fairchild Supplies LED Drivers to Osram

Fairchild Semiconductor has been selected by one of the world's largest lighting manufacturers, Osram, to supply LED driver solutions. The FSEZ1016A was developed by Fairchild to meet and exceed the stringent performance benchmarks set by Osram.

Lighting applications consume nearly 22 percent of electrical energy generated worldwide. Reducing wasted energy in these applications can have a significant impact on energy conservation. As the industry moves from standard incandescent light bulbs to CFL, LFL and LED lighting, a 75% energy saving can be realised. Fairchild provides solutions for all lighting applications including linear fluorescent ballast, compact fluorescent ballast, LED and HID. The company's portfolio ranges from discrete to integrated solutions that contain PFC controllers, ballast control ICs, high voltage gate drivers and MOSFETs. Fairchild's FSEZ1016A fits 1W-4W LED products. OSRAM is also considering deploying FAN6300 LED driver for its 12W to 60W products. The new FSEZ1016A and FAN6300 are designed for lighting manufacturers seeking energyefficient LED driver solutions. "We worked closely with Osram's engineers, based at the LED R&D facilities in China, and frequently discussed the technical details in our efforts", said Benjamin Tan, Fairchild's regional vice president of sales, China and South East Asia. "We look forward to continuing our strategic partnership with Osram

and to assisting them with developing and supplying further innovative devices that benefit consumers as well as the environment".

Osram also announced that In the new version of the Audi A8 Osram's LEDs are responsible for the dipped and full beams as well as for other specific lighting functions. Apart from their efficiency, an excellent argument for LEDs is their long life, which exceeds that of the vehicle. "LEDs have left the niche market of limited edition and luxury vehicles and have arrived successfully in volume production. As they already meet all the requirements of modern car lighting and set new standards in many respects,

LEDs are perfectly suited to mass market use" says Peter Knittl, LED automotive director at Osram Opto Semiconductors. The Ostar headlamp LEDs fitted in the A8 illuminate the road surface with

perfect definition, without glare, and they produce a light similar to daylight, which enhances perceptions of contrast. In the peripheral field of vision especially, i.e. where pedestrians, animals or poorly lit vehicles may suddenly appear at night, it is easier to recognise objects with white LED light. But even potholes, obstructions and worn road markings are much more visible. Another benefit is that the colour temperature is close to that of sunlight, so a driver's eyes will not tire so quickly. Essentially, this technology has the potential to prevent numerous accidents caused at night.

The Ostar headlamp is available as a new product platform with up to five LED chips. Typical light values achieved for each LED chip are 160lm at 700mA. Depending on the variant and operating current, values between 125lm and 1100lm are achievable. With its scalable brightness, the Ostar headlamp is suited to all headlamp functions such as full and dipped beams, cornering lights, fog-lamps and even for use in daytime running lights.

iSuppli's forecast for the worldwide

high-power through-hole, SMD and

navigation devices, digital picture frames and cameras. The market

emergence of new applications,

of large-sized LCDs in televisions, notebooks and computer monitors and personal illumination.

mobile handsets, personal

also is being aided by the

such as backlighting

www.isuppli.com

display LED lamps

market for standard-brightness, HB and

Headlamps are evolving from a mechanical type of component to an electronic module, which can operate linked to the vehicle's electronic system. For a glare-free full beam, data from the navigation system and information from a light-based driver assistance system are combined. Thus, the lighting system can by itself illuminate only the required parts of the road when cornering or in oncoming traffic. LED arrays play a particular role here in future - depending on the lighting function, individual LED pixels can be switched on or off, which enables light to adjust perfectly to various conditions.

www.fairchildsemi.com www.osram-os.com



LED headlamps at night - OSRAM LEDs take on all the headlamp functions in the new Audi A8 Photo: AUDI AG

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Sharp and STMicroelectronics Sign Agreement for PV-Panel Manufacturing Plant

Enel Green Power, Sharp and STMicroelectronics signed in January an agreement for the manufacture of triple-junction thin-film photovoltaic panels in Italy. Also Enel Green Power and Sharp signed a further agreement to jointly develop solar farms.

This agreement marks the first time that three global technology and industrial powerhouses have joined together in an equal partnership to contribute their value-add to the solar industry. Sharp's exclusive triplejunction thin-film technology will be operational in the mother plant in Sakai (Japan) as of spring 2010. STMicroelectronics' factory, located in Catania in the existing M6 facility, is expected to have an initial production capacity of 160MW per year. The plant's capacity is targeted to be gradually increased to 480MW per year over the next years and right from its start will represent the single most important production facility for solar panels in Italy. Photovoltaic panel manufacturing at the Catania plant is expected to start at the beginning of 2011. The factory output will be used to serve the most attractive solar markets in the EMEA region with a particular focus on the Mediterranean area. In this region, Enel Green Power and Sharp already have important sales networks and also plan to jointly develop solar farms. The project of 160MW will require a total investment of Euro 320 million and will be funded by a combination of equity, state grants and project financing.

www.st.com

New Automotive MOSFETs

International Rectifier introduced on January 21 the automotive DirectFET(r)2 power MOSFETs that deliver exceptional power density, dual-sided cooling and low parasitic inductance and resistance in a robust, reliable and AEC-Q101 qualified package for automotive applications.

"The AUIRF7739L2 and the AUIRF7665S2 combine the outstanding reliability and performance of the proven DirectFET packaging technology with IR's latest trench silicon process. The new DirectFET2 devices may be optimised by application for nextgeneration vehicle platforms for ultra-low on-state resistance, gate charge or logic level operation to deliver improved performance and efficiency, and reduced system size and part count," said Benjamin Jackson, IR's Automotive product manager. The AUIRF7665S2 small

can device is optimised for very low gate charge and exhibits extremely low parasitics for fast and efficient switching performance. The DirectFET2 MOSFET is ideal for automotive switching applications including the output stage of Class D Audio amplifiers as well as DC-DC converters and fuel injection systems (see our cover story for more details). Pricing for the AUIRF7739L2 and the AUIRF7665S2 begins at \$2.60 each and \$0.46 each respectively in low volume quantities.

In December 2009 the company has received a Master Performance award from EADS Astrium in recognition of their high reliability DC/DC converters. "IR was chosen for the Master Performance award because of the company's ability to achieve and maintain stringent end to end process requirements necessary to meet the specific demands of space satellite



applications", commented Steve Osborne, Repeater Module Electronics Commodity Manager, EADS Astrium Satellites. IR's Santa Clara (California) facility is DSCC certified class K to design and manufacture ruggedised hybrid DC/DC converters. The group is supported by a design center in Skovlunde (Denmark) for spacecraft power system designs and complex power conversion system solutions, and a silicon design center in El Segundo (California).

www.irf.com

National Enters Power Module Market

With the Power Modules for Switch Mode Power Supplies within the Simple Switcher Family National Semiconductor enters a new market segment.

So-called Simple Switchers are on the market since more than 20 years, the first regulator was already introduces in 1989, followed by the first synchronous regulator in 2005 and the 5th generation in 2008. "Over the years we have gained a base of 25,000 customers for this product family, which is more used in industrial applications and here open-frame or IC-like modules are not so convenient for the designer", said Michael White, VP of National's Performance Power Product line.

"That's why we are now introducing our new power modules capable of input voltages between 3.3V and 24V with output currents up to 5A and efficiency levels of more than 90% due to our low on-resistance power MOSFETs in the output stage. Thus the power modules provide the efficiency of a synchronous switching regulator with the simplicity of a linear regulator, eliminating the external inductor and complex layout placement challenges typical of switching regulator designs".

The LMZ power modules simplify power supply design for fieldprogrammable gate arrays (FPGAs), microprocessors, digital signal processors (DSPs) and other point of load (POL) conversions for medical, broadcast video, communications, industrial and military applications. Its patent-pending packaging technology provides low radiated electromagnetic interference (EMI) to meet the requirements of the EN55022 (CISPR22) Class B radiated emission standard. The latter is due to shielded internal



inductors and the conservative switching frequency below 1MHz. Efficient heat dissipation (thermal package resistance 20K/W) is due to large exposed-bottom pad allowing operation in high-ambient temperatures without the need for forced airflow (operating temperature -40°C to 125°C). The bottom pad allows also for prototyping on lab benches, eliminating the possibility of nonvisual solder bridging. The size and lead pitch enable the use of the same pick-and-place manufacturing employed with standard TO-263 packages. Each module is pin-to-pin compatible with other family members, allowing designers to create one layout to facilitate lastminute drop-in replacements if load current requirements change.

The LMZ10504 supports maximum load currents of 4A with an input voltage range of 2.95V to 5.5V; the LMZ12003 supports maximum load currents of 3A with an input voltage range of 4.5V to 20V; and the LMZ14203 supports maximum load currents of 3A with an input voltage range of 6V to 42V. The LMZ10504 is priced at \$7.10 each, the LMZ12003 is \$7.25 each, and the LMZ14203 is \$9.50 each in 500-unit quantities.

Easy design via Webench

Along with these power modules the company has introduced the Webench Power Architect for multioutput DC/DC power supplies, an extension of the recent launched Webench Visualizer (see PEE 8/2009, page 8). "Power Architect is the next step after Visualizer targeted from agile designs toward agile systems. For that we have stored more than 20,000 components from 110 manufacturers including inductors and other passive components. We supply only 300 components, included here are the power MOSFETs", explained Phil Gibson, National's VP Technical Sales Tools. "Depending on the tool's optimiser dial setting, a typical system with eight power loads will have a bill of materials count ranging from 50 to 150 components. This is the only tool that lets you instantly compare performance and cost for many alternative system combinations including topology, intermediate voltage rails, footprint, efficiency, component count and cost, and



quickly implement them".

When engineers finish "dialing-in" their preference for footprint, system bill of materials (BOM) cost and power efficiency, Power Architect's graphical analysis capability instantly identifies major sources of power dissipation, cost and footprint area. It allows the user to edit individual power supplies and loads to further model and optimise the overall

system for thermal and electrical performance design goals. When the design is complete, the tool generates a system summary report including schematics, BOMs and electrical operating values. Multiple international distributors provide pricing and the "Build It!" feature offers complete BOM prototype kits with overnight shipping. Roughly 300,000 accumulated

with output currents up to 5A

designs have been counted by end of 2009, more than 40% of them from Europe. "In terms of applications LED lighting becomes mainstream. And sequencing of individual power rails will be realised within the next Webench version". Gibson added. AS

www.national.com/switcher www.national.com/powerarchitect



Easy power supply design via Webench Power Architect

Gallium Nitride Gains Momentum

Recent developments and the upcoming events illustrate that Gallium Nitride (GaN) will gain momentum in power electronics since more and more established semiconductor companies as well as start-ups even in Europe enter this train.

Recently Belgium-based nanoelectronics research center Imec presented at IEEE IEDM 2009 in Baltimore an innovative GaN-on-Si double heterostructure FET architecture for GaN-on-Si power switching devices. The architecture meets the normally-off requirements of power switching circuits and is characterised by low leakage and high breakdown voltage, both essential parameters to reduce the power loss of high-power switching applications.

Imec obtained a highbreakdown voltage of almost 1000V combined with low onresistance by growing an SiN/AlGaN/GaN/AlGaN double heterostructure FET structure on a Si substrate. By combining its double heterostructure FET architecture with in-situ SiN grown in the same epitaxial sequence as the III-nitride layers, Imec succeeded in obtaining enhanced mode device operation. This is typically required in applications for safety reasons. The fabrication is based on an optimised process for the selective removal of in-situ SiN. The resulting SiN/AlGaN/GaN/AlGaN double heterostructure FET is characterised by a high

breakdown voltage of 980V, high uniformity and a low dynamic specific on-resistance of 3.5 m_.cm_ that is well within the present state-of-theart. These results hold the promise of a huge market opportunity for GaN-on-Si power devices.

Within its industrial affiliation program (IIAP) on GaN-on-Si technology, Imec and its partners (i.e. National Semiconductor) focus on the development of GaN technology for both power conversion and solid state lighting applications. An important goal of the program is to lower GaN technology cost by using large-diameter GaN-on-Si and hence by leveraging on the scale of economics. Imec invites both integrated device manufacturers and compound semiconductor industry to join the program and to benefit from sharing of cost, risk and talent.

"Performance is only one dimension of the equation leading to the conclusion that GaN-on-silicon is a gamechanger. The other dimensions are product reliability and cost", comments Alex Lidow, formerly CEO of International Rectifier and now heading the start-up Efficient Power



200V Silicon Device (30 milli Ohms) 200V GaN Device (25 milli Ohms) (25 milli Ohms)

Size comparison between 200V Si MOSFET and 200V GaN device featuring nearly same on-resistance Source: EPC

Conversion Corporation in El Segundo/USA.

According to Lidow HEMT (High Electron Mobility Transistor) GaN transistors first started appearing in about 2004 with depletion-mode RF transistors made by Eudyna Corporation in Japan. Using GaN on silicon carbide substrates, Eudyna successfully brought into production transistors designed for the RF market. The HEMT structure demonstrated unusually high electron mobility near the interface between an AlGaN and GaN heterostructure interface. Adapting this phenomenon to Gallium Nitride grown on Silicon Carbide, Eudyna was able to produce benchmark power gain in the multi-gigahertz frequency range. In 2005, **Nitronex Corporation**

Imec's SiN/AlGaN/GaN/AlGaN double heterostructure FET feature a breakdown voltage of 980V

Source: Imec

introduced the first depletion mode RF HEMT transistor made with GaN grown on silicon wafers. In 2009 EPC introduced its enhancementmode GaN on silicon power transistors designed specifically as power MOSFET replacements. These products are designed to be produced in high-volume at low cost using standard silicon manufacturing technology and facilities. At CIPS 2010 in Nuremberg Lidow will explain this technology and product roadmap in detail.

Besides Imec and EPC other vendors such as International Rectifier (see PEE 5/2009, pages 23 - 27) or Azzuro and MicroGaN in Germany (PEE 7/2009, page 15 - 16) have already introduced GaN products for power electronic applications. Now the race is open! AS

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Focus on Applied Power

The Applied Power Electronics Conference and Exposition (APEC) celebrates its 25th anniversary from February 21 - 25 in Palm Springs (California/USA). About 1900 attendants registered for the event in 2009, along with some 150 exhibitors, making it one of the most important power electronic events also in 2010. New semiconductor materials such as GaN are expected to gain more attention at this conference.

Seminars will start on Sunday (Febr. 21) to Febr. 22. Tim McDonald, International Rectifier, will give a seminar on "Current State and Future Improvements of GaN Based Power Conversion". GaN on Si based power conversion has received a lot of recent public notice and has been positioned as a "next generation" solution to provide sustained dramatic improvement in switch performance at a time when silicon power transistors are approaching some physical limits in performance. This seminar is directed towards the intermediate to advanced level audience of power design engineers, systems engineers, component engineers and power design managers. Seminar attendees will witness GaN power conversion in a host of applications from point of load to PFC and will be brought up to date on the progress GaN on Si has made from prototypes to products. Modeled and actual performance benefits will be studied.

Cree's Robert Callanan will give a seminar on "Silicon Carbide Characteristics and Applications". This will be an in-depth discussion of characteristics and application of silicon carbide (SiC) 1200V, 20A DMOSFETs from the experienced user's perspective. The SiC DMOSFET has the advantages of low conduction and switching loss along with higher operating temperature capability. However, the operating characteristics of this device are different from what is usually expected from Si MOSFETs superjunction MOSFETs, and IGBTs. The chief purpose of this seminar is to provide an understanding of these differences so that the SiC DMOSFET can be applied to its fullest potential. This will be achieved by a discussion of the operating characteristics of the SiC DMOSFET and how they differ from representative Si MOSFETs and IGBTs. This will include comparisons between DC output characteristics, forward conduction, transfer curves,



Welcome to APEC 2010

leakage current, gate charge, switching, and body diode considerations. Application considerations will also be discussed throughout. This seminar will also include a brief description of the operating characteristics of the SiC bipolar junction transistor (BJT) which is an attractive device for power conversion applications.

Dean Venable, Ablepower Corporation, will give a hands-on seminar on "Analog and Digital Feedback Loop Design". He will discuss the three basic types of analogue feedback amplifiers, Type 1, Type 2, and Type 3, and show how they directly relate the three types of digital feedback compensators, I, PI, and PID. Anyone with a degree in Electrical Engineering should be able to follow this seminar. A live demonstration is showing how to measure digital loops as easily as analogue loops. Everyone in the audience will learn how to stabilise a feedback loop by actually doing it.

Doug Hopkins, University at Buffalo, helds a seminar on "Power Electronics in a Smart-Grid Distribution System". Power Electronics is an integral part of the future Smart-Grid Distribution System, particularly as multiple opportunities are availed with the introduction of more DC generation and distribution. However, the fundamentals of power flow and system dynamics are the same from transmission through distribution to end-use. This seminar focuses on how power electronics affects power flow in grid distribution and distributed energy systems, and what power controllers need to do to offer greater benefits to system stability and economic resource. A distributed generation system, as found in a smart grid interconnection of several intermittent power sources, e.g. batteries, fuel cells, PV and wind turbines, is used to describe power electronic networks that affect the basics of power flow control and transient system stability. Topics are introduced from 'an electronics processing perspective'. With the move to greater DC generation and direct load usage, a good segment is devoted to DC system challenges for cabling and protection.

What are the trends?

The plenary session on February 22 afternoon will give an introduction to some of the main topics, starting with a look back on APEC history by John Kassakian, one of four key contributors to the origin of APEC.

The demise of the Power Concepts, Inc. International Power Electronics Conference (1975-1984), better known by its registered service mark Powercon, left the power electronics industry without a conference focused on the working engineer. There were other power electronics conferences, such as the more specialized IEEE Power Electronics Specialists Conference (PESC), but these were generally oriented more towards publishing of advanced research than solving the problems of the day. The IEEE Power Electronics Council, the predecessor to the IEEE Power Electronics Society (PELS), acted to fill this void and created the Applied Power Electronics Conference and Exposition. The first APEC was held in April of 1986, only about nine months after the concept was first proposed. APEC has been held every year since.

JB Straubel, CTO of Tesla Motors, will give a keynote on "Power Electronics and continued improvements in Electric Vehicle performance, efficiency and drivability". Batteries are usually the first topic of discussion for electric vehicles and with good reason due to their dominance over vehicle range but the power electronics that manage the flow of all electricity between the battery, motor and power grid have been improving quickly and offering dramatic improvements in overall vehicle acceleration, charging times, reliability and cost. At Tesla Motors we have moved through four generations of power electronics in the Roadster sports car and each time increased current density and motor torque substantially while decreasing cost. These increases in current and torque offer immediate and tangible value to consumers relative to internal combustion vehicles and they have allowed us to eliminate a two-speed transmission and the associated shift times and cost. In just the last few years it has become possible to build an electric power-train with better overall performance than any internal combustion engine and these desirable driving characteristics will only accelerate EV adoption beyond the environmental benefits. Power electronics improvements and cost reductions are also allowing for faster charging rates and more sophisticated vehicle interfaces with the power grid.

The 3rd keynote given by Robert V. White, Chief Engineer at Embedded Power Labs, covers "Digital Power: After the Hype". Not so long ago it seemed every power electronic publication had an article on the wonders of digital power. Digital power was going to reduce cost, increase functionality, increase efficiency, have units send out messages they were failing, and with adaptive controls, put power electronics engineers out of work. Digital power has inspired countless papers and seminars as well as a digital power specific conference. Now that the hype has mostly



passed, what is the state of digital power? Has it delivered on its promises? This talk will try to answer those questions. What we see today is that digital power is alive and well, quietly making inroads all across the power electronics spectrum. Even powerful digital signal processors (DSPs) are inexpensive enough to be considered for many designs. And digital signal controllers - hybrids between feature rich microcontrollers and computationally powerful DSPs offer designers new low cost ways to both close the loop and implement housekeeping functions. Cycle by cycle loop compensation in new ICs coming to market offer eliminates instability problems once and for all. In the server world, PMBus(tm) is being use to enable energy saving system management functions. So while digital power has not yet, and probably never will, live up to the hype, it is becoming a powerful tool in the power electronics designer's toolbox.

Victor K. Lee, CTO at Emerson

Network Power, will talk on "Power and Cooling for Future Data Center". There are two challenges facing today's data center operation: firstly, current utilisation of data center resources is very low - server utilisation is around 35%, storage utilisation is only at 30% and network utilisation is only about 35%. Secondly, power and cooling capacities are limited; it is an important and challenging task to improve power and cooling architectures to meet the increasing demand for power density. To solve under-utilisation issues, the computing industry is moving towards virtualisation on server, storage system and data center. Thus, the trend for future data center design starts is virtualisation to "private cloud computing" to "cloud computing". This tendency definitely has significant impact to the power and cooling architecture for future data center. The four most critical challenges in power and cooling for

future data centers: availability of

power capacity, rising cost of energy, complexity and scalability are the focus of this keynote.

Ron Van Dell, President and CEO SolarBridge Technologies, finally will talk about "Power Conversion and Energy Harvest in Distributed Photovoltaics to Generation Systems".

DC/AC inverters are key to overall photovoltaics system function yet only represent about 10% of total system cost. However, this critical element of power electronics has historically not really been challenged to make a real difference in total system performance. There is an opportunity - and a genuine need for the inverter in PV systems to become much more than another part of "Balance of System" costs, somewhere in between the cost of solar panels and installation. Where progress has been made it has been generally in improving efficiency in very large inverters used in utilityscale installations. Distributed generation of solar power, particularly on residential and light commercial

APEC 2009 exhibition featured more than 150 exhibitors Photo: AS

roof-tops, is major new segment to be developed, but poses some unique challenges, and has not been well served with current technologies based on high voltage DC feeds into centralised inverters. Recently, major strides are being made in microinverters by a number of companies with the objective of doing roof-top power conversion on a per-panel basis. This approach can yield significant gains in how many sites can qualify for PV, and increase energy harvest, while also decreasing installation cost. There are, however, some tough technical challenges that must be overcome if ACPV is to realise its full potential and accelerate the timing to grid parity.

Besides the plenary sessions numerous papers will be given in technical, special, dialogue and rap sessions.

www.apec-conf.org

Focusing on Power Systems

CIPS stands for the 6th International Conference on Power Electronics Systems Integration. It will be held from March 16 to 18 at Nuremberg's Maritim Hotel. It will be co-organised by German VDE ETG, ECPE, ZVEI and IEEE PELS. CIPS 2008 attracted more than 180 delegates.



The three main topics of CIPS are power electronics systems, highpower modules, and reliability of power electronics systems. For all three topics system integration will help to increase power density (and reduce costs), to increase performance (and reduce EMI), and improve reliability by a more efficient thermal management (and better cooling).

One of the basic ideas of CIPS is to bring together industry and academia such, that industry is describing new concepts and needs and academia is providing solutions for it. The scientific/technical quality of presentations and written papers, however, is ensured by an Technical Programme Committee headed by Dieter Silber (University of Bremen) and Eckhard Wolfgang (ECPE).

Two keynotes, 11 invited and 41 oral papers, 18 posters and one panel discussion will be presented. 26 come from industry, 26 from academia, 7 are authored by industry and academia and 13 come from applied research institutes.

Johann Kolar (ETH Zurich) will open the CIPS 2010 with the keynote on "Performance,

Trends and Limitations of Power Electronics". The status of "Integrated Driver Circuits" will be described by Reinhard Herzer (Semikron). Dushan Boroyevich (CPES) will give an overview on "Status of Power Electronics Systems Integration", followed by 4 papers on this topic.

Michel Mermet-Guyennet starts the reliability session with a contribution to "Railway Traction Reliability" followed by five regular papers. Three contributions to driver circuits finish the oral presentations of day 1. The Dialog Session starts at 19:15 during that Franconian snacks and beverages will be served.

The second day starts with five invited papers entitled "Power Electronics System Integration for Electric and Hybrid Vehicles" by Martin März (Fraunhofer IISB),

"Solar Power Converters" by Regine Mallwitz (SMA), "Fault Tolerant Designs" by Glynn Atkinson (Univ. Nottingham), "Paralleling of High-Power Modules" by Ulrich Schlapbach, (ABB Semiconductors), and "Nondestructive SOA Testing of Power Modules" by Giovanni Busatto (Univ. Cassino). In the afternoon there are two parallel sessions on "Power Electronics and DC/DC Converters", and in parallel "Packaging and Materials". The final session on day 2 is a Panel Discussion on "Virtual Prototyping - CAD Tools for Power Electronics: What is available and what is missing", moderated by Thomas Harder (ECPE) and Dushan Boroyevich (CPES).

The third day starts with an invited lecture on "Prognostics and Health Management" by Chris Bailey (Univ. Greenwich). He will explain how the "rest-of-life" of a system under operation can be estimated. The following five papers will deal with thermal management, two with EMI and two with advanced cooling technologies. Finally, in the afternoon session "Future Perspectives" there will be two invited papers "New Semiconductor Technologies Challenge Package and System Setup" by Gerhard Miller (Infineon Technologies), and "Future Power Device Possibility" by Ichiro Omura (Univ. Kyushu).

Finally, Alex Lidow (EPC) will present the second keynote on "Is it the End of the Road for Silicon in Power Management?" where he will discuss the perspective of GaN devices and systems. In the closing session the best regular oral paper will receive the "ECPE Best Paper Award" as well as the best poster the "VDE ETG Best Poster Award".

www.cips-conference.de

CIPS 2010 program overview

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Energy Savings and Sustainability



The power electronics sector is further growing. Additionally, the overall economic climate brightens up. This positive trend can be recognised at PCIM Europe 2010 as well. Around 6,000 visitors and 255 exhibitors were on the floor at PCIM 2009, and more than 500 delegates attended the conference. From May 4 - 6 this year the PCIM Europe Conference in Nuremberg offers a program with focus on energy savings and sustainability.

The day before the exhibition and conference a series of tutorials will help answer the key questions currently being posed in the power electronics sector. New tutorials in 2010 are "Power Electronics and Control for Renewable Energy Systems; Batteries, Charger Solutions, Monitoring and Management Systems; Electromagnetic Design of High Frequency Converters; Switching Power Supply Design; Application design criteria for ultrafast switching MOS-controlled reverse conducting devices and management of their parasitic effects.

In more than 170 papers highly respected authors from industry and science will present the results of their latest research and user reports. Other highlights include the keynote papers at the beginning of each conference day featuring "Energy Storage" by Dirk Uwe Sauer (RWTH Aachen/Germany), "HVDC Light can deliver 1,100 MW" by Björn Jacobson (ABB/Sweden), and "Virtual Prototyping of Power Electronic Systems" by Jürgen Biela (ETH Zurich/Switzerland).

As in previous years, Power Electronics Europe has organised a Special Session entitled "Power Electronics for Efficient Inverters in Renewable Energy Applications" which meets directly the PCIM 2010 focus, it will be held on May 4 early afternoon just after lunch break. The four papers will concentrate on wind and solar energy applications from a power electronics designer perspective and will include of course the latest developments in power semiconductors. And PEE will also sponsor for the 3rd time the Best Paper Award to be handed over at the official conference opening on May 4.

Early conference registration rates are available until 26 March 2010.

www.pcim.de

VTH Aachen	Application Optimized Switches	Digital Power and Energy Effincieny	I C H	Power Electronics for Efficient Inverters in Renewable Energy Applications	Thermal Aspects in Power Systems	gue Sessions
D. Sauer, RV	High Power Converters	Sensorless Drives I	LUN	Power Electronics in Energy Generation and Distribution	Sensorless Drives II	Poster / Dialo
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of Power Electr J. Biela, E	ECPE Panel Discussion »Electronics for Energy Efficiency and Sustainability«	Motor Drives	I U N	Sensors and Metering	Electrical Machines	



ABOVE: PCIM 2010 program overview

LEFT: PCIM Exhibition development 2007 - 2009

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Power Density and Performance Improvement of New Automotive Power Semiconductor Packages

Steadily but surely automobile manufacturers are looking to design out the engine-driven auxiliary loads such as fuel, water, brake and power steering pumps with electric driven ones. Here MOSFETs are the devices of choice to power such applications. Improved fuel efficiency, reliability and reduced CO₂ emissions are the main drivers, and variable speed electric drives rise to this challenge, but the dominance of the existing technology is strong. With Automotive DirectFET 2, the lead frame, wire bonding and molding are eliminated all together leading to further performance and reliability improvements. **Benjamin Jackson, Product Manager Automotive MOSFETs, International Rectifier, USA**

In March 2009 the Ford Motor Company announced that by 2012 it was targeting to have up to 90% the vehicles it produces equipped with Electric Power Steering. Ford cited the improved performance and a possible 5% fuel economy as driving factors for this rapid adoption.

Power density is a phrase often used in describing servers, but less often associated with cars, but it is indeed important; the vehicle needs to be a finite size and increasingly to meet emissions and fuel consumption regulations limits are put on weight. A typical lead acid battery has an energy density of around 0.1MJ/kg compared with around 45MJ/kg for gasoline; this is one reason why such advanced battery technology is needed to make hybrid and electric vehicles a practical reality - the traditional technology offers great energy density. Similarly the existing engine and hydraulic driven pumps on a car offer very good power density compared with a typical electrical motor, so replacing these traditional solutions with electric drives requires advanced motor design and highly efficient and compact power electronics.

Semiconductor switching losses

No semiconductor today is an 'ideal' switch with an infinitely low on resistance so heating occurs, and how this energy is managed and extracted from the switch, greatly affects power density. Consider thermal resistances and electrical resistances to be alike, temperature difference like electrical potential difference and power transfer the equivalent of current flow. Thus the power dissipation in the steady state of a semiconductor can be expressed according to equation 1 [1],

(1)
$$Pd = \frac{T_j - T_A}{R_{thJA}}$$

where Pd is the power dissipated in the semiconductor switch, T_i is the junction temperature, T_A the ambient temperature and $R_{\text{thu}A}$ is the total thermal resistance from junction to ambient.

Linking power dissipation to current through the MOSFET allows a current density comparison between packages to be made, taking equation 2 into account:

$$(2) \quad P_d = I_D^2 R_{DS(on)}$$

Substituting 1 and 2 together we arrive at equation 3:

(3)
$$I_D = \sqrt{\left(\frac{T_j - T_A}{R_{thJA}}\right) / R_{DS(on)}}$$

Finally dividing by the area of the MOSFET's PCB footprint we can arrive at the current density of a particular switch (equation 4):

(4)

$$CurrentDensity = \frac{I_D = \sqrt{\left(\frac{T_j - T_A}{R_{bblA}}\right) / R_{DS(on)}}}{A_{CD}}$$

We will now use equation 4 to see how we can increase current density and compare and contrast how different power semiconductor packages maximise this metric. Essentially there are three routes to getting good current power density in MOSFETs:

- 1) Minimal junction heating through using the lowest possible $R_{\mbox{\tiny DS(on)}}$
- 2) Extract the heat as efficiently as possible
- 3) Make the MOSFET as small as possible without sacrificing 1 and 2.

Keeping it small

Ultimately the smaller the footprint the MOSFET greater the power density, however such a reduction in package footprint area must not be done at the expense of RDS(GN) or current carrying ability. Ultimately the designer wants to get the lowest RDS(GN) possible in a given space. As die size and RDS(GN) are inversely proportional, calculating the ratio of package footprint area to maximum die size area for the given package is an indication of the RDS(GN) performance that a given package can offer in a given space. Figure 1 plots the ratio of package footprint to maximum die size area.

In Figure 1, the ideal ratio would tend towards 1, giving the least mm² of PCB footprint for a given RDS(OM). However it clearly shows the area overhead that the more traditional packages such as the DPak and D2Pak place on the die size area, and ultimately the reduction in current density. The D2Pak has a package footprint to maximum die size area of 5; the package area is five times the size of the largest die size. Large Can DirectFET however offers a ratio of about 1.7 - so ultimately on the PCB a given RDS(OM) in a smaller space can be achieved.

The technology and basic design of the D2Pak and DPak have changed little over the years, the leadframe, wrie bonds and molding take up area and volume while at the same time impeding performance;



Figure 1: Package footprint to maximum die size area

they are an increasingly bothersome overhead as semiconductor technology improves. The latest power packages like the 5x6 PQFN fit far more silicon in a given space and in the case of Automotive DirectFET 2, the lead frame, wire bonding and molding are eliminated all together leading to further performance and reliability improvements.

Limiting heating

There have been dramatic advances in semiconductor technology over the years to achieve the lowest possible RDS(m) for a given area of silicon. Now with the very best trench technology and smallest geometries semiconductor designers are coming close to the fundamental

performance limits of silicon, so not surprisingly new substrates like Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming popular as they can offer up to 10 times lower RDS(m) per area than a silicon based technology.

But before getting absorbed in new materials it's important to realise that there is still room for improvement on the packaging which will house the semiconductor, regardless of whether it's a Silicon or Silicon Carbide switch.

MOSFETs with an on-resistance of around $< 2m\Omega$ are common place in the market today and increasingly on such devices around half of the R_{DS(an)} stated on the datasheet is not attributed to the semiconductor die, but due to the

packaging, or the Die Free Package Resistance (DFPR). Figure 2 shows the DFPR values for different types of packages, the lead frame and wire bonds used in the package add a significant distance to the path that the electrical current has to flow along and therefore make a large contribution to the RDS(on). When the wire bonds and leadframe removed (in the case of DirectFET) the DFPR is reduced to a value of less than half of equivalent plastic power package. The removal of this barrier ultimately means that a lower area of silicon is needed for a given RDS(on), and opening up the possibility of a system level cost saving.

Cooling down

From equation 4 its can be seen that as RthJA tends to zero the current density will increase as the heat generated in the junction is extracted and dissipated into the ambient more easily. Figure 3 shows the two thermal routes that make up the RthJA for different package types, Rth(J-C) top the thermal route through the top of the package, and $R_{th(J-PCB)}$ through the bottom of the package to the PCB. Power packages like the D2Pak and copper strap PQFN have excellent junction to PCB thermal paths, but like all the other traditional packages they are far less effective at allowing the heat generated to flow out through the top of the package, indeed they were not designed with top side cooling in mind. However when both top and bottom thermal paths are utilised drastic reductions in Rtha can be made, as can be seen on the



Figure 2: Comparison of Die Free Package Resistance (DFPR) for different semiconductor power packages semiconductor power

packages



DirectFET package type.

 Table 1: Comparison

 of Current Density for

 a D2Pak-7P and a

 Large Can DirectFET

 with different cooling

 arrangements

Drawing the factors or space, R_{DS(or)} and R_{thA} together, Table 1 makes a side by side comparison of a large die, low R_{DS(or)} D2pak product with a counterpart Automotive DirectFET product using equation 4. The table summarises the improvement in current density. By taking two high performance 40V power MOSFETs which are typically used in automotive applications Table 1 shows how the simple construction of package like DirectFET, the elimination of wire bonds and leadframe allows $R_{DS(en)}$ PCB footprint and R_{thA} to be minimised. This results in current density to be increased by over 3 times when compared with a traditional plastic D2Pak-7P, even in an

Part	AUIRFS3004-7P	AUIRF7739L2
Package	D2Pak-7P	Large Can DirectFET
PCB Footprint	170 mm ²	64 mm ²
Single Side Cooled on FR4		
R _{thJA} (Single side cooling)	40 °C/W	40 °C/W
R _{DC(on)} @ T _j = 105°C, T _A = 25 °C	1.24 mΩ	0.9 mΩ
	40.13 A	46.29 A
	0.24 A/mm ²	0.73 A/mm ²
Ratio of current density	1	3.1
Dual Sided Cooled		
R _{thJA} (Dual side cooling DF only)	12.5 °C/W	40 °C/W
R _{DC(on)} @ T _j = 105°C, T _A = 25 °C	1.24 mΩ	0.9 mΩ
	40.13 A	82.81 A
Current Density	0.24 A/mm ²	1.3 A/mm ²
Ratio of current density	1	5.5

application where dual sided cooling is not used.

Conclusion

The ability to drive more current through a smaller space, at higher efficiency and increase power density is going to become of greater importance as the electrification of the automobile unfolds. The replacement of fuel tanks and spark plugs of the past with batteries, IGBTs and MOSFETs of today will not happen by default. The new power electronic drive trains will not only have to meet but exceed the performance of the traditional internal combustion engine powered solution. With such demanding goals the use of next generation power semiconductor power packages which interfere less with the operation of the semiconductor will be key to ensure next generation efficiency, power density and performance goals are met.

Literature

[1] Power MOSFETs, Theory and Applications, Duncan Grant, John Gower



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Subcon

"Tuesday and Wednesday were both very busy days with a good calibre of enquiries and a good response. We had 12 people manning the stand and they were all very busy."

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"Initial indicators on the decision to go back to Drives and Controls were well founded. Quality leads from a busy 3 days."

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John Wilkins – Rittal Ltd

"A superb show. By the end of the Tuesday we already knew that we would be back in 2010."

Dave Proud – KTR

Energy Harvesting Gets a Boost

A wide range of low-power industrial sensors and controllers are turning to alternative sources of energy as the primary or supplemental means of supplying power. Ideally, such harvested energy will eliminate the need for wired power or batteries altogether. Although energy harvesting has been emerging since early 2000 (its embryonic phase), recent technology developments have pushed it to the point of commercial viability. In short, in 2010 we are poised for its "growth" phase. Building automation sensor applications utilising energy harvesting techniques have already been deployed in Europe, illustrating that the growth stage may have already begun. **Tony Armstrong, Director of Power Product Marketing, Linear Technology, USA**

Transducers that create electricity from

readily available physical sources such as temperature differentials (thermoelectric generators or thermopiles), mechanical vibration (piezoelectric or electromechanical devices) and light (photovoltaic devices) are becoming viable sources of power for many applications. Numerous wireless sensors, remote monitors, and other low-power applications are on track to become near "zero" power devices using harvested energy only (commonly referred to as "nanoPower" by some).

Commercial acceptance

Even though the concept of energy harvesting has been around for a number of years, the implementation of a system in a real world environment has been cumbersome, complex and costly. Nevertheless, examples of markets where an energy harvesting approach has been used include transportation infrastructure, wireless medical devices, tire pressure sensing, and of course, building automation. In the case of building automation, systems such as occupancy sensors, thermostats and light switches can eliminate the power or control wiring normally required and use a mechanical or energy harvesting system instead.

Similarly, a wireless network utilising an energy harvesting technique can link any number of sensors together in a building to reduce heating, ventilation & air conditioning (HVAC) and lighting costs by turning off power to non-essential areas when the building has no occupants. Furthermore, the cost of energy harvesting electronics is often less than running sense wires, so there is clearly economic gain to be had by adopting a harvested power technique.

A typical energy scavenging

Figure 1: The LTC3108 serves as ultra-low voltage boost converter and power manager in energy-scavenging systems configuration or system, (represented by the four main circuit system blocks shown in Figure 1/2), usually consists of a free energy source such as a thermoelectric generator (TEG) or thermopile attached to a heat generating source, such as an HVAC duct for instance. These small thermoelectric devices can convert small temperature differences into electrical energy. This electrical energy can then be converted by an energy harvesting circuit (the second block in Figure 2) and modified into a usable form to power downstream circuits. These downstream electronics will usually consist of some kind of sensor, analogue-to-digital converter and an ultra-low power microcontroller (the third block in Figure 2). These components can take this harvested energy, now in the form of an electric current, and wake up a sensor to take a reading or a measurement then make this data available for transmission via an ultra-low power wireless transceiver - represented by the fourth block in the circuit chain shown in Figure 2.

Each circuit system block in this chain, with the possible exception of the energy source itself has had its own unique set of constraints that have impaired its commercial viability until now. Low cost and low power sensors and microcontrollers have been available for quite sometime; however, it is only within the last couple of years that ultra-low power transceivers have become commercially available. Nevertheless, the laggard in this chain has been the energy harvester and power manager.

Existing implementations of the power manager block are a low performance discrete configuration, usually consisting of 35 components or more. Such designs have low conversion efficiency and high quiescent currents. Both of these deficiencies result in performance compromised in an end system. The low conversion efficiency will increase the amount of time required to power up a system, which in turn increases the time interval between taking a sensor reading and transmitting this data. A high quiescent current limits how low the energyharvesting source can be since it must first overcome the current level needed for operation before it can use any excess to supply power to the outputs.

New boost converter and system manager

What has been missing until now has been a highly integrated DC/DC boost





Figure 2: The four main blocks of a typical energy-scavenging system

converter that can harvest and manage surplus energy from extremely low input voltage sources. However, the LTC3108 (Figure 1), an ultra-low voltage boost converter and power manager, greatly simplifies the task of harvesting and managing surplus energy from extremely low input voltage sources such as thermopiles, thermoelectric generators (TEGs) and even small solar panels. Its step-up topology operates from input voltages as low as 20mV. This is significant since it allows the LTC3108 to harvest energy from a TEG with as little as 1K temperature change.

The circuit shown in Figure 3 uses a small step-up transformer to boost the input voltage source to a LTC3108 which then provides a complete power management solution for wireless sensing and data acquisition. It can harvest small temperature differences and generate system power instead of using traditional battery power.

The LTC3108 utilises a depletion mode N-channel MOSFET switch to form a resonant step-up oscillator using an external step-up transformer and a small coupling capacitor. This allows it to boost input voltages as low as 20mV high enough to provide multiple regulated output voltages for powering other circuits. The frequency of oscillation is determined by the inductance of the transformer's secondary winding and is typically in the range of 20kHz to 200kHz.

For input voltages as low as 20mV, a primary-secondary turns ratio of about 1:100 is recommended. For higher input voltages, a lower turns ratio can be used. These transformers are standard, off-theshelf components, and are readily available from magnetic suppliers. Our compound depletion mode N-channel MOSFET is what makes 20mV operation possible.

The LTC3108 takes a "systems level" approach to solving a complex problem. It can convert the low voltage source and manage the energy between multiple outputs. The AC voltage produced on the secondary winding of the transformer is boosted and rectified using an external charge pump capacitor and the rectifiers internal to the LTC3108. This rectifier circuit feeds current into the VAUX pin, providing charge to the external VAUX capacitor and then the other outputs.

The internal 2.2V LDO can support a low-power processor or other low power ICs. The LDO is powered by the higher value of either VAUX or VOUT. This enables it to become active as soon as VAUX has charged to 2.3V, while the VOUT storage capacitor is still charging. In the event of a step load on the LDO output, current can come from the main VOUT capacitor if VAUX drops below VOUT. The LDO output can supply up to 3mA.

The main output voltage on Vour is charged from the VAUX supply and is user programmable to one of four regulated voltages using the voltage select pins VS1 and VS2. The four fixed output voltage are: 2.35V for supercapacitors, 3.3V for standard capacitors, 4.1V for Lithium-Ion





battery termination or 5V for higher energy storage and a main system rail to power a wireless transmitter or sensors thereby eliminating the need for multi-M Ω external resistors. As a result, the LTC3108 does not require special board coatings to minimise leakage, such as discrete designs where very large value resistors are required.

A second output, Vour2, can be turned on and off by the host microprocessor using the Vour2_EN pin. When enabled, Vour2 is connected to Vout through a P-channel MOSFET switch. This output can be used to power external circuits such as sensors or amplifiers that do not have low power sleep or shutdown capability. An example of this would be to power on and off a MOSFET as part of a sensing circuit within a building thermostat.

The VSTORE capacitor may be a very large value (even multiple Farads), to provide hold-up at times when the input power may be lost. Once power-up has been completed, the main, backup and switched outputs are all available. If the input power fails, operation can still continue, operating off the VSTORE capacitor. The VSTORE output can be used to charge a large storage capacitor or rechargeable battery after Vour has reached regulation. Once Vour has reached

Figure 3: The LTC3108 used in a wireless remote sensor application powered from a TEG (Peltier cell)

regulation, the V_{STORE} output will be allowed to charge up to the V_{AUX} voltage, which is clamped at 5.3V. Not only can the storage element on V_{STORE} be used to power the system if the input source is lost but it can also be used to supplement the current demanded by V_{OUT}, V_{OUT2} and the LDO outputs if the input source has insufficient energy.

Conclusion

With analogue switchmode power supply design expertise in short supply around the globe, it has been difficult to design an effective energy harvesting system as illustrated in Figure 1. However, with the introduction of the LTC3108 thermal energy harvesting, DC/DC boost converter and system manager that's all about to change. This device can extracts energy from solar cells, thermo-electric generators or other similar thermal sources. Furthermore, with is comprehensive feature set and ease of design, it greatly simplifies the hard-to-do power conversion design aspects of an energy harvesting chain.

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IXGA30N60C3C1	600V	30A	3.0V	47ns	0.33mJ	0.56°C/W	TO-263		
XGP30N60C3C1	600V	30A	3.0V	47ns	0.33mJ	0.56°C/W	TO-220		10A
XGH30N60C3C1	600V	30A	3.0V	47ns	0.33mJ	0.56°C/W	TO-247		RE
XGH30N60B3C1	600V	36A	1.8V	100ns	1.50mJ	0.5°C/W	TO-247		141
XGH48N60B3C1	600V	48A	1.8V	116ns	1.30mJ	0.42°C/W	TO-247		
IXGH48N60C3C1	600V	48A	2.5V	38ns	0.57mJ	0.42°C/W	TO-247		
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Features

+15V/-10V gate voltage 3W output power 20A gate current 80ns delay time Direct and half-bridge mode Parallel operation Integrated DC/DC converter Electrical isolation for 1700V IGBTs Power supply monitoring Short-circuit protection Fast failure feedback Superior EMC

Design Concept for a Transformerless Solar Inverter

Vincotech is able to offer a wide spectrum of power modules for solar applications. For transformer-less single phase solar inverter the power module FZ06BIA045FH-P897E is able to carry a output power of 6kW but for efficiency optimisation a nominal power of 3kW is recommended. **Michael Frisch and Temesi Ernö, Vincotech Germany and Hungary**



The topology is supporting the required functions of adjustment to the maximum power point (MPP) of the solar string and inverting to sinusoidal output current and voltage (see Figure 1).

Booster

The booster is active when the solar voltage is below the peak of the power grid voltage.

In this case the booster (T5, D8,9) sets the MPP for the photo voltaic solar cell (PV). When the PV MPP voltage reaches the peak of the line, the bypass diode (D7) cuts boost stage losses. The adjustment of the MPP has to be controlled by the output H-bridge inverter. The output of the booster is the DC link voltage, filtered by a capacitor (C4). This capacitor should be a parallel composition of a high tangent delta film capacitor and an electrolytic capacitor. The high frequency capacitor have to be placed



close to the module pins to limit overvoltage shoots at turn off of the MOSFET (T2 and T4), while the electrolytic capacitor should be sized for the 100Hz power fluctuation of the 50Hz mains.

H-bridge inverter

The H-bridge works by asymmetric unipolar modulation. The high side of the asymmetric H-bridge should be driven by 50Hz half-wave dependent on the polarity of the mains while the opposite low side is PWM modulated to form the mains sinusoidal shape.

The 10nF ceramic capacitor (C5) should be placed close to the gate-emitter pins of the high side transistors to eliminate cross through conduction due to fast switching of the low side transistors. A negative gate turn off voltage on the high side gate may also improve switching performance. The low side gate drive resistor should be selected to adjust the speed of MOSFET switching.

Output filter and current sense

The inductors L1 and L2 are for the differential mode (DM) and common mode (CM) voltage filter. Both have a double winding, one of each in both phase connection (Figure 2).

However one of the inductors is connected with opposite winding direction in one phase connection. In this manner the utilisation of the inductor becomes more effective (Figure 3) than with single winding (Figure 4) inductors and delta capacitors, while still keeping the common mode voltage noise between line and DC link to an even lower level (Verrd).

If the output current sense is put before the inductor (L1), the test current will be the sum of output current to grid and CM (common mode) current to C1 and C2. So two current senses have to be used and put on the output line before L1. The output current to grid is determined by the sum of the two currents.

Power module

For a conclusive module design low induction in the DC-link is a must. To achieve this target, the internal inductivity caused by wire bonding, layout and module pinning has to be minimised. This means the DC+ and DC- pins in the boost circuit as well as in the output inverter have to be placed as close to each other as the standards allow. Also sense contacts for the fast-switching power transistors are necessary.

The parasitic inductance of the wire bond at switch on/off of the IGBTs or MOSFETs will reduce the gate signal. This might cause oscillations in the transistor or at least increased switching losses. The







Figure 3: Wave form dual inductor with split windings topology

Figure 5: Wave form

of the dual inductor

single winding

topology

current-less sense wire, bonded directly on the source or emitter pad of the transistor chip, will eliminate the problem. This is only possible with module technology.

Figure 6 shows the Vincotech standard module flowSOLO-BI (P896-E01) which incorporates the functions listed previously such as:

- Boost circuit with MOSFET (600V/45mΩ) and SiC rectifier
- Bypass diode for maximum power (when exceeding nominal power)
- H-bridge with 50A/600V IGBTs and SiC rectifier in the high side and MOSFET (600V/45m Ω) in the low side
- * Temperature Sensor

Efficiency

A simulation based on measured values of this circuit (here are only the semiconductor losses considered) shows the following results (conditions P_{IN} = 2kW, f_{PWM} = 16kHz, V_{PMominal} = 300V, V_{DC} = 400V): The efficiency for the module (booster + inverter) is 98,8%. This shows that a total efficiency, including the passive components, of 98% is reachable. Figure 7 also shows that the efficiency of the alternative full IGBT solution drops significantly at partial load.



ABOVE Figure 6: Module flowSOL0-BI incorporating boost circuit and mixed inverter

RIGHT Figure 7: Efficiency simulation result for the output inverter shows 99,2% compared to 97,2% of a pure IGBT solution (dotted line)



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25A

100A

50A

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APTGV50H60BG

APTGV25H120BG

SP6-P

Monitoring Batteries Improves UPS Reliability

Systems from mobile telecommunications to data centres must operate with minimal downtime, making the reliability of the electrical mains supply a key concern. Uninterruptable power supplies (UPSs), which provide back-up power in the event of mains failure, are therefore widely used to ensure critical electronic systems continue to function normally in the event that the mains power goes down. Sentinel III; a set of components for a battery monitoring addresses the needs of UPS OEMs and battery providers. These components are used to create a simple to install and intuitive solution for continuous battery monitoring within mission critical installations. **Loic Moreau, LEM SA, Geneva, Switzerland**

Although other technologies, such as

flywheels, can be used, most UPSs use batteries to store energy. Batteries provide significant capacity and are able to deliver power almost instantaneously. If the UPS is to operate reliably, it is essential that the batteries are not only fully charged, but also in good condition.

High influence on UPS performance

Battery cells have a limited lifetime, which can be shortened considerably if the environmental conditions - particularly temperature - are outside the optimum range. In most installations cells are replaced at a fixed interval based upon the warranty - typically every five years. This approach is imperfect: batteries operated outside of the expected environmental conditions can fail sooner, whilst well maintained batteries might have a longer lifetime.

Modern UPSs are required to deliver high power levels, and therefore many cells are required. In large strings, a failure in a single cell can cause the whole string to fail. Large and medium UPSs will implement redundancy to ensure that a string failing does not result in the entire UPS failing. Whilst the UPS will continue to operate, the peak current that can be delivered and the time for which the system can run using the UPS will both be reduced. Furthermore a failed cell can damage the other blocks in the string, reducing their lifetime.

Battery monitoring and maintenance represents a significant cost associated with running UPSs. Typically an engineer visits the site on a regular basis - perhaps monthly - to measure the electrical characteristics of the cells in the system. Typically the voltage of the cell will be measured, identify cells operating out of range, which will then be replaced. Output voltage is not always a good predictor of



Figure 1: Battery cell output voltage



Figure 2: Cell failure

failure, so cells may fail in between these regular visits, require an additional service.

Permanent monitoring of batteries not only reduces cost by reducing the time for an engineer to physically check the state of each of the batteries, making their site visits more efficient, but also allows for preventative maintenance. By identifying potential failures, cells can be swapped out during routine visits, ensuring greater reliability and removing the need for emergency engineer visits.

Monitoring a large UPS

LEM used the Sentinel (see Sidebar) battery monitoring system to measure the cells in a broadcast facility with an 800kVA UPS. Figure 1 shows the output voltages of a number of cells in one of the strings. In this case each string had 200 monoblocks, delivering around 440V. There is considerable variation in the voltage, which is due to incorrect configuration of the battery conditioning, which is discussed later in this article.

The graph clearly shows one cell is delivering 2V, rather than the nominal 2.2V. Although the block is producing a lower voltage than expected, the difference is relatively small, and is stable. This behaviour is typical, making the use of output voltage as an indicator of impeding failure is unreliable, as the voltages can be remain within thresholds and therefore alarms are not triggered.

In this case, the battery monitoring system was being used to assess the effectiveness of the scheduled maintenance approach, and not to warn of potential problems. As no action was taken, Figure 2 shows that on 9th October (10/9) the cell fails catastrophically. Note that prior to the cell voltage dropping to 0.7V, the voltage of the faulty block remains constant, giving no indication that the block is about to fail. The voltage returns to normal on 19th November when the cell was replaced.

The output voltage is not a good predictor of likely failure, as there was no change in its value prior to the failure of the cell. Another characteristic of the cell impedance - is a much better indicator as Figure 3 shows. This graph illustrates the impedance rising in June, and by the start of July the value has increased by more than 20%. A trend is easy to detect: measuring impedance could have identified the problem three months before the cell failed. If the customer used the impedance data, the cell could have been replaced during regular preventative maintenance before its deterioration caused the failure.

Permanent monitoring provides other useful information that can help increase



Figure 3: Cell impedance predicts failure

UPS reliability. For the example in Figure 1 it is clear that there are plenty of charge/discharge cycles (shown by the spikes on the voltage trace). Although all batteries need to undergo conditioning the battery discharge is much too frequent, with 4-5 discharges per month. Whilst some battery conditioning lengthens life, too many discharge cycles will reduce the lifetime: a normal configuration will cycle only two or three times per year. Typically cells have a guaranteed lifetime of 20-50 cycles. In the case we are considering the batteries would have exceeded this in just a few months, and a strategy of replacing batteries every five years would mean that the cells would undergo several times more discharge cycles than they were designed to endure.

The frequent charge/discharge cycles at this site were caused by the installer leaving the UPS in a commissioning mode that cycles the battery charge frequently to allow testing - a surprisingly common mistake that can drastically shorten the lifetime of the batteries. Erroneous configurations will not be obvious to engineers during their visits to the site continuous automatic monitoring, however, makes the problem obvious.

Another cause of shortened battery lifetime is high temperature. Even a small increase in temperature increases the rate of the unwanted chemical reactions in the battery that ultimately cause it to fail. Typically battery manufacturers quote lifetimes at 20°C. Figure 4 shows the ambient temperature in this system varying



Figure 4: Temperature monitoring

with time, and at one point reaching 22°C. The air conditioning failed to maintain the temperature within an acceptable range, which will result in a reduction in battery life. Furthermore the increased temperature may void the battery manufacturer's warranty.

Conclusion

Permanent battery monitoring offers many advantages, beyond the reduction in cost by making site visits by engineers more efficient. In this example automatic monitoring of the impedance of the battery would have identified a failing cell three months before the cell became faulty. Continuous monitoring also makes identifying UPS configuration problems simple: particularly incorrect charge/discharge frequency that can dramatically reduce battery life. Monitoring measures ambient conditions, ensuring that lifetime is not reduced because of high temperatures. Monitoring maximises the life of the cells, reducing the risk of failure and saving money by ensuring that strings do not need to be replaced prematurely, as well as ensuring early detection of deteriorating cells, often allowing replacement before the string goes down. Although critical systems such as UPSs are usually not the first target for cost savings, it is important that users switch to permanent monitoring as it both cuts cost and increases reliability.

Sentinel III Battery Monitoring Components

The Sentinel solution comprises transducers, data loggers and software components to create a standby battery monitoring solution (SBM). In order to extend the functionality of the existing Sentinel, LEM has developed the S-Box; a data logger featuring an embedded webserver, which enables administrators to monitor installations remotely. The state-ofthe art measurement and data logging features include bloc, string and battery voltage measurement, Bloc temperature and impedance measurement, discharge

performance and discharge/charge current. The S-Box also measures ambient temperature, a key factor affecting battery life.

The Sentinel transducer is designed to reduce installation time, offering DIN-rail mounting and an external temperature patch. Users can set up an alarm for each of the parameters measured by the transducers connected to the S-Box. As well as instant alarms the S-Box can also provide a weekly report to the administrator, containing all daily measurements and critical system information



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Thermal Behaviour of Three-Level Trench Gate IGBT Modules in PFC and PV Operation

The control of the power semiconductors in a three-level NPC topology employs a set of 12 control signals in total. A back-to-back two-level/three-level inverter has been built to circulate power performing arbitrary load conditions to analyse the thermal dissipation of the power semiconductors. This thermal analysis utilises an IR camera to perform an in-situ measurement and allows precise modelling of thermal and electrical parameters. Once this experimental platform has been calibrated, the loss on each semiconductor chip can be acquired and compared with the simulated results. Hence, tuning of the model parameters becomes possible. **Marco Honsberg and Thomas Radke, Mitsubishi Electric Europe, Germany**

The continuously growing consciousness towards energy saving needs have led to intense research towards highly efficient power conversion methods. Online Uninterruptible Power Supplies (UPS) being connected and loaded 24 hours and 7 days, as well as photovoltaic (PV) inverters, are dedicated applications with a high potential in energy saving by an

increase of the total system's efficiency. Besides the continuous improvement of the power device's inherent loss performance and the outlook to have Silicon Carbide (SiC) based switching devices and their optimised packaging technology widely available in a few years, three-level technology has been found efficient in decreasing a system's power loss

Three-level IGBT modules, with their comparatively complex structure in terms of chip layout and their thermal performance under varying load conditions, are essential to fabricate a compact and reliable threelevel inverter. Figure 1 shows a view into an opened three-level 13in one IGBT module. In addition to the pure NPC three-level structure, there is a 1200V-class IGBT to perform a braking operation in conjunction with the employed free-wheeling diode (FWD). Such a braking operation can become necessary in case a regenerative load is connected to the UPS. The circuitry of the module is shown in Figure 2.

All chips forming a P-side and, respectively, an N-side functional group, e.g T 1, T 2 and their FWDs and Clamp diodes (CLDs) and T 3, T 4, their FWDs and the CLDs, respectively, for the N-side are located on one AlN ceramic substrate for



Figure 1: Opened three-level IGBT module



Figure 2: Three-level IGBT module topology including circuitry



best thermal conduction. The internal layout, power chips and the thermal profile in a sample module has been analysed by thermograph and baseplate temperature sensors under varying load.

Three-level NPC topology and short circuit detection

The outer switches (IGBT 1 and IGBT 4) are equipped with a real-time current controller (RTC), a unique technology utilising a fraction of the collector current to detect an over-current situation and to force the IGBT into a current controlled desaturation. The principle of the RTC and its location on the substrate is shown in Figure 3. Basically, the aforementioned fraction of the collector current is flowing through the shunt resistor (inside the red dashed line of Figure 3) and creates a voltage drop accordingly. The following comparator pulls down the Gate Emitter voltage (V_®) when the reference voltage level (Vref) is exceeded by shunt voltage drop.

A similar circuit has been used in previous generations of Intelligent Power Modules (IPM) for more than 10 years to control the desaturation current level precisely, and has been adopted here for an IGBT module the first time. As a result, the comparatively low current level reduces the stress on the IGBT during a short-circuit situation. Such a stress reduction improves the reliability of key applications like PV inverter and UPS. The increase of MTBF is a key objective for UPS applications where power quality and availability, as well as a long lifetime, is a main target for PV inverter. The inner IGBTs (2 and 3) are lacking this RTC, leading to a higher desaturation current. Hence, the module provides an essential feature to efficiently protect a three-level inverter system in short-circuit situations, as the described deliberate implementation of RTCs at IGBT 1 and IGBT 4 ensure that inner IGBTs (IGBT 2 and IGBT 3) would never desaturate before the outer ones. This feature of the three-level IGBT modules is

simplifying the gate driver and the connected fault detection logic usually being implemented into a programmable logic device.

Power loss calculation approach

The thermal evaluation has been done by the modelling of the device and the characterisation of loss parameters like switching and conduction losses as a function of their influencing parameter. With this device data and the knowledge about the commutation in a real inverter operation, it becomes possible to perform a loss simulation for the specific operation conditions which are considered typical for PV-inverter or UPS operation.

In three-level NPC configuration, the



substantially higher and leads to a more complex way of calculating loss for the individual FWD/CLD or IGBT chip. The value and the direction of the current, in conjunction with the output voltage represented by a pulse width modulated (PWM) signal and their phase angle in between, are the input parameters of the loss calculation approach. Additionally, the chip inherent loss dependencies:

number of commutation paths is

- $V_{ce(sat)} = f(I_c, T_j)_r$
- $V_F = f(I_E, T_j)$,
- Eon, Eoff, $E_{rr} = f(I_c, R_G, V_{cc}, T_j)$

have to be taken into account, where Vce(sat) is the saturation voltage, Ic is the collector current, Ti is the junction temperature of the chip and E_{on} , E_{off} are the switching energies to turn on or off the device and Err to recover the incorporated diodes respectively.

R^G represents the connected gate resistance and V_{cc} is the DC-link voltage. An arbitrary combination of voltage and current and their phase angle between them needs to be considered when performing the loss calculation (Figure 4). In the example during the interval where current and output voltage are having equal polarity, the 'outer' IGBT (IGBT 1 or IGBT 4 respectively) together with their corresponding clamp diodes are switching/ recovering while the inner IGBTs (IGBT 2 and IGBT 3 respectively) are only having conduction losses as a function of the





Figure 5: Black painted chips



actual output current polarity. In the same way, the active components and their individually imposed loss must be identified in the remaining intervals to perform a calculation over one cycle and hence getting an image of the total loss inside the module.

In reality, the voltage waveform is usually established by a PWM signal, which is adjusting the (fixed) DC-link voltage to the mean output voltage value of the switching instance by the applied duty cycle 'D'. If the thermal simulation is done in this precise way, pulse by pulse, the calculation of total loss becomes simple by summarising the loss per switching instant or pulse 'p'.

With t1= ϕ and t2= π , this specific calculation for T1 can be performed according to equations 1 - 5 considering Pss steady state or conduction loss and Psw switching loss.

1)
$$p = pulse$$

- 2) $P_{T1}(p) = P_{SS_T1}(p) + P_{SW_T1}(p)$
- 3) $P_{SS_T1}(p) = \overline{i}(p) \cdot V_{CE_sat}(\overline{i}(p), Tj(p-1)) \cdot D(p)$
- 4) $P_{SW_T1}(p) = E_{SW}(i(p), V_{cc}, R_G, Tj(p-1)) \cdot fc$

5)
$$\overline{P_{T1}} = \frac{1}{T} \int_{t1}^{t2} P_{T1} \cdot dt = \sum_{p(t1)}^{p(t2)} P_{T1}(p) \cdot \frac{1}{T}$$

Loss calculation in PV-inverter and UPS especially for the front end portion of the UPS (3 ~ PFC) are quite simple because of a simplification of the interval situation. Assuming sinusoidal shape of current waveforms, the calculation can be performed according to the aforementioned equations. The correctness and the precision of such a loss calculation is checked to allow a tuning of parameters to reach a good matching between simulation and reality. Hence, a precise measurement instead of simulation of loss under realistic conditions provides the required precision for a simulation tool. For this purpose, a back-to-back configuration of inverters has been developed that is able to perform a circulation of power. Hence, the specific conditions found in PV-inverter operation and 3 ~ PFC operation can be created easily, helping to investigate on the thermal behaviour and evaluate the performance of two- and three-level IGBT modules.

Load generation test set-up

Before applying the realistic application conditions the setup consisting of the IGBT module and the heatsink was prepared and calibrated. For this purpose the device under test (DUT), a 75A three-level IGBT module CM75YE13-12F, has been equipped with various thermocouples mounted into the baseplate just under the specific IGBT or diode chip. Moreover, the gel has been removed from the module and the bare chips have been coated by a black varnish with known emission coefficient. Figure 5 shows the result after the coating.

In order to acquire the thermal resistance from junction to the baseplate for each chip precisely a DC current test has been performed, which is powering all available IGBTs by one current source and the DUT by a separate current source to create realistic temperature gradients in the module's baseplate. As a result of the chosen set-up, two entire legs are powered by one current source and the positive/ negative part of the leg where the DUT is located is powered separately. At the DUT, along with the precise DC current measurement, a Veccent measurement is performed on chip level (Figure 6).



Figure 7: Thermal investigation by a set of two inverters which are circulating the power

The thermocouple touching the baseplate just under the chip and the infrared camera is observing the black painted surface of the IGBT/FwDi chip. The DC-loss of this selected operation point is well-known and the thermal resistance can be determined by linking power loss and temperature rise by means of the thermal resistance, according to the well known equation 6:

$$P = \frac{T_j - T_c}{R_{th(j-c)}}$$

The thermal investigation has been performed by a set of two inverters which are circulating the power. Figure 7 reveals the configuration of the experimental testbench which allows the setting up of arbitrary operation conditions for the power stage by a digital control of DC-link voltage, switching frequency load currents, PFC/ inverter mode and current phase angle. Hence, the loss distribution inside the IGBT module can be shifted and the corresponding individual chip temperature observed accordingly.

Application conditions for PV-inverters

IR images of typical operation conditions for PV- inverter, e.g. $\cos(\phi) = 1$ and modulation index variation of 0.5 to 1.0, PFC operation and also mixed conditions with highly capacitive or inductive load have been tested. The case presented below shows the typical operation under PV conditions operating at the following application parameters:

- $V_{CC} = 750V$
- $\hat{I} = 50A$
- modulation ratio = 69%
- $cos(\phi) = 1$
- $f_c = 10 \text{kHz}$
- f_° = 50Hz
- $T_f = 65^{\circ}C$

By the interpretation of the thermal image and considering the corresponding baseplate temperature of the chip, the power loss can be calculated according to equation 6.

From the IR image (Figure 8), the absolute temperatures can be easily read out and it becomes clear that in this operation, as already described in the power loss calculation approach, thermally the outer IGBT T1 is the bottleneck. The FWDs are not taking over any load as Figure 8: IR image indicating the absolute chip temperatures



Figure 9: Chip temperatures at $cos(\phi)$ variation

theoretically already understood. Hence, the colour of the IR image indicates a substrate temperature accordingly. It is remarkable that, in this operation, the clamp diode (clamp) is thermally only slightly loaded despite the small modulation index of only 0.69. With respect to PV-applications, it is an indication of a conservatively selected chip size inside this three-level IGBT module.

Furthermore, a qualitative result on the junction temperature change as a function of varying phase angle between current and voltage explains that the set-up of chip sizes inside a module can be optimised for certain operation conditions. The shift of load reflected in the thermal dissipation as a function of the $\cos(\phi)$ is indicated in the IR images shown in Figure 9. For all of these tests, the amplitude of the current and the modulation index have been kept constant, but they are different compared with the previously measurement results. Referencing to the naming convention, according to Figure 2, all measurements have been taken out of leg V and D1 is the FWD to T1 and Dc1 is the CLD of the positive part of the leg.

From these images, it can be understood

	calc.∆T(j-c)	meas.∆T(j-c)	Error
IGBT T1	34.4K	34.7K	0.3K
IGBT T3	20.2K	20.1K	-0.1K
FWD D4	ОК	-0.4K	-0.4K
Node CIDi	13.2K	13.0K	-0.2K

Table 1: Temperaturerise ΔT (j-c) resultscalculated versusmeasured results

that the lower the $cos(\varphi)$ is the lower the power loss in T1 gets. T2 shows a quite stable dissipation under all these changing conditions. However, the origin of this power loss is changing: While in the case of $cos(\varphi)$ = 1 T2 is mainly heated by conduction loss, the situation at PFC operation ($cos(\varphi) = -1$) is changed to a mixture of (less) conduction loss but more switching loss.

The differences indicated as ERROR between real measurement and simulated results are very small. The results presented in Table 1 show a good match.

Conclusion

The inverter and the control structure according to Figure 2 has been calibrated and successfully commissioned to generate realistic test conditions for the optimisation of two- and three-level IGBT modules. IR images and the analysis of the corresponding loss information has led to the conclusions regarding the suitability of the chip set-up of the suggested three-level IGBT module under PFC and PV-inverter operation with varying power factor. The results show the potential hotspots inside a three-level IGBT module depending on the actual load conditions and allow for optimising a loss simulation tool.

Literature

'Three-level Trench Gate IGBT modules with IGBT and their thermal analysis in UPS, PFC and PV operation modes', published at EPE 2009 -European Conference on Power Electronics and Applications, Barcelona, 8-10 September 2009

Intelligent Doping Leads to Success

Switched power supplies are everywhere today; it is the only technology capable of delivering high efficiency. Power factor correction supposedly can keep sine wave distortion and noise low in the power grid, but also creates additional power losses. New, specially designed Silicon diodes can reduce the costs for such circuitry easily. **Wolf-Dieter Roth, HY-LINE Power Components, Unterhaching, Germany**

Diodes are the first semiconductor component being implemented in industrial processes starting with the galena crystal detectors of the early radio industry. Then came selenium rectifiers, germanium diodes and transistors, silicon components from diodes up to microprocessors, Gallium Arsenide (GaAs) amplifiers and light emitting diodes, Gallium Nitride (GaN) and silicon carbide (SiC) semiconductors and finally Schottky barrier semiconductors, coming up with a barrier between semiconductor and metal, thus somehow closing the circle back to the crystal detector.

New semiconductor materials offer exciting physical characteristics, which make new devices like the blue LED possible. But new materials also implement a new learning curve in production, leading to high prices and higher failure rates when production of a new semiconductor starts. Sometimes later as well: GaAs semiconductor components never really became mass market - the material is still too expensive and difficult to process compared to silicon.

An interesting strategy thus is to improve today's standard semiconductor processes with clever constructions: Gigahertz amplifiers, which once could only be realised in GaAs technology, are built on a standard silicon wafer nowadays. Similarly, attributes once only associated to SiC components may now also be realised in plain silicon semiconductors, which is not only saving money, but also offers more robustness. An example for this are the Qspeed power factor correction diodes offered by HY-LINE Power Components (see Figure 1).

High efficiency and poor power factor

Switched mode power supplies (SMPS) are a big step-up from the classical setup of a 50/60 cycles transformer, rectifier and

Figure 2: Block diagram of the front rectifier of a switched power supply with PFC circuitry



Figure 1: Qspeed-HY-LINE PFC diodes are optimised for PFC applications

linear regulator. They offer higher efficiency, smaller volume and weight, plus smaller idle losses. However, a problem for the power grid remains: their output is gained from inverting, transforming and rectifying of a DC voltage that is derived directly via diodes from the mains, without the damping and linearising effect of a conventional mains transformer being put in-between.

Instead of the continuous draw of a resistive load or the phase shifted, but still

continuous draw from capacitive or inductive loads, a rectifier with a following load capacitor will cause a pulse draw. The mains will only be loaded at the voltage peak to recharge the capacitor - power factor is low. The result: In offices with a lot of personal computers or in computer centres the sine wave of the mains voltage will be cut off thus leading to harmonics in the mains; also the pulse currents will lead to higher wire losses. Finally the missing sine wave peaks will result in lower voltage





at the charge capacitors in the power supplies.

Power factor correction (PFC) circuits (Figure 2) normally use an additional stepup converter (boost) as a front end, which delivers current to rectifier and charge the capacitor continuously through the whole current phase instead of only at the peak. Thus problems with harmonics and line overload will be reduced, as long as the PFC circuit does not create any harmonics itself, but efficiency will still suffer slightly, even though the mains is used more efficiently, due to the fact that now a second converter is in use. It is important to make the PFC converter as efficient as possible to not devaluate the power factor correction

One key component next to the inductor is the diode used in the PFC circuit: it has to switch fast, but not too rough, and must have a low reverse recovery charge QRR. Often SiC

semiconductors are used for this, but their Q_{RR} is sub-optimal.

Speed is not always sufficient

Qspeed's diodes (Figure 3) for PFC applications are offering forward voltage, reverse voltage and -current, plus speed similar to much more expensive SiC diodes, for a price only slightly above that of ordinary silicon high speed (ultra fast) diodes.

These diodes have far less EMI problems compared to standard hardswitching platinum-doped "ultra fast" diodes due to "soft recovery", they are an excellent choice for PFC applications operating directly on mains power, where all kinds of electromagnetic interference due to hard switching slopes can immediately spread into the grid.

Qspeed diodes offer up to 5% more efficiency compared to conventional silicon "ultra fast" diodes, reduce MOSFET



Figure 3: Internal structure of a Qspeed diode

temperature of 5 to 20K due to their lower reverse recovery charge and deliver better EMI performance. If those advantages are used to use the next smaller MOSFET size, overall costs will stay the same or even drop while efficiency is still higher due to the fact of easier filtering. The efficiency of a power supply using PFC rises up to almost a whole percent point if Qspeed diodes are used (Figure 4).

Robust CMOS wafer technology

Currently, Qspeed's diodes are available up to 600V / 20A or 300V / 30A and also as a dual unit. However, it is not a good idea to choose a diode of larger size than the circuit really demands. Diodes with higher voltage or current reading will also have a higher charge that has to be dissipated when reversing polarity (reverse recovery charge). Thus efficiency would drop. Also, bigger diodes would of course cost more. As a rule of thumb for choosing the right diode the manufacturer recommends around 1A per 100W of the power supply rating.

Some characteristics of silicon diodes will work against each other. If the semiconductor wafers are heated longer when doping them, foreign atoms may diffuse stronger into the material, thus lowering the forward voltage V_F but rising Q^{RR} . Qspeed diodes are optimised for low Q^{RR} .

The real secret of the patented technology lies within the internal semiconductor structure of the diodes. They use 0.3µm CMOS technology and offer Schottky barriers as well as standard p-n barriers. To achieve this, p doted cones oriented to the cathode are placed in front of the Schottky barriers around the anode. When polarity changes, the Schottky junctions will conduct first and offer a low forward voltage, whereas the p-n junctions switching on later when current flow sustains enable highest current densities. In reverse mode, current will be blocked quicker and better: Whereas normal Schottky diodes suffer from high leakage currents, trench technology used in Qspeed diodes will generate additional areas of low carrier density around the p cones that will spread up to the Schottky barrier thus clearing it of carriers. This will stabilise the semiconductor and reduce leakage currents significantly, which would be up

Figure 4: Increase in efficiency from normal ultra fast to Qspeed diodes in a PFC power supply using 100V input voltage and delivering 840W output power



such strong ringing that damping with RC elements becomes necessary to prevent the components from being destroyed by going over their maximum reverse voltage, Qspeed diodes do not suffer from ringing even without damping, which raises efficiency up to 2%. Also their temperature behaviour is much better (Figure 6). Up to 105°C Qspeed diodes outperform even SiC!

At first glance, Qspeed diodes may cost a bit more than simple ultra fast diodes. But those costs are offset by using a smaller MOSFET. Lower costs and higher reliability also result by eliminating EMI filter components. Additionally, more efficient circuits may be used: Instead of using DCM - discontinuous conduction mode - common in current designs, wanting to keep high losses low that result from diodes with high QRR by reversing charges less often, CCM - continuous conduction mode - may be used, which offers simpler regulation circuitry and lower switching currents. This way, completely new designs with high efficiency and compact size become possible.



diodes are not limited to power factor

correction. In standard rectifying circuits,

their soft switching is also an advantage.

to a few ten milliamperes with diodes of this size otherwise.

Schottky and p-n combined

Another advantage of Qspeed diodes is their size. SiC is efficient, but also expensive, so SiC chips are kept very compact. An overload - no matter how short - can easily destroy the diode. Qspeed diodes on the other hand, use bigger chips, which is affordable in standard silicon technology, thus offering the robustness of a classical 2N3055 power transistor. Therefore, there is plenty of headroom to design them for an average current, rather than peak current, surviving spikes and transients without problems. Still, they are fast enough that power supplies with these diodes can run at 65 up to 100kHz, thus reducing size and cost of inductors.

Of course, the capabilities of the new

Figure 6: QRR with rising junction temperature at SiC (red), ultra fast (black) and Qspeed diodes (blue)

When "ultra fast" diodes would produce **Qrr versus Junction Temperature** 70 I OAOSTC600 UUF Silicon Silicon Carbide 60 50 40 30 20







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