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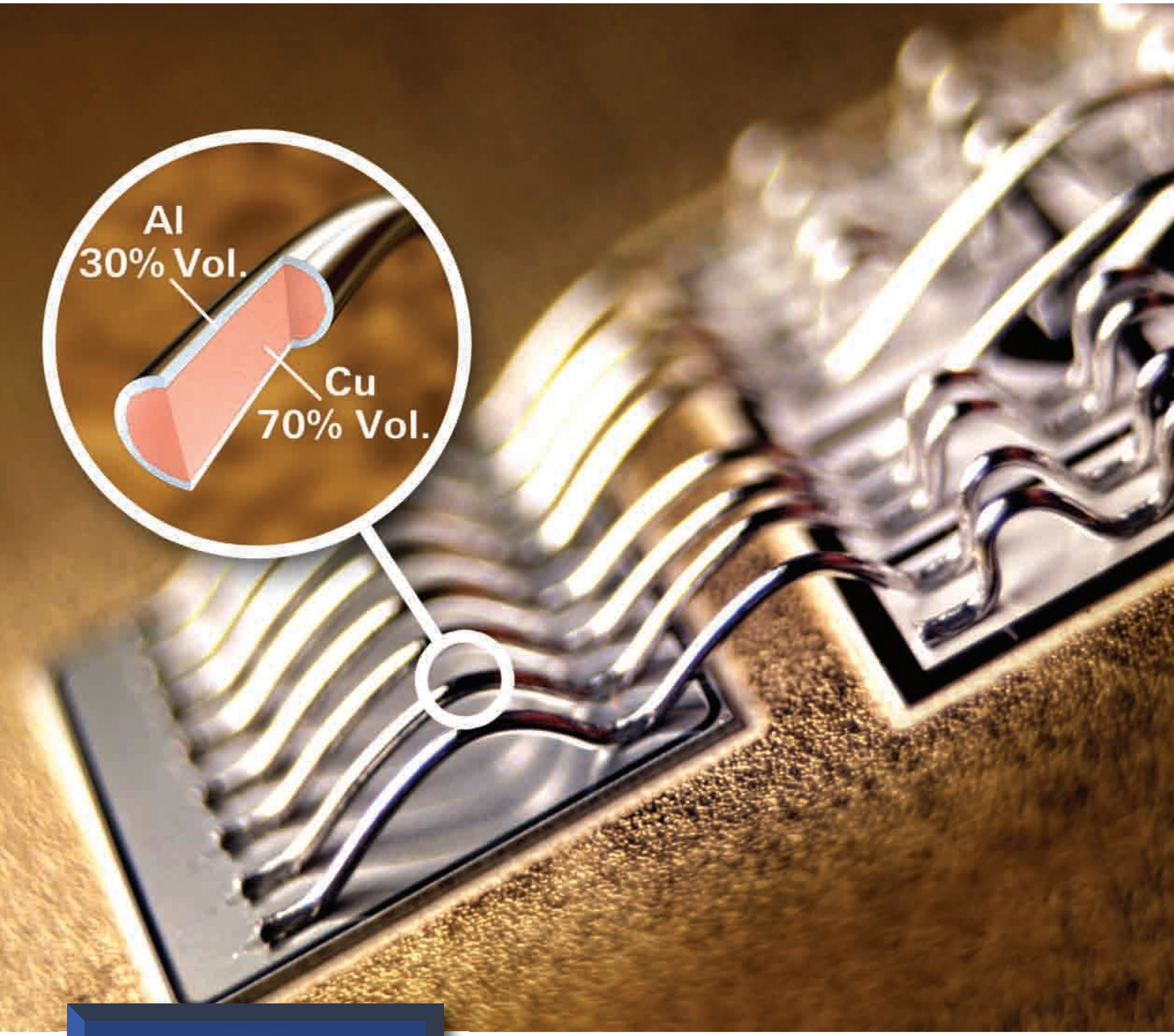
POWER MODULES

Extension of Operation Temperature Range to 200°C Enabled by Al/Cu Wire Bonds



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Market News

PEE looks at the latest Market News and company developments

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PCIM 2012 Report

COVER STORY

Extension of Operation Temperature Range to 200°C Enabled by Al/Cu Wire Bonds

Device manufacturers have announced the extension of the maximum junction temperature to 200°C in the next generation of IGBTs. The demand for an extension of the operation temperature range has been promoted by several trends: Firstly, the use of the combustion engine cooling system for cooling power electronic components in hybrid passenger cars requires an extension of the maximum junction temperature since the cooling liquid temperature can be as high as 110-120°C. Secondly, the wide bandgap materials like SiC and GaN are capable of high temperature operation and therefore demand for a packaging technology for higher operation temperatures. Last but not least, the higher current capability provided by the extended temperature range increases the power density without additional improvements of the power electronic system. However, this extended temperature range can only be utilized when accompanied by a significant enhancement of the package reliability. Al-clad Cu wire bonds together with Ag sinter technology have the potential to achieve this goal. Full story on page 18.

Cover supplied by SEMIKRON Elektronik, Nuremberg, Germany

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Ultra Low On-Resistance SIC Trench Devices

A new generation of Silicon Carbide (SiC) planar MOSFETs, trench structure Schottky diodes, and trench MOSFETs has been developed. The planar SiC MOSFET technology suppresses the degradation of the parasitic PN junction diodes even if forward current penetrates into the diodes. The trench Schottky diodes exhibit lower forward voltage than conventional SiC diodes while keeping leakage current at an acceptable level. And SiC MOSFETs with a double-trench structure improve reliability of the device while maintaining ultra low on-resistance because the new structure effectively reduce the highest electric field at the bottom of the gate trench, thus preventing gate oxide breakdown. **K. Okumura, N. Hase, K. Ino, T. Nakamura, and M. Tanimura, Rohm, Kyoto, Japan**

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Silicon Carbide BJT's in Boost Applications

Efficiency is becoming more and more important as well as size and cost. In boost DC/DC converters, typically used in PV inverters and PFC circuits, increased switching frequency makes a big impact on both size and cost. Silicon Carbide (SiC) bipolar junction transistors (BJT's) offer low-loss high speed switching combined with low conduction losses enabling higher switching frequency and maintaining high efficiency. SiC BJT's combine the best properties from Silicon unipolar and Bipolar technologies in a normally-off device. The design and performance of a 1kW boost circuit based on the SiC BJT is presented in this article. **Peter Haaf and Martin Domeij, Fairchild Semiconductor Germany and Sweden**

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SiC MOSFETs under High-Frequency Hard Switched Conditions

Silicon carbide (SiC) MOSFETs enable lower system costs by providing the ability to increase power density and frequency of operation, thereby reducing the size, weight and complexity of the system. The first commercial SiC MOSFET was released by Cree in early 2011 and initial demonstrations of its high frequency capability were presented at PCIM 2011. In this article results that make direct comparisons of the SiC MOSFET to Silicon (Si) MOSFETs and IGBTs are presented which show the large reduction in switching losses in the SiC MOSFETs. **Bob Callanan and Julius Rice, Cree Inc., USA**

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Wide Bandgap Power Devices in Megawatt Applications

Although researched for many decades, it is only recently that wide bandgap power devices have started to achieve an acceptable market entry level in terms of overall performance competitiveness in special applications with relatively lower power ratings. Therefore we will discuss the status of SiC in particular in connection with Megawatt applications and we will compare the potential benefits and challenges of introducing SiC technology. We will also discuss the widely proposed Si IGBT and SiC unipolar diode hybrid solution at 1.7 kV including experimental results and some important challenges to the acceptance of this concept in MW applications. **Iulian Nistor and Andrei Mihaila, ABB Corporate Research; Munaf Rahimo , Liutauras Storasta and Chiara Corvasce, ABB Switzerland Ltd., Semiconductors**

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Product Update

A digest of the latest innovations and new product launches

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Website Product Locator

New Horizons for Power Semiconductors

Driven by energy-efficient industrial and renewable energy applications, the demand for power semiconductors has been increasing rapidly. Hence, the longer-term prospects of the global power semiconductor market are very positive with forecasts showing 50 % market growth to $24.0 billion by 2015. In particular, the power module market has seen a tremendous growth, driven primarily by industrial motor drives, renewable energy, hybrid and electric cars, and consumer electronics. Though there are ups and downs this is an impressive figure. Thus PCIM 2012 has closed with record numbers in terms of exhibitors, exhibition space, visitors and conference delegates. And PEE was part of this event, particularly with our Special Session on SiC and GaN applications. Though since 20 years in discussion SiC now is ramping up with higher current carrying MOSFETs and JFETs, incorporated in power modules from various manufacturers particularly suited for solar power applications. Some managers even expect SiC to become a successor of the IGBT and invest in this technology along with drivers. Why that? SiC is the key material for energy saving in power electronic applications. The breakdown voltage is ten times higher than Silicon. Significant power loss reduction of a power device is possible with this feature. SiC also provides benefits in conduction losses for low frequency applications at very high voltages by avoiding the need for series connections of lower voltage Si devices. Similarly SiC is extremely suitable in applications at very high frequencies and low power levels due to the extremely low switching losses. Some new aspects are starting to “change the game” compared to the situation of the industry just a few years back. For example, most of the SiC technology developments were focused in the past either at voltages around 600V-1200 V or above 10 kV. Today a development trend towards voltage levels of 1200V and 1700V is on the way, where many interesting applications for MW levels can be identified. And the role of SiC have been underlined by awarding Japanese SiC semiconductor manufacturer Rohm with the PCIM best paper on double trench SiC MOSFETs. At the exhibition the company also showed full SiC modules.

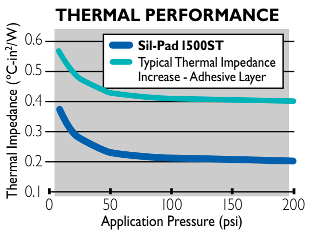
This trend also indicates that a certain performance/cost level is difficult to reach for SiC technology at voltages below 1200 V, where the competition is fierce from upcoming GaN on Si technologies. GaN gained more interest due to new nature and additional market entrants also in wafer processing or foundry services. This market need to be provided at competitive cost, which leads to the decision to use standard large diameter Si wafers as a substrate. This decision comes with the constraint that the required GaN epitaxy is mechanically more strained compared to competing substantially more expensive substrates like Sapphire or SiC. On the one hand the utilization of large diameter substrates is a prerequisite to keep the process cost low. On the other hand the mechanical strain of large diameter GaN-on-Silicon is the main challenge for the commercialization process. Generally speaking, the lattice mismatch between GaN and Si cause crystallographic defects, which are partly electrically active. On Si wafers the isolating GaN layer thickness is defining the maximum application voltage of the devices processed on such wafers. Today 4-inch GaN-on-Silicon wafers with the appropriate epi layer thickness are available, which make 600V devices feasible. The material quality improvement in 6-inch GaN-on-Silicon is a matter of homogeneity progress in the epi quality and thereby a matter of yield improvement to switch to 6-inch utilization.

GaN normally-on switches combined with low voltage Si MOSFETs provide all required function blocks to set up an efficient high voltage solution. Asresult of such a mini module, cascode or cascade, normally-off switch and high voltage diode operation are available from various manufacturers such as International Rectifier, MicroGaN or Transphorm. The reason for this approach is the resulting time to market, similarly to normally-on SiC JFETs which are also cascoded to have a normally-off device. Thus GaN gained a lot of interest at PEE’s Special Session “High Frequency Switching Technologies and Devices for Green Applications” at PCIM. We will publish the presented papers of this session as well as the best PCIM paper (award sponsored by PEE) in this and upcoming issue(s).

Last but not least new die attach and bonding technologies for power modules leading to higher reliability, power density and temperature behavior are in intense discussion. Soldering or sintering, aluminum or copper bonds or a mix of both - that is the question. Our PCIM report and cover story give answers to this question. I hope you will enjoy reading raising your interest.

Achim Scharf
PEE Editor


OUR NEW TACK
TO SUPERIOR
DISPENSING.


THERMAL PERFORMANCE
Sil-Pad 1500ST
Typical Thermal Impedance Increase - Adhesive Layer
Thermal Impedance (°C-in²/W)
0.6
0.5
0.4
0.3
0.2
0.1
0
50
100
150
200
Application Pressure (psi)

New Opportunities with Power SoC

Hampton/USA-based privately held Enpirion introduced a new family of integrated 12 V DC/DC converters, so-called Power SoCs (power system on chip) capable of delivering output currents up to 15 A and designed for applications such as telecommunication, enterprise, industrial, embedded computing, and storage systems. The fabless company works closely together with Virginia Tech in integrating the passive components and with the Korean foundry Dongbu Hitek in integrating logic and power.

The EN2300 devices offer compact solution footprints from 4 A at 190 mm^2 to 15 A at 308mm^2 from an input voltage range of 4.5 to 14 V and an output voltage range of 0.6 to 5 V. Efficiency is up to 94 %. The PowerSoC technology integrates the controller, power MOSFETs, high frequency input capacitors, compensation network and inductor in a single package.

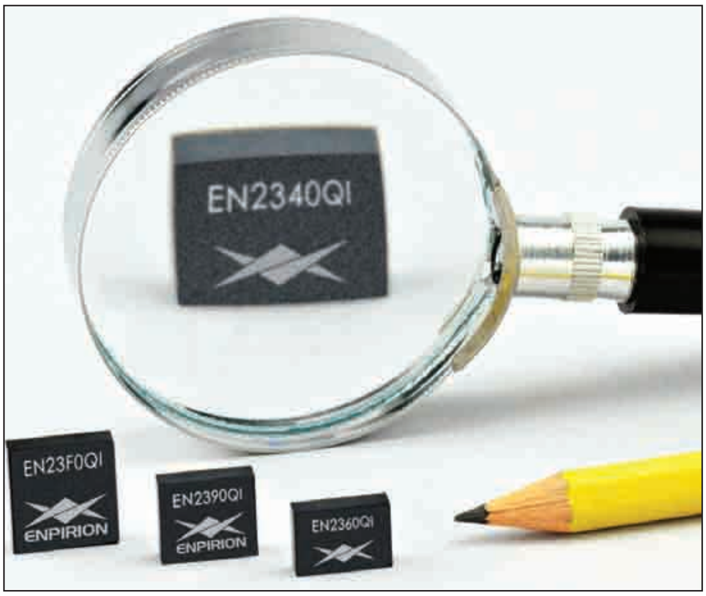
Challenges of integration

In power systems the most popular switches are Silicon-based MOSFETs. Non-Silicon options include SiC, GaAs and GaN switches. As the latter pose non-conventional manufacturing methods outside of mainstream foundry operations these will tend to be adverse to cost and integration goals. “GaN as a debated technology is suitable for voltages above 50 V, below that threshold Silicon cannot be beaten in terms of cost”, CTO Ashraf Lotfi pointed out. In Silicon there are three basic types of power MOSFETs: the vertical diffusion MOS (VDMOS), the trench MOS, and the lateral diffusion MOS (LDMOS). Among these the trench MOSFET has the lowest on-resistance but the highest gate charge, while the lateral MOSFET has the highest switching speed and CMOS integration.

The VDMOS and trench MOS are more suitable for low-frequency, high-current applications, while the LDMOS is more suitable for high-frequency, low-current applications. A lateral-trench MOSFET has the potential to apply at intermediate frequencies and currents. The gate-drain charge and on-resistance product (Q_{gd} x R_{dson}) referred to as the Figure-Of-Merit (FOM) characterizes the device performance. In general the trench MOSFET exhibits the highest FOM due to high gate charge, while the LDMOS has the lowest value. “That’s why we are focusing on lateral technology delivering low gate charge and thus a low figure-of-merit of 20”, Lotfi underlined. The chosen 0.18 micron LDMOS (CMOS) process normally uses 20 masking steps, two additional steps are required for the integrated power MOSFETs. “That is a different approach building up the structure in a mainstream fab compared to discrete power MOSFETs requiring up to eight masking steps”.

Another advantage of LDMOS is the availability of high-speed circuitry such as oscillators, flip-flops or PLLs which allow for high-speed control and thus fine resolution, Lotfi added. “For example, body diode conduction period in a 300 kHz power supply is around 50 nanoseconds, but with LDMOS this timing can be controlled down to 2 nanoseconds. And losses are proportional to that time!”

Another performance factor is the package parasitics. Different methods are used to connect the die to the pins; e.g., wire bonds or solid copper straps. These introduce parasitics such as the common-source inductance and the drain-side parasitic inductance. Both turn-on and turn-off losses will increase as the first increases, also the total switching losses are tremendously impacted. On the other hand, increasing the drain inductance will decrease the turn-on loss, but increases the



Enpirion’s new Power SoCs offer output currents up to 15 A and efficiency of 94 %

turn-off loss and so does not significantly influence the total switching losses.

Weak point inductors

All switching DC/DC topologies utilize at least one magnetic element to store and release energy at each cycle. The amount of energy stored in one switching cycle is inversely proportional to the operating frequency, the inductance of this element decreases inversely with operating frequency. Therefore it is possible to reduce the physical volume occupied by the magnetic material which forms the bulk of the size of a given magnetic device. "Moreover, the reduction in the size of the magnetics is the single largest contributing factor to the overall size of a switching converter, so the ability to reduce the size of the magnetics will have the most significant impact on achieving higher power density. But the core magnetic material have to work at elevated frequencies and have to be compatible with Silicon packaging, and this constraint has never been touched so far", Lotfi pointed out.

Among commercial materials, the operating frequency of amorphous magnetic materials and NiZn ferrites can be as high as 10 MHz. Besides these commercial materials, research aimed at developing new magnetic materials for high-frequency and integration applications is going on, such as granular film CoZrO, polymer-bonded materials, thin film alloys such as CoNiFe and amorphous FeCo alloys. At high frequency granular film CoZrO has the lowest core loss density, while NiZn ferrite 4F1 and the electroplated thin film alloy CoNiFe exhibit lower core loss densities. "We already have experimented in our lab with thin-film core materials running at 30 MHz having the same losses as traditional materials at 1 MHz", Lotfi said. And Power SOCs with integrated inductors running at 18 MHz are already in sampling stage.

"We are building up even the power MOSFET structure in a mainstream fab with two additional masking steps", Enpirion's President and CTO Ashraf Lotfi points out

A secondary energy storage element are the input and output bulk capacitors necessary to provide adequate filtering of AC components to meet specific voltage ripple requirements. Similarly the amount of bulk capacitance needed for a give ripple specification is inversely proportional to operating frequency. Therefore similar, but smaller, gains in bulk capacitor density are achievable with increased operating frequencies since parasitic equivalent series inductance and self-resonant frequencies limit the theoretical reductions in size.

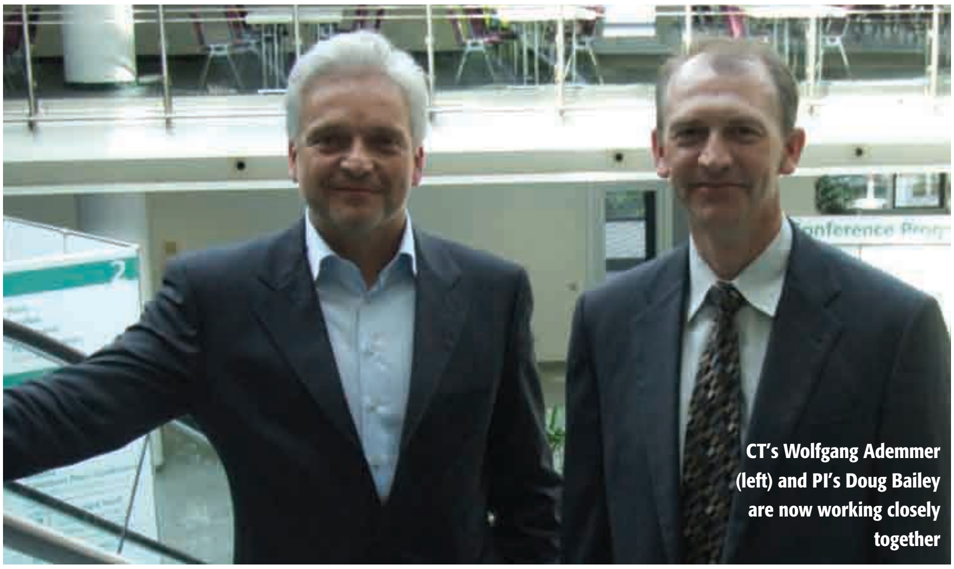
Finally in integrated power packaging is another pillar. Replacing a laminate substrate with a copper lead frame package is a first step. Magnetic die and LDMOS die are co-packaged in a standard multi-die assembly line. "In future the magnetic core, copper windings and LDMOS are fully implemented on a single wafer yielding a monolithic DC/DC converter", Lotfi promised. AS

www.enpirion.com

Power Integrations Moves Towards High Power

With recent investments in Silicon Carbide (SemiSouth) and IGBT drivers (CT Concept) Power Integrations prepares itself for the future. At PCIM we spoke with PI's Doug Bailey and CT's Wolfgang Ademmer about current and future activities

Power Integrations extends its portfolio towards more industrial applications rather than power supplies. In October 2010 the company invested $30 million in Mississippi-based SiC manufacturer SemiSouth, which includes an equity investment, a technology license and other financial commitments. Obviously the other financial commitments include the acquisition at a later stage. "We have the exclusive right to purchase them and we will use this option which will be triggered by profitability and some other parameters. With Silicon Carbide we were looking firstly on solving the efficiency problem in power supplies for servers and PCs, but we quickly found out that there is a far bigger market outside power supplies such as renewable energies. Realistically, SiC is the successor technology to the IGBT. Though the starting material is much more expensive, the efficiency gains are easy to monetize, especially in high-power applications such as solar and wind power generation", stated PI's VP Marketing Doug Bailey. Not only the higher switching frequency capability but also the possibility to use a 2-level instead a 3-level topology for the power converter requiring less components speaks for SiC.



CT's Wolfgang Ademmer (left) and PI's Doug Bailey are now working closely together

The most recent acquistion ($115 million) of Switzerland-based CT Concept AG gained more interest at PCIM. Founded in 1986, Concept develops drivers for high-voltage IGBT modules with 65 employees. The management team and employees will remain at the company's Biel headquarters, which will serve as PIs' center of excellence for high-voltage driver design. "That investment is a better way to use cash than putting it into a bank. But it is also a strategic investment, and the future transition to SiC requires appropriate drivers as well", Bailey said. "We will modify our existing technology to drive also SiC power modules, equipped with SemiSouth SiC JFETs", added Wolfgang Ademmer, who continues as president of Concept and became also a PI vice president. So far no change in management and brand name is planned.

According to Ademmer customers are looking particularly for the voltage scalability of Silicon Carbide even beyond 6.5 kV and having the high-voltage drivers in place this makes a nice fit. "When SiC is entering such applications, in example traction, the design on system level is substantially simplified, which in turn can justify the higher pricing of the devices, then we are in the middle of the game and can bring in our competence to that applications. So far we have a very broad customer base especially in the high-voltage arena, though there were not so many players in the past, but we are enabling new players to come into the game. The domain of switching high-voltage IGBTs has been reserved for the big players so far, but now we see a lot of new market entrants coming from China or South America. In general we are dealing with applications offering a volume of 100,000 drivers. A huge portion is happening in China where we enable companies to use high-tech from scratch - on system level".

Regarding the question of further investments in order to stimulate Concept's growth opportunities PI's intent is to grow the company as fast as the market grows, not as fast as CT's internal resources will allow. AS

www.powerint.com, www.igbt-driver.com

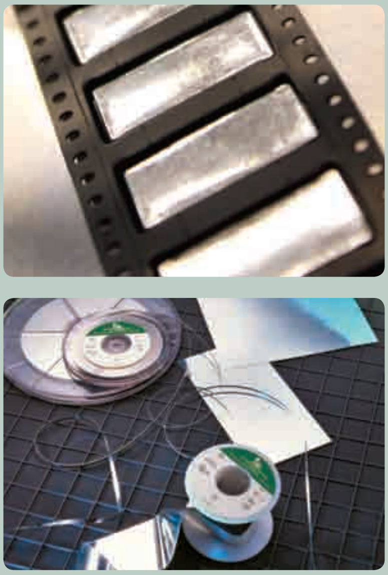
New CEO at Infineon

Dr. Reinhard Ploss will take over as new CEO of Infineon Technologies AG as of October 1, 2012. He replaces Peter Bauer, who is resigning from this position on September 30, 2012 due to health reasons. As a member of the Management Board, Dr. Ploss is currently responsible for Operations, Development, Technology and Human Resources. The new Operations department will relieve the Management Board - which will be reduced to three members - of important operational issues and simultaneously do justice to the major significance of Operations at Infineon. Ploss is with the company for over 25 years and presides over profound knowledge of the complex semiconductor industry. After numerous leadership roles in development and manufacturing, he assumed responsibility for Infineon's Automotive and Industrial units, encompassing products underlying the vast majority of Infineon's sales today. He was appointed to the Management Board in 2007.

Additionally Peter Schiefer will assume leadership of Operations. He will report to Dr. Ploss, and be responsible for the company's Manufacturing, Supply Chain and Purchasing activities. Schiefer will simultaneously give up his position as Head of the Power Management & Multimarket (PMM) Division, which he has led since January 1, 2012. As of September 1, 2012, the new Head of PMM will be Andreas Urschitz. As a member of the PMM management he is currently responsible for worldwide Sales, Marketing and Distribution of the division. He will continue these activities.

www.infineon.com

Dr. Reinhard Ploss will take over as new CEO of Infineon Technologies



SEMIKRON Innovation Award

Spanish research team comprising José A. Cobos, Oscar García, Roberto Prieto, Pedro Alou, Jesús A. Oliver and Miroslav Vasi_ from Univ. Politécnica de Madrid have been awarded the Innovation Award for their concept "RF Power Amplifier with Increased Efficiency and Bandwidth" at PCIM. The Young Engineer Award goes to Lars Lindenmüller of the TU Dresden for his research on the "Forced Evacuation Switch".

"The SEMIKRON Foundation merits innovations with considerable potential to deliver social benefits, such as the improvement of energy efficiency, conservation of resources, sustainability and environmental protection", said Dirk Heidenreich, CEO of the SEMIKRON Group, who presented the Innovation Award on behalf of the Foundation. The jury's decision to award the prize to the Spanish research team was based on the fact that their concept is instrumental in saving energy in base stations used in mobile communications systems such as satellite or mobile phones. This crucial technological breakthrough is based on a new switching topology featuring new power components in the power amplifier. This new solution will deliver a 30 % energy saving in comparison to conventional systems, which, if projected to the many mobile communications systems in use today, will lead to immense cost savings and reduced emissions. The innovation developed by Lars Lindenmüller is based on high-power medium- frequency resonant converters such as those used in intelligent power networks, renewable energy applications or high-speed trains, for example. In his converter topology, Lindenmüller uses high-power IGBTs, the losses from which could be significantly reduced using dedicated IGBT clocking and a demagnetizing network. Since in most of these applications the converter is in permanent use, this innovation results in an increase in efficiency and a significant reduction in carbon dioxide emissions.

Semikron's CEO Dirk Heidenreich (left) awarded Lars Lindenmüller, José A. Cobos, and Oscar García for outstanding innovations in power electronics

Mersen acquires Eldre

NEWBURYPORT/USA-based Mersen has completed the acquisition of Eldre as part of Mersen's strategy to support its partners in the development of power electronic applications with components that improve system reliability and safety. Eldre is based in Rochester/NY with European manufacturing in France (Saint Sylvain d'Anjou) and employs approximately 300 people.

The business will be integrated into Mersen's Electrical Components and Technologies segment.Mersen's expanded product offering combines product expertise in laminated busbar, cooling, and semiconductor fuses with application knowledge to maximize performance and balance cost.

The cooling systems are based on the principle that the efficiency of heat dissipation depends on the conductivity of materials used, the transfer surface between the heat transfer fluid and the dissipator, and the latter's heat transfer coefficient. The choice of design and dimensions of the dissipator also help to maximize the performance of a cooling system. Offered are air, fluid and phase-change (heatpipe) coolers.

www.mersen.com

SiC for Solar

Though Vincotech has been acquired around one year ago by Mitsubishi Electric, the Munich/Unterhaching-based power module company can operate independently using various chip sources and additionally can take advantage of the huge internal resources.

In 2010 the power business was accelerating throughout industry, Vincotech reported a 100 % growth. Sales in 2011 were $83 million, but the growth rate declined to 52 % and for the running year the figure will be even lower. "Nevertheless, more than 90 percent of our turnover is in power modules, we are well positioned to produce more than six million small and bigger power modules annually and we are broadening steadily our chip supplier base now including Mitsubishi, Fairchild, Cree, SemiSouth, Rohm or Infineon, to mention the popular names", said CEO Joachim Fietz at PCIM. "But, so far we have no access to Infineon's IGBT5 or .XT, though we have asked for".

Photovoltaics contributed with 200 % CAGR in 2011 very much to the business figures, but also motion control with 20 %. "The solar business is very volatile over the past three years, we experienced some quarters with almost zero business and another quarters accounting half of the turnover. At the moment were are approaching a deep valley and I can not give any comment on the near term. It's a crazy situation currently", Fietz stated. The company has reacted and offers now due to its modular approach application-specific solutions within four weeks lead time.

"Our major business today is in solar, but this is very volatile in these times", so Vincotech's CEO Joachim Fietz

For high-performance solar inverters up to 30 kW the company has designed a range of standard power modules in a flow 0 housing measuring 12 mm in height, featuring fast SiC switches from four manufacturers. These new products feature a 1200 V dual booster input stage and a 1200 V MNPC inverter. They also provide fast switching without tail current. High-frequency DC link film capacitors are on-board ensuring fast-switching, low-inductive designs and help minimize voltage overshoots. The MNPC topology has been implemented with split outputs to achieve high efficiency and immunity to shoot-through, cross-conduction current. MNPC modules are equipped with SemiSouth SiC normally-off JFETs, Infineon and SemiSouth SiC normally-on JFETs in cascode configuration as well as Cree and ROHM SiC MOSFETs. Dual Booster modules are equipped with SemiSouth SiC normally-off JFETs as well as Cree and ROHM SiC MOSFETs. "The cost difference is between 30 to 100 percent to a comparable Silicon module", said Werner Obermaier, Head of Product Marketing. "We prefer to pack more smaller devices in parallel into a module rather than big devices due to yield and cost reasons. And in the short term I do not see a demand for higher operating temperatures in such applications".

www.vincotech.com

GaN Foundry Services

RFMD, so far a supplier for RF power semiconductors, offers with its newest GaN process rGaN-HV substantial system cost and energy savings in power conversion applications ranging from 1 to 50 kW. It delivers device breakdown voltages up to 900 V, high peak current capability, and ultra-fast switching times for GaN power switches and diodes. RFMD will manufacture discrete power device components for customers in its Greensboro, NC/USA, wafer fab and provide foundry services for customized power device solutions. "We expect our newest GaN power process will expand our opportunities in the high-voltage power semiconductor market, and we provide access to rGaN-HV to our external foundry customers to support their success in the high-performance power device market", said Director Marketing GaN Power Daniel Schwob at PCIM.

www.rfmd.com

More Power for a Greener World

Regenerative and green energy sources will drive power electronics over the coming decades, this is the conclusion of many keynotes and presentations at PCIM 2012. The most important European power electronics event closed on May 10 with 263 exhibitors, 6.874 visitors and 744 conference delegates - the highest numbers recorded so far. Besides new semiconductor technologies and devices such as Gallium Nitride (GaN) and Silicon Carbide (SiC) new assembly and interconnect technologies for power modules gained a lot of interest.

More than 230 papers have been presented at the conference, out of this four outstanding papers were awarded for three young engineers and one for the best paper. The three Young Engineer Award winners received prize money, whilst the Best Paper Award winner received prize money and an invitation to the PCIM Asia 2013 Conference in Shanghai - the latter sponsored by Power Electronics Europe and Semikron.

The three winners of the PCIM Young Engineer Award were Johannes Kolb, Karlsruhe Institute of Technology, Germany for 'Operating Performance of Modular Multilevel Converters in Drive Applications'; Hari Babu Kotte, Mid Sweden University, Sweden for 'A ZVS Half Bridge DC-DC Converter in MHz Frequency Region using Novel Hybrid Power Transformer'; and Marek Siatkowski, University Bremen, Germany for the paper 'Construction of a High Force Density Linear Motor with a Passive Stator using Transverse Flux Technology'.

The winner of the Best Paper Award was Keiji Okumura, Rohm Co., Ltd., Japan, for the paper 'Ultra low On-Resistance SiC Trench devices'. This paper presented next generation Silicon Carbide (SiC) planar MOSFETs, trench structure Schottky diodes, and trench MOSFETs. The newly developed SiC planar MOSFETs have suppressed the degradation of parasitic PN junction diodes even if forward current penetrates into the PN junction diodes. Secondly, SiC Schottky diodes are attractive devices to reduce switching losses in high voltage applications. And SiC MOSFETs with a double-trench structure have improved reliability of the device while maintaining ultra low on-resistance due to the fact that the new structure effectively reduced the highest electric field at the bottom of the gate trench, preventing gate oxide breakdown.

This paper complemented PEE's Special Session 'High Frequency Switching Devices and Technologies for Green Applications' which focused on Gallium Nitride and Silicon Carbide application trends.

Renewable energies stimulate power electronics

The global electrical energy consumption is still rising and there is a steady demand to increase the power capacity. It is expected that it has to be doubled again within 20 years. "The production, distribution and use of the


BPA handover to Rohm's Keiji Okumura at PCIM 2012 opening ceremony by Semikron's Uwe Scheuermann (left), PEE Editor Achim Scharf and Scientific Advisory Board Chairman, Prof. Leo Lorenz (right)

“Superinductors”

That’s what engineers are calling our new ultra-low DCR power inductors

Superconductors pass current with virtually no resistance.

Our new XAL/XFL inductors do much the same. Their DCR is incredibly low: often half that of similar size parts.

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"Power electronics is playing an essential role when integrating renewable technologies like PV and wind energy systems into the future Grid structure", Frede Blaabjerg emphasized in his keynote

energy should be as technological efficient as possible and incentives to save energy at the end-user should also be set up. Two major technologies will play important roles to solve the future problems. One is to change the electrical power production sources from the conventional energy sources to renewable energy resources. Another is to use high efficient power electronics in power generation, power transmission/distribution and end-user application, where power electronics are changing from being a minor energy source to be acting as important power sources in the energy system", underlined Frede Blaabjerg from Aalborg University (www.et.aau.dk) in his keynote on 'Grid Integration of Renewables'.

The wind power has grown to a cumulative worldwide installation level of 200 GW with over 39 GW of newly installed wind power capacity in 2010. Now there are predictions that the installed capacity could grow one order of magnitude to 2300 GW by 2030, according to a study published by the Global Wind Energy Council and Greenpeace International. The worldwide penetration of wind power in 2010 was around 2 %. China was the largest market in 2010 with over 19 GW installed and in general EU, USA and China are sharing around one third each of the total market.

The most used generator type is changing from an induction generator to Permanent Magnet Synchronous Generators (PMSG), where a full scale power conversion (FSC) is necessary. However, the cost of permanent magnets are becoming a challenge for this concept. All wind turbine manufacturers are using a step-up transformer for connecting the generator to the grid. Today the DFIG is still dominating the market but in the future FSC is expected to take over.

The annual installation of PV power has increased to above 5 GW in 2005 to roughly 40 GW in 2010. The annual growth rate is still very high (>30 %) especially for the last four years. As in the previous years the vast majority of new capacity was installed in EU with Germany as dominating the market followed by Spain and Italy. The USA market is also growing fast. "The most progressing technology is wind power but PV power plants are also emerging rapidly now and the technology has the highest growth rate. The applications of power electronics in various kinds of wind turbine generation systems are showing that the wind turbine behavior and performance are significantly improved by using power electronics and will be able to enable a muck more flexible grid structure. Wind turbines are able to act as a contributor to the frequency and voltage control in the grid by means of active and reactive power control using power electronics. The same will be the case for PV power plants and the standards will be changing in the next years. Thus, power electronics is playing an essential role when integrating renewable technologies like PV and wind energy systems into the future Grid structure", Blaabjerg emphasized.

"Our new mAgic sinter materials provide novel interconnect solutions for DCB devices with operation temperatures above 150°C and enable designs with higher power density", stated Thomas Krebs, Head of Microbond Assembly Materials at Heraeus

Towards lower losses and higher operating temperatures

Power module manufacturers are faced increasingly with the challenge to deal with higher temperatures of 175°C or more for Silicon power chips inside the modules, SiC and GaN are capable for even higher temperatures. In a power module the chips are normally soldered on their backside to the substrate, usually direct bonded copper (DBC) via soft solders with melting points below 250°C. This die attach spreads the generated heat to the DBC and from that the heatsink. The electrical connections on the upper side of the chips are realized by ultrasonic bonded aluminum wires. Both die attach and bonding are becoming more and more the weak points for power modules in demanding applications such as transportation (hybrid electric vehicles) or renewable energies which call for long lifetime of the power electronics and thus for high reliability.

The melting point of today's soft solders used for die attach is between 183°C (SnPb) and 220°C (SnAg). As long as the (junction) temperature of the power chips is well below the melting point of the solder material the connection between chip and substrate is reliable, but an increase up to 175°C (standard for new IGBTs) or above leads to a significantly decrease of the solder interconnect stability and thus reliability. Early failures due to solder fatique or brittle fracture can occur.

This creates a demand for new interconnection materials that can fulfill the reqirements of higher temperature stability, thermal conductivity and increased reliability when compared to lead-free solders. For the die attach two techniques have been developed recently, silver sintering and diffusion soldering or bonding (the latter is used in Infineon's latest PrimePACK power modules).

New sinter materials for DCB power modules

Sintering of silver (Ag) particles comprises a silver powder applied between chip and substrate, which is pressed (> 40 MPa) under moderate temperature (> 250°C) to form a compact Ag joint. This low temperature joining technology (LTJT) provides high thermal and electrical conductivity as well as long lifetime of the modules at temperatures > 150°C. "However, design and process constraints currently hamper the quick implementation in production lines, because special sintering presses are needed and the process is not compatible with pressure and temperature sensitive dies", said Thomas Krebs, Head of Microbond Assembly Materials at Hanau-based Heraeus **(www.heraeus-contactmaterials.com)**. At PCIM the company introduced its new so-called mAgic micro-silver sinter materials (paste and adhesive) as an alternative for solder and LTJT materials in DCB power modules with operation temperatures above 150°C.

The sinter paste is formulated mainly with silver powder and solvents, it can be sintered with low or even no pressure. The resulting sintered joint is a porous structure of silver particles without organic residues, which are also sintered to the die and substrate surface. "This sintered structure ensures low electrical resistivity and high thermal conductivity as well as high adhesion strength. The high silver melting point above 960°C allows to raise the operating temperature to 150°C and more without the risk of joint degradation", Krebs stated.

The sinter adhesive consists of silver powder in a polymer matrix and are processed in a pressure-free curing step. The pores and open spaces in the resulting joint are filled with cured resin. "The sintered particles exhibit thermal and electrical conductivities comparable to solder, what enable the mAgic adhesive to be used in low to medium power DCB devices. Also the temperature stability is significantly higher compared to solders", Krebs pointed out.

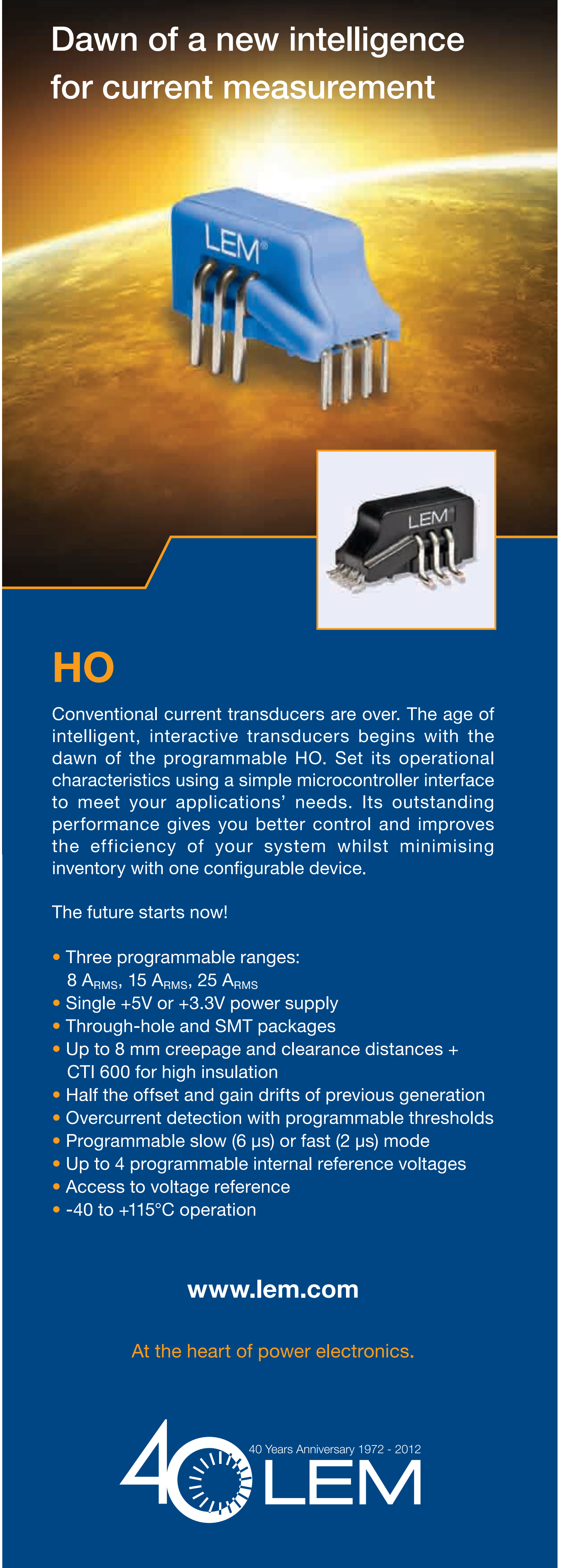
The pressure sintering process consists of paste printing, pre-drying at 60°C for up to 15 min, die placement in the dried paste and sintering at 250°C for up to 3 min in a press at 10 (LTS 043) to 30 MPa (LTS 016 paste). The total processing time is 15 to 20 minutes. Dies up to 100 mm_ can also been sintered in a convection oven with a defined temperature profile. "In contrast to LTJT sinter pastes our new sinter pastes can be processed in pressure assisted or even no pressure steps at low temperatures without drying channels for die sizes up to 100 mm_ on DCB substrates metallized with Ag and NiAu. The mAgic sinter materials provide novel interconnect solutions for DCB devices with operation temperatures above 150°C and enable designs with higher power density", Krebs concluded.

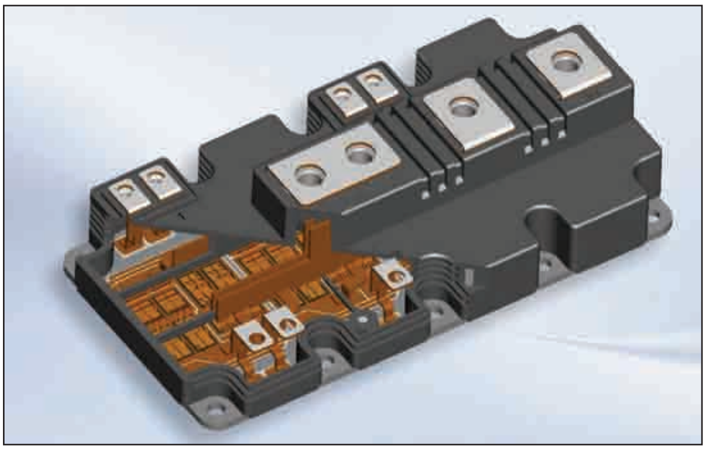
Diffusion soldering and copper bonding allows for higher temperatures

Infineon **(www.infineon.com)** follows the second alternative approach in which the phase formation reaction of the intermetallics during soldering is utilized to form a high melting point bond. "Depending on the process parameters the resulting joints consist of one or more intermetallic phases with melting points well above 400°C", stated Infineon's Head of Packaging Technology Karsten Guth recently. For the copper-tin (Cu-Sn) combination the joint can be realized by the compounds Cu3Sn and Cu6Sn5 which have much higher melting points and mechanical strength than Sn-based soft solder.

To create pure intermetallic joints with a remelting temperature greater 400°C a rapid solidification of Sn-Ag solder within seconds is applied. "The whole volume of low melting solder is consumed by the solidification process resulting in a high melting bond between chip and substrate. Depending on the ratio of the two different intermetallic phases, that are formed in the copper-tin system, the homologous temperature for these joints ranges from 0.50 to 0.69", Guth explained. Result is a 30-60 fold increase of the power

"We are in the final stage of qualifying our IGBT5 chips featuring .XT technology", Infineon's Division President Industrial Power Control (IPC) Helmut Gassel pointed out





First PrimePACK power module featuring IGBT5 and .XT technology **Source: Infineon**

cycling capability even for an increased junction temperature. “During our tests it appeared that the substrate layout sepcific influence on the heat distribution has got more impact on the module’s lifetime than the technology itself. Accordingly, both sintering and diffusion soldering are qualified to meet the requirements of next generation power module packages”, Guth stated. Diffusion bonding is one of the key technologies in Infineon’s so-called .XT technology, along with a copper layer on the top of the chip to allow copper bond wires instead of aluminum.

At PCIM 2012 Infineon’s Division President Industrial Power Control (IPC) Helmut Gassel introduced IGBT5 and .XT as the beginning of a new era in IGBT chip and internal packaging technologies. “We are in the final stage of qualifying our IGBT5 chips featuring .XT technology. First lead customers of our power modules already have received samples, volume production of PrimePack power modules featuring IGBT5 and .XT die attach and copper bonding techniques is scheduled for 2013. Also some external power modules manufacturers have been sampled with IGBT5 chips”, Gassel stated.

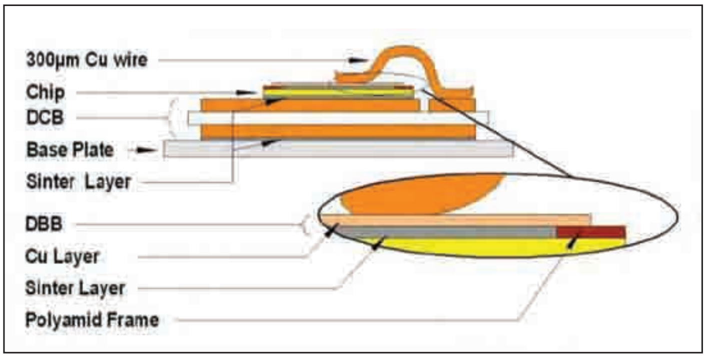
Besides diffusion soldering for the die attach copper bonding is the second major step in .XT for achieving higher reliability and power cycling capability of power modules due to the intrinsic lower electrical resistance and higher thermal conductivity of copper. “The copper finishing of the chip surface is a prerequisite for copper bonding, here we can look at a long track record of copper finishing of DCB substrates. Tests and simulation have shown that even under harsh environmental conditions this copper connections withstands corrosion. We will offer external power module manufacturers willing to implement IGBT5 chips the choice to use this advanced die attach and bonding or to stay with conventional aluminum bonding. The respective wafers will be supplied. All in all IGBT5 is qualified for operating temperatures up to 175°C, output power and power density increases by up to 25 percent or lifetime by a factor of ten. And last but not least .XT supports junction temperatures of 200°C”, Gassel concluded.

Copper bond contacts on sintered metal buffer

Danfoss Silicon Power **(www.danfoss.com)** follows a different approach. “Copper wire bonding maintains the design and process flexibility of the current Al wire bonding method but Cu wires demand a much more robust top metallization in order to protect the power semiconductor against chip crack and damage of the fine structures under the bond pad. In some applications, soldering of the die is successfully substituted by low temperature sintering or by diffusion soldering. The combination of a reliable die attach technique as well as a reliable top contact technology is a necessary and promising solution for significantly increased power module reliability”, explained Ronald Eisele, Prof. at University of Applied Sciences Kiel **(www.fh-kiel.de)** and Danfoss advisor.

The result is Danfoss Bond Buffer (DBB) technology, which mainly consists of a thin copper foil which is sintered onto the upper surface of the semiconductor. Sintering is also used to replace the soldering between the die and the DBC substrate. “The design of the DBB was dimensioned for the thermo mechanical optimum to reduce the mechanical stress due to CTE mismatch. In addition to the property during bonding to absorb energy and protect the die, the DBB also has thermal and electrical advantages. No silicon cracks after the DBB process were observed. The volume of the DBB forms a thermal capacity which has a positive influence on the thermal impedance. As the copper layer has a large cross-sectional area, which increases the vertical current flow, the DBB provides a uniform current density distribution in the semiconductor. Due to the improved vertical current flow, there is no mandatory need to place a stitch bond on the semiconductor", said Eisele.

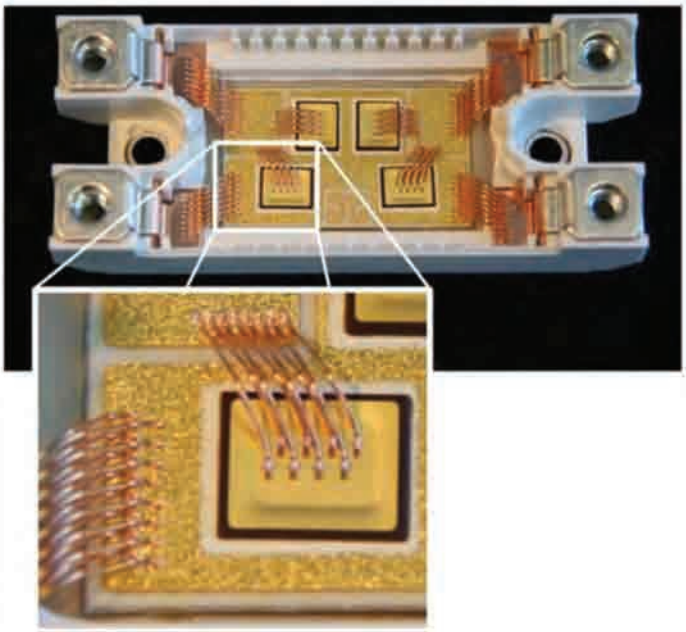
Through the integration of the sintering and the DBB technology the main weaknesses of the standard module were eliminated. The solder joint from the die to the DBC and the Al wires on the die top side were the main bottlenecks in the development of highly reliable modules. The DBB technology is applicable to a large number of standard semiconductors and allows flexibility of the layout due to the bonding technology.



Cross section of Danfoss Bond Buffer (DBB) technology featuring sintering and Copper bonding

DBB was implemented on a 400 V/150 A rectifier module for testing and benchmarking. The next step is the DBB-application on transistor layouts using a gate pad area and an emitter area (in case of an IGBT) in the same bond buffer. This will extend the beneficial properties also to the gate wire bond. IGBTs as well as MOSFETs are already under first examinations. Extreme current carrying capability can be enabled due to expanded wire cross sections up to 600 µm of each Cu wire.

An other approach using Aluminum-cladded Copper wires has been introduced by Semikron (see our feature 'Extension of Operation Temperature Range to 200°C Enabled by Al/Cu Wire Bonds').



DBB 400 V/150 A rectifier module

Speakers of PEE's Special Session in the final Q&A featuring MicroGaN's Ertugrul Sönmez (left), Cree's Bob Callanan, ABB's Iulian Nistor, IR's Michael A. Briere, and Fairchild's Peter Haaf

Focus on Green Applications with SiC and GaN

PEE's Special Session "High Frequency Switching Technologies & Devices for Green Applications" on May 9, 10.00 - 12.30 am focused on WBG (SiC and GaN) power applications. Around 100 delegates were interactively involved in the final discussion after all presentations, an outstanding feature for our PCIM Special Sessions over the past four years. Naturally GaN on Silicon received most of the attention due to its promises to be less expensive than SiC and its possible future capability of handling 1200 V, while SiC is in discussion for decades and thus more mature.

The papers covered "Efficient Power Electronics for the price of Silicon - 3D-GaN Technology for GaN-on-Silicon" by MicroGaN/Germany, "The Status of HV GaN based Power Device Development at International Rectifier", "Comparative High Frequency Performance of SiC MOSFETs Under Hard Switched Conditions" by Cree, "Silicon Carbide BJT's in boost applications" by Fairchild Semiconductor, and finally "Opportunities and Challenges for Wide Bandgap Power Devices in Megawatt PE Applications" by ABB. The presented papers can be found in this and the upcoming PEE issues.

Extension of Operation Temperature Range to 200°C Enabled by Al/Cu Wire Bonds

Device manufacturers have announced the extension of the maximum junction temperature to 200°C in the next generation of IGBTs. However, this extended temperature range can only be utilized when accompanied by a significant enhancement of the package reliability. Al-clad Cu wire bonds together with Ag sinter technology have the potential to achieve this goal. **Uwe Scheuermann, Product Reliability Manager, SEMIKRON Elektronik, Nuremberg, Germany**

The demand for an extension of the operation temperature range to 200°C has been promoted by several trends: Firstly, the use of the combustion engine cooling system for cooling power electronic components in hybrid passenger cars requires an extension of the maximum junction temperature since the cooling liquid temperature can be as high as 110-120°C. Secondly, wide bandgap materials like SiC and GaN are capable of high temperature operation and therefore demand for a packaging technology for higher operation temperatures. Last but not least, the higher current capability provided by the extended temperature range increases the power density without additional improvements of the power electronic system. However, the development of power electronic devices with a maximum junction temperature of 200°C must be accompanied by a significant increase of lifetime for the packaging technology. Applying classical lifetime models, this reliability increase must be in the range of a factor of 5.

Power modules for junction temperatures up to 175°C

The latest generations of IGBTs and freewheeling diodes are already rated for maximum junction temperatures of 175°C. This increase of 25°C with respect to the former traditional junction temperature limit of 150°C already required improvement of the packaging technology - the elimination of solder fatigue and the enhancement of Al wire bond reliability.

These improvements were implemented in the first 100% solder free module SKiM63/93 presented in 2008 [1]. Solder fatigue is eliminated by the architecture without base plate, which eliminated both the base plate and the base plate solder interface on the one hand and by replacing the chip solder interface by a Ag sinter diffusion layer on the other. This power module design requires a reliable pressure contact technology and spring contacts for the control contacts, both technologies have been validated in years of field experience. Additionally, the reliability of the Al wire bonds had to be improved to enhance the lifetime for 175°C maximum junction temperature. This was achieved by an optimization of the wire bond geometry. Increasing the loop height of the wire bond can significantly increase the lifetime during repetitive temperature swings in active power cycling tests [2]. While the reliability enhancement of Al wire bonds with increased aspect ratio (i.e., the ratio of loop height to the distance between bond stitches) is sufficient for maximal junction temperatures up to 175°, a further enhancement is required to fulfill the demand for an extended operation temperature up to 200°C.

Aluminum-clad copper wire bonds

Heraeus as a major supplier of wire bond material had started to investigate the use of composite materials for wire bonding already in the 1980s. The increase of the number of cycles to failure for Al-clad Cu ribbon bonds shifted this technology back into focus in 2007 [3]. Consequently, a technology development for fabricating Al-clad Cu wire bond material with a circular cross section was started at Heraeus.

Figure 1 shows a cross section of the Al-clad Cu wire bond supplied by Heraeus for this investigation. The material consists of 60-70% Cu by volume, which is equivalent to an Al layer thickness of 25-35 µm around a 230-250 µm Cu core for a 300 µm wire. The high fraction of Cu requires fine-tuned tailoring of mechanical

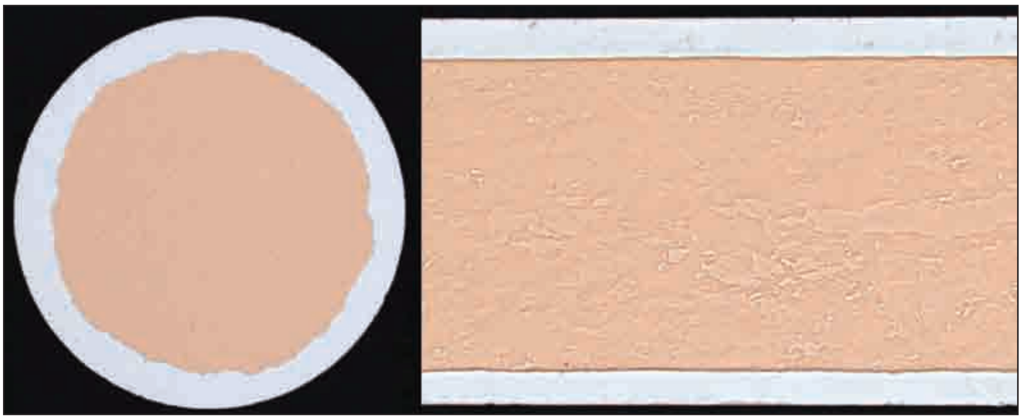


Figure 1: Cross section of an Al-clad Cu wire in radial and longitudinal direction

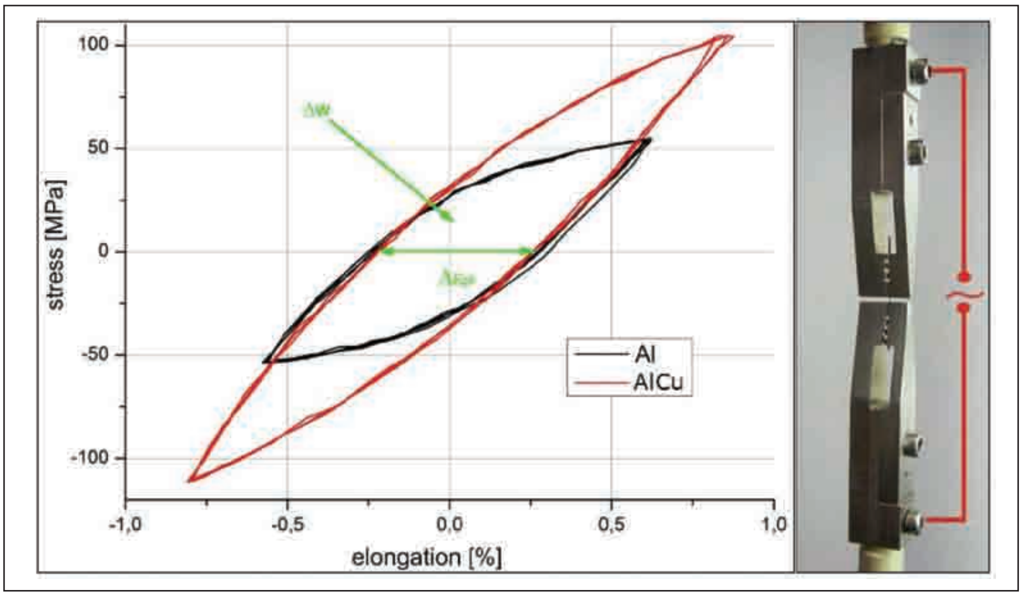


Figure 2: **Measurement of strain-stress characteristics of Al and Al/Cu wire material (left). Equipment detail for the uniaxial tests, the wire specimen is located between the holders (right)**

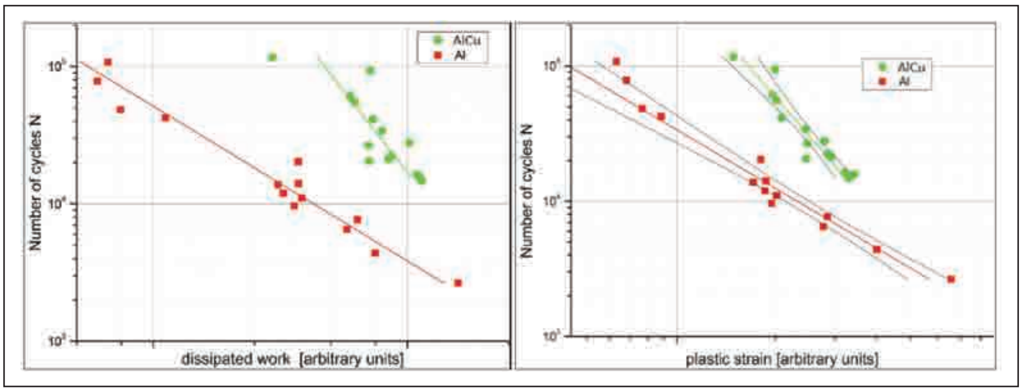


Figure 3: **S-N curve for Al and Al-clad Cu wire (type B) for plastic strain (left) and dissipated work (right)**

properties for different wire bonding applications.

For this reason two different versions have been tested: Type A is the robust version of this Al-clad Cu wire with harder Al material and higher yield strength. This material combination shows the maximum reliability in mechanical cycling due to high work dissipation capability. The full effect can be utilized in bonding on robust semiconductor surfaces or passive devices. Type B is the softer version of Al/Cu wire optimized for better bondability. With softer Al coat and lower yield strength type B provides a wider bond window and lowers the risk of chip damage. The mechanical cycling reliability is lower than for type A, but still expected to be higher than for pure Al. Type B is more appropriate for sensitive devices.

Uniaxial mechanical cycling was performed to show the difference between the standard Al wire and the Al-clad Cu wire. A several millimeter long piece of wire was fixed in a measuring device and exposed to periodical stress with defined plastic strain. Two criteria for the deformation process have been applied: constant elongation and constant dissipated work. In Figure 2 the elongation is shown on the X-axis, the corresponding dissipated work is the integral of elongation over related stress, shown as the area within the hysteresis curve. One characteristic difference between both materials is the higher stress at the same elongation for the Al-clad Cu wire. The enclosed area is "rotated" in Y-axis direction for the Al/Cu wire. The numbers of mechanical cycles to failure at related strain build the S-N curves shown in Figure 3. The results confirm that Al-clad Cu wire is able to withstand a higher number of mechanical cycles before breaking compared to Al wire.

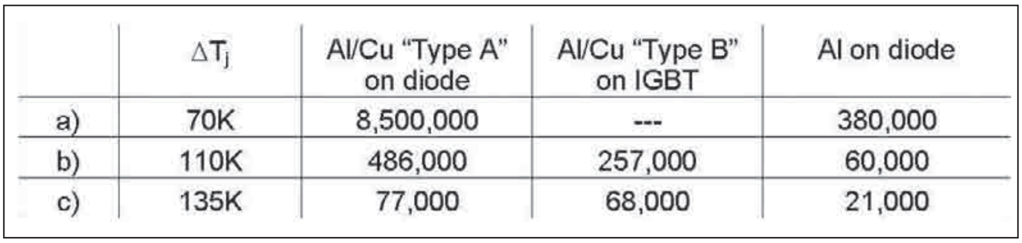
Power cycling results for Al-clad Cu wire bonds

A SKiM63 module was selected as the vehicle for the power cycling test. In a first test series the "type A" Al-clad Cu wire was compared to the standard Al wire. To avoid heel cracking bond loops with comparable aspect ratios of approx. 0.32 were generated for both wire materials. As the "type A" wire was still too hard to be successfully bonded onto sensitive IGBT dies, tests could only be performed on diodes. The power cycling was conducted with three different junction temperature swings and all tests were set with relatively small power-on times (1-2s) to reduce overall test duration.

In a second test series the "type B" Al/Cu wire was investigated. Due to the increased softness of the composite material the bonding process was less critical and also IGBT chips could be successfully bonded. Thus, power cycling tests for the "type B" wire were performed on the IGBT chips. As test duration of the ΔT_j=70K test was expected to be very long, only test conditions ΔT_j=110K and ΔT_j=135K were selected for the characterization of "type B" wire. Table 1 shows the corresponding test results in comparison to the diode results of "type A" Al/Cu wire and the standard pure Al wire.

Although the bonding process is less critical for the softer "type B" version of the Al/Cu wire, its power cycling capability is significantly reduced compared to the original "type A" version. Instead of 77,000 cycles to failure only 68,000 cycles could be achieved with the "type B" wire in the ΔT_j=135K test. The reduction is even more pronounced for the ΔT_j=110K test: The "type B" wire failed after 257,000 cycles. Compared to the "type A" wire test result of 486,000 cycles, this means a reduction of almost 50%. Nevertheless, if compared to the standard Al-wire bonds there is still a

Table 1: **Power cycling test results for "type A", "type B" and pure Al wire bonded**



	ΔT_j	Al/Cu "Type A" on diode	Al/Cu "Type B" on IGBT	Al on diode
a)	70K	8,500,000	---	380,000
b)	110K	486,000	257,000	60,000
c)	135K	77,000	68,000	21,000

huge advantage in load cycling capability (factor >4) which is expected to further increase at smaller temperature swings, which are more relevant for real applications.

It should be emphasized that the presented results were obtained on very first samples of the novel composite material and no detailed bond process optimization was conducted. Further optimization of the wire bond material and the corresponding bonding parameters is expected to allow a better trade-off between the excellent wire bond lifetime and the compatibility to establish a stable wire bond process.

Advantages of Al-clad Cu wire bonds

Pure Cu wire bonds have been proposed as an alternative to pure Al wire bonds for packages of devices with a maximum junction temperature of 200°C. The implementation of pure Cu heavy wire bonds requires the change of chip metallization from Al to Cu, which is associated with severe problems. Cu contacts on silicon devices are subjected to diffusion and corrosion. Diffusion of Cu into the semiconductor device can interfere with the electrical function of the device. Corrosion can also compromise the device functionality if conductive corrosion products interact with the high electrical fields at the passivation edges of high blocking devices. Both problems have to be solved by a suitable design of the contact metallization.

Al-clad Cu wire bonds, however, are compatible with the state-of-the-art aluminum metallization on the top side contact of power devices. They can be applied with minor changes to the bond parameters and do not even require a special bond tool. Therefore, Al-clad Cu wire bonds are well suited to increase the wire bond lifetime without the drawback of a new chip top side metallization.

Al-clad Cu wire bonds versus SKiN-technology

The SKiN technology which replaces the wire bonds by a flexible power layer [4] is a new design approach to address the future needs of power electronics - higher operating temperatures, integration, elimination of thermal grease interface and reliability. The SKiN-technology combines a reduction in thermal resistance and an improved internal parasitic inductance with the enhanced reliability of a wire bond free package technology platform. However in order to exploit the advantages emerging from this new technology, the module outline and system configuration must be adapted to this new packaging platform.

Al-clad Cu wire bonds are suited to replace standard Al heavy wire bond with enhanced Al-clad Cu wires. This replacement does not require additional changes to the module design and can be implemented in any existing module with wire bonded chips. In combination with a replacement of solder die attach by more reliable technologies as Ag diffusion sintering or Transient Liquid Phase Bonding (TLPB), modules with an extended operation temperature range are feasible without impairing the lifetime expectation. Therefore, Al-clad Cu wire bonds allow an evolution of established module designs and thus enable reliability enhancement in existing system designs.

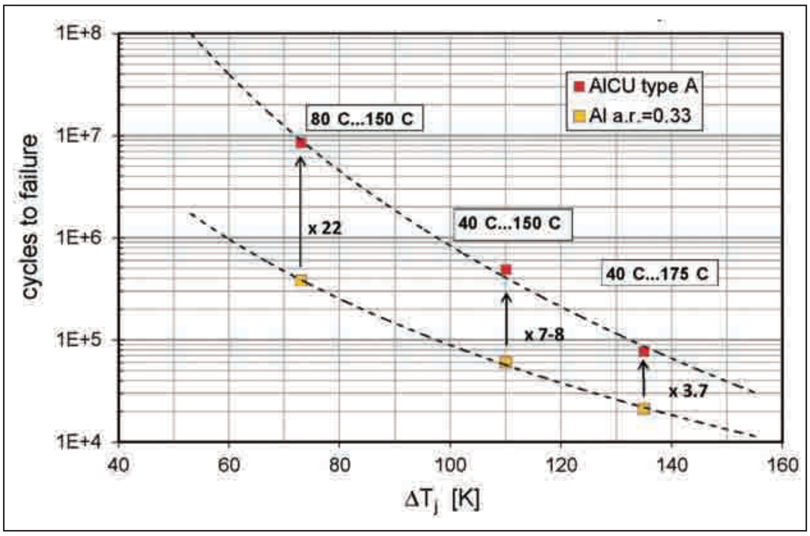


Figure 4: **Power cycling results as a function of ΔT_j: Comparison of 300 µm Al wire bonds with Al-clad Cu-bonds with comparable aspect ratios ("type A", bonded on diodes)**

It should also be noted, that comparison of power cycling lifetime is typically related to a fixed temperature swing. This methodology is acceptable for modules with a comparable thermal resistance. However, when comparing modules with significant differences in thermal resistance (SKiN exhibits a more than 20 % reduced thermal resistance compared to classical module) it must be emphasized, that a higher current density is required for the module with the better thermal resistance to generate the same temperature swing. Based on a constant current density, a module with a higher thermal resistance must feature a much higher lifetime in active power cycling to achieve the same performance.

Conclusion

Both technologies, Al-clad Cu wire bonds and the SKiN technology, are required to meet the challenges of improving the energy generation and distribution and to enhance the efficiency of electrical power consumption.

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CONCEPT
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Taming the Beast

Ultra Low On-Resistance SIC Trench Devices

A new generation of Silicon Carbide (SiC) planar MOSFETs, trench structure Schottky diodes, and trench MOSFETs has been developed. The planar SiC MOSFET technology suppresses the degradation of the parasitic PN junction diodes even if forward current penetrates into the diodes. The trench Schottky diodes exhibit lower forward voltage than conventional SiC diodes while keeping leakage current at an acceptable level. And SiC MOSFETs with a double-trench structure improve reliability of the device while maintaining ultra low on-resistance because the new structure effectively reduce the highest electric field at the bottom of the gate trench, thus preventing gate oxide breakdown. **K. Okumura, N. Hase, K. Ino, T. Nakamura, and M. Tanimura, Rohm, Kyoto, Japan**

Full SiC 1200 V7100 A power module enabling high-frequency operation above 100 kHz

Mass production of SiC planar MOSFETs for the sake of lower switching losses in high voltage applications such as converters and inverters has already started. However, on-resistance increases when current flows into the parasitic body diodes of these MOSFETs. This is because the parasitic PN body diodes, with the base plane dislocation, induce expansion of stacking faults in 4H-SiC epilayers and degrade the on-resistance of both the body diodes and MOSFETs. This is an obstacle for application in circuits which require current penetration from source to drain such as converters and inverters. However, some groups have reported no degradation of PN diodes at the research level.

Our group developed substrate, epitaxy and device fabrication processes to prevent degradation of the body diodes. Figures 1/2 show the MOSFET's on-resistance evaluation and differential on-resistance of the body diodes after continuous current penetration, respectively. We compared two conventional planar 1200 V SiC MOSFETs with 22 newly developed planar MOSFETs. On-resistance is typically 0.09 Ω, die size and active area are 13.2 mm^2 and 10 mm^2, respectively. Applied continuous current from source to drain of the MOSFET is 8 A.

After 24 hours continuous current

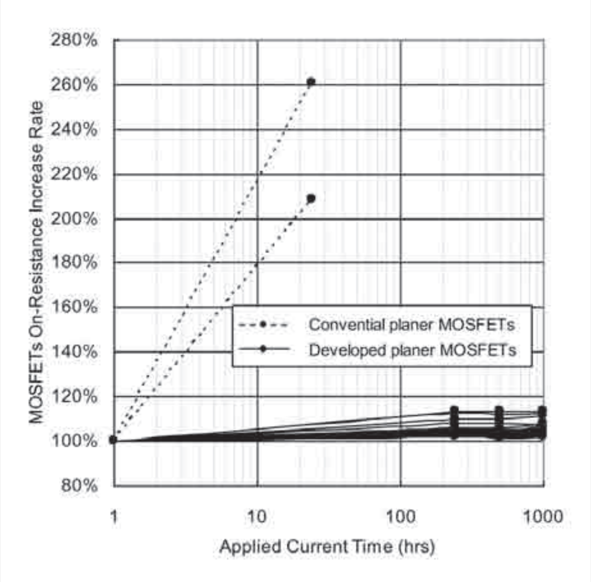

Figure 1: **Comparison of MOSFET's on-resistance increase rate after current application**

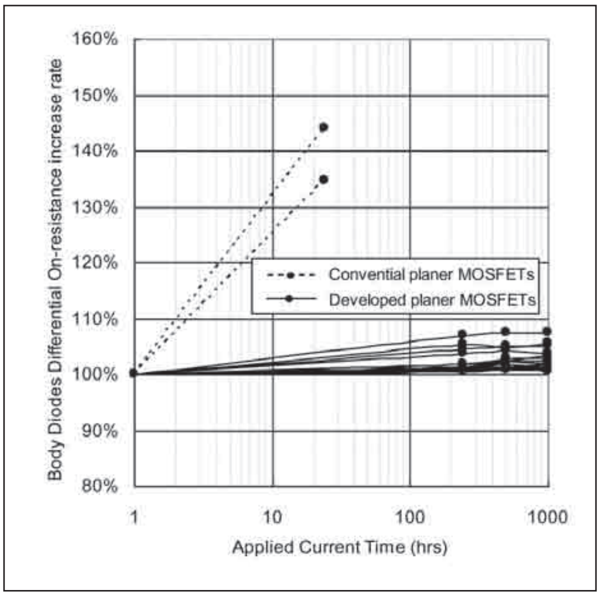

Figure 2: **Comparison of body diodes differential on-resistance increase rate after current application**

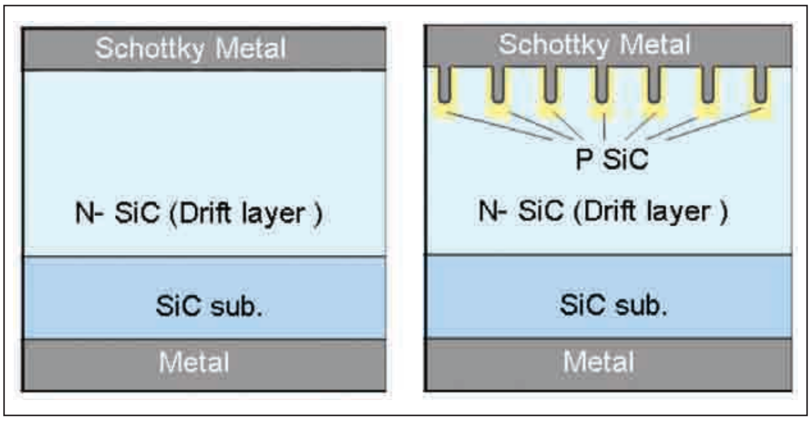

Figure 3: Schematic cross section of the planar (left) and trench Schottky diodes

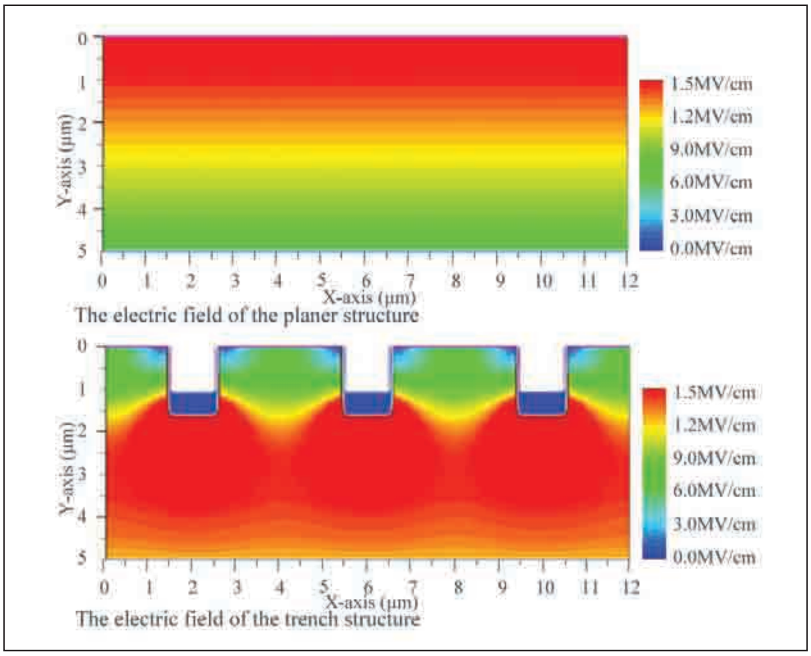

Figure 4: Reverse bias simulation results at 600 V

application, conventional planar MOSFETs show drastically increased on-resistance of MOSFETs and differential on-resistance of body diodes. On the other hand, the planar MOSFETs suppressed degradation of on-resistance even after 1000 hours current application.

SiC trench Schottky diode technology

SiC Schottky diodes are attractive devices to reduce switching losses in high-voltage applications. The reduction of conductive losses is also required to improve efficiency. However, SiC Schottky diodes have higher forward voltage drop when compared to Silicon PN junction diodes. The reason is that SiC Schottky diodes need high barrier heights to block leakage currents because SiC has a breakdown strength 10 times greater than Silicon. The reduction of electric fields at the Schottky interface is crucial for SiC Schottky diodes.

Our group proposes the trench structure Schottky diodes to obtain a lower forward voltage drop while maintaining the same leakage current [1]. Figure 3 shows the schematic cross section of a 4H-SiC planar and trench structure Schottky diode. Trench p region can suppress the concentration of electric field at the Schottky interface.

Figure 4 shows reverse bias simulation results of the electric field distribution. Figure 5 indicated the highest electric field at the Schottky interface of the planar structure and the trench structure is 1.65 MV/cm and 0.68 MV/cm, respectively. The simulation shows a lower barrier height can be obtained by using a trench structure.

The barrier heights of the fabricated TO-220 planar and trench diodes are different at 1.31 eV and 0.85 eV, respectively. Trenches are 1.05 µm deep. The diode die size is 3.06 mm^2.

The threshold voltage of the trench structure is 0.48 V smaller than that of the planar device. The smaller threshold voltage can reduce the conductive losses during forward operation. The leakage current at 600 V is comparable.

SIC double-trench technology for MOSFETs

Compared with planar MOSFETs SiC trench MOSFETs can have lower conductive losses because the planar technology feature JFET regions which increase the on-resistance [2, 3]. Our group previously reported 790 V SiC trench MOSFETs with the lowest Ron at room temperature. However, the trench MOSFETs had issues regarding oxide breakdown at the trench bottom during high drain-source voltage application. To resolve the issue of gate oxide breakdown, a double-trench structure with both source and gate trenches was developed [4, 5].

The structures for the single and double-trench structures are shown in Figure 5. To suppress the electric field at the gate oxide bottom, the source trench is fabricated deeper than the gate trench. Figures 6/7 show drain-source bias simulation results of the electric field distribution at 600 V with a gate-source voltage of 0 V. In the single-trench structure the highest electric field at the bottom of the gate trench was 2.66 MV/cm. On the other hand, that

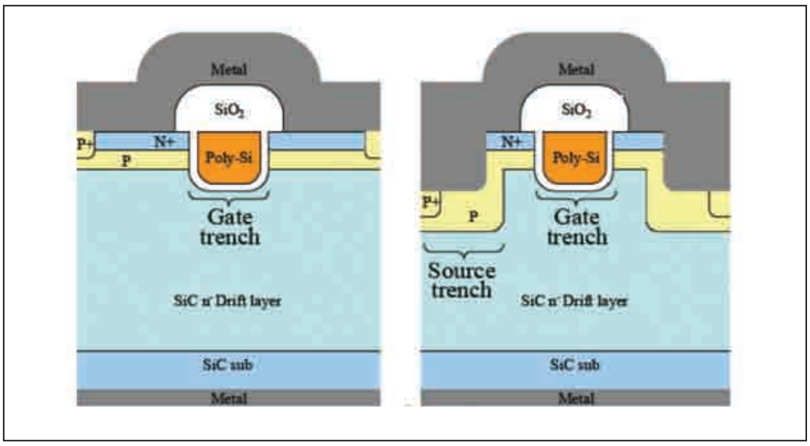

Figure 5: Cross section of 4H-SiC trench MOSFET with single-trench (left) and source/gate trench

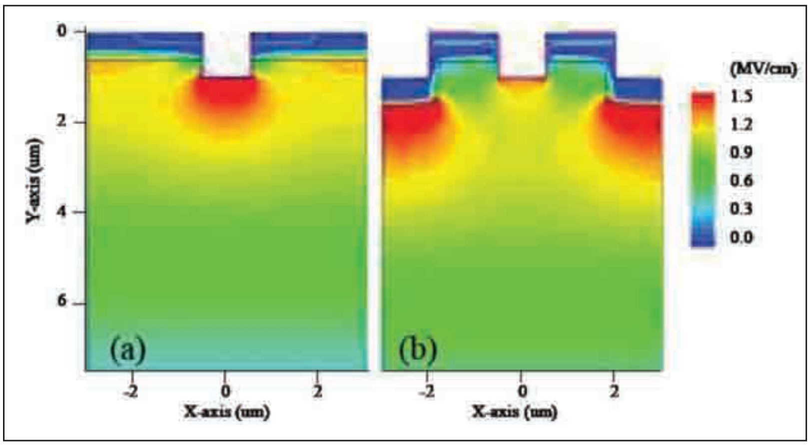

Figure 6: Drain-source bias simulation results at 600 V with 0V gate-source voltage

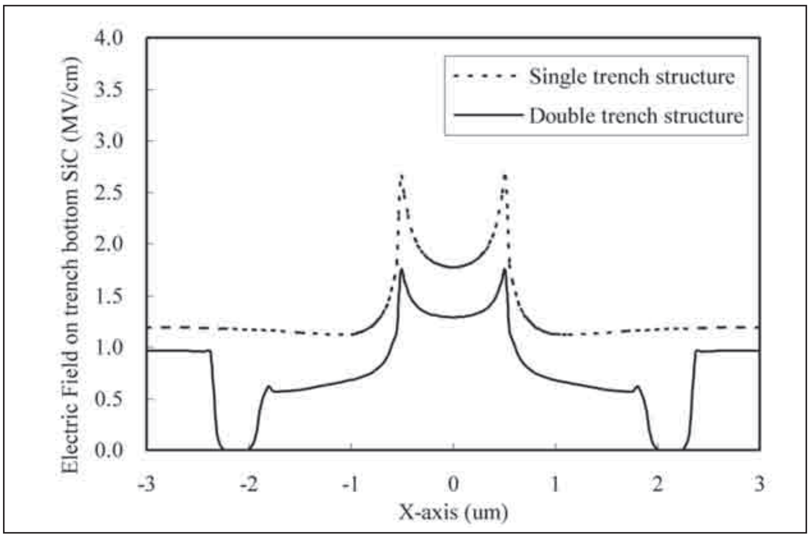

Figure 7: Electric field for the single and the double-trench structure

figure was effectively reduced to 1.66 MV/cm in the double-trench structure. Deeper source trenches prevent the concentration of electric fields at the bottom of the gate trench.

Double-trench MOSFETs are fabricated using two different epitaxial layers. The trench depth is typically 1.0 µm, the thickness of gate oxide about 50 nm.

The measured channel mobility on the trench sidewalls of the double-trench MOSFET is about 11 cm²/Vs. The charge to oxide breakdown estimated by CCS-TDDB (constant current stress time dependence dielectric breakdown) test of the gate oxide was typically 15 C/cm² equivalent to that of a Silicon device. The negative gate bias of the commercial SiC MOSFETs is limited to -6 V. This is because continuous negative gate bias causes a negative shift in threshold voltage, possibly due to hole traps in the gate oxide or MOS interface. However, the rate of change in threshold voltage of the SiC trench MOSFETs under negative gate bias testing at V_{gs}=-18 V after 3000 hours covered a range of only 5 %.

Figure 8 shows two kinds of I_d/V_{ds} characteristics of the trench MOSFETs using different epi-layers: 1.8 $e^{16}cm^{-3}$/ 5 µm and 7.5 $e^{15}cm^{-3}$/7 µm. The die sizes are the same, 2.56 mm² and the active areas are 1.422 mm². The $R_{on,sp}$ was estimated at 0.79 mΩcm² and 1.41 mΩcm² at I_d=1 A, respectively. The blocking voltage was 690 V and 1200 V at I_d=100 µA, respectively. Figure 9 shows the performance comparison of 4H-SiC switching devices. Low on-resistance while maintaining the high reliability of the gate oxide has been achieved.

Conclusions

Our newly developed SiC planar MOSFETs suppress the degradation of the parasitic PN junction diodes when forward current penetrates. SiC Schottky diodes with trench structure successfully showed ultra low forward voltage drop while maintaining low leakage current. SiC MOSFETs with a double-trench structure have obtained ultra low on-resistance with improved reliability of the gate oxide. This article has been derived from a paper entitled ‘Ultra Low Ron SIC Trench Devices’ presented at PCIM 2012. It has been awarded as the best paper [6].

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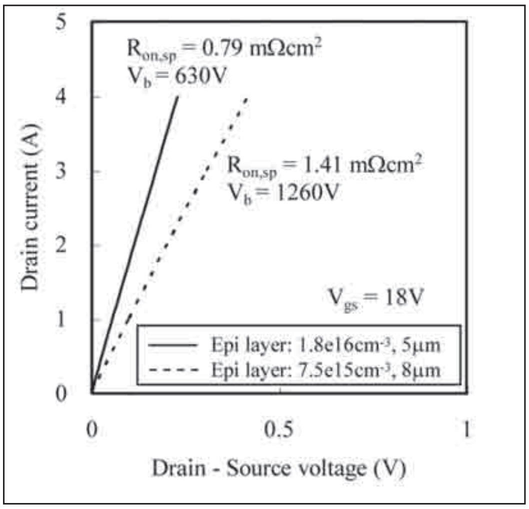

Figure 8: I_d/V_{ds} characteristics of double-trench MOSFETs at V_{gs}=18 V

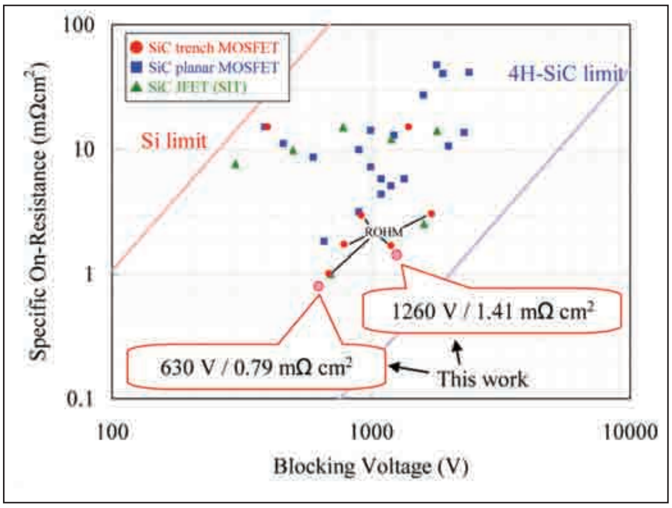

Figure 9: Performance comparison of 4H-SiC switching devices

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Full SiC Power Modules

ROHM announced at PCIM mass production of full SiC power modules (1200V/100A) as custom design comprised entirely of SiC power elements.

The new modules integrate a state-of-the-art dual-element SiC SBD/MOSFET pair that reduces loss during power conversion by 85 % compared with conventional Si IGBT modules. In addition, high-frequency operation of at least 100 kHz is possible. Although the modules are rated at 100 A, their high-speed switching capability, reduced loss, and heat dissipation characteristics make them replacements for 200-400 A Si IGBT modules. Replacing a conventional 400 A-class IGBT with this compact, low-profile package can cut volume by 50 %, and the lower heat generated requires less cooling countermeasures, contributing significantly to end-product miniaturization.

Due to the expertise of Erlangen-based wafer supplier SiCrystal AG, which is part of the corporate group, ROHM possesses total manufacturing capability for SiC semiconductors from ingot formation to power device fabrication. This allows the rapid development of products and complete control of raw materials.

Silicon Carbide BJT's in Boost Applications

Efficiency is becoming more and more important as well as size and cost. In boost DC/DC converters, typically used in PV inverters and PFC circuits, increased switching frequency makes a big impact on both size and cost. Silicon Carbide (SiC) bipolar junction transistors (BJT's) offer low-loss high speed switching combined with low conduction losses enabling higher switching frequency and maintaining high efficiency. SiC BJT's combine the best properties from Silicon unipolar and Bipolar technologies in a normally-off device. The design and performance of a 1kW boost circuit based on the SiC BJT is presented in this article.

Peter Haaf and Martin Domeij, Fairchild Semiconductor Germany and Sweden

SiC BJTs using a vertical NPN structure were fabricated and assembled in an industrial standard TO-247 package. This type of transistor combines very low conduction losses with fast and low loss switching behavior [1]. The high critical field strength of SiC gives the possibility to have low saturation voltages without driving the transistor into hard saturation. Since there is no channel region in a BJT the $V_{CE(SAT)}$ is determined mainly by the collector series resistance.

It is not necessary to drive the SiC BJT into hard saturation which gives them excellent switching properties. There is no current tailing and a minimal storage delay (5 ns) at turn-off. The SiC BJT is also a very robust device with a wide RBSOA, good short circuit capability [2] and can operate at high temperatures [3]. SiC BJT's have suffered from bipolar degradation, making the gain decrease significantly over time [4]. The BJT's discussed do not have this problem (Figure 1).

Base drive circuit and the challenges

A SiC bipolar transistor is a current driven device. The driver must deliver enough current to turn the device on and off, plus load and unload the Miller charges quickly enough. Nevertheless the losses in the drive circuit should be limited. One target for this development was to decrease the driver losses as much as possible, without impacting the switching speed.

To have enough safety margin the base current should be oversized by a factor of 1.5 compared with the calculated base current (I_b = beta • I_c). To simplify the base drive circuit using a constant base current is recommended.

We developed a driver board with an adjustable dual supply, V_{cc} and V_{ee}, a high speed opto-isolator and an additional capacitor C10 in parallel to the base resistor R2 to boost the base current for a short moment, just during turn-on and turn-off of the BJT.

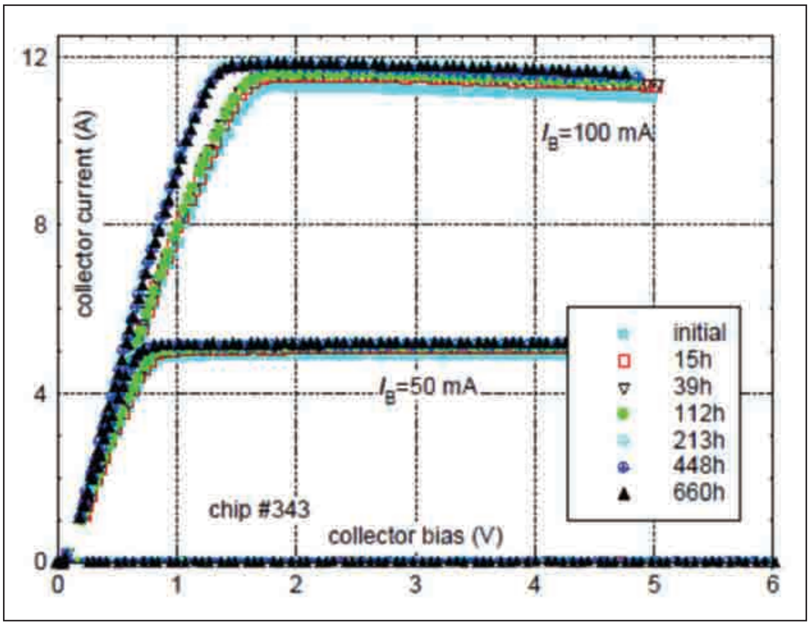


Figure 1: **Gain (hFE) and $V_{CE(SAT)}$ before and after 660 hour DC stress test (open collector, I_{BE}=0.25 A)**

When the BJT is turned on, V_{be} is equal to 2.9 V with a slightly negative temperature coefficient. The positive supply voltage of the driver is divided into a small voltage drop in the driver, the V_{be} and the voltage drop across the base resistance R2. The capacitor C10 in parallel to R2 will be charged in this moment to the voltage across R2. When the device is turned off, this capacitance provides a short increase in the drive current to increase the switching speed of the BJT.

Two big obstacles for fast switching are the parasitic inductances of the package and the PCB. To reduce the influence of these parasitics the supply voltage for the driver could be increased, but this would lead to significant higher drive losses during turn-on. The alternative would be two separate drivers, one for fast switching, the other for supplying the base current. As this would make the circuit expensive and complicated, we decided to use the additional boost capacitor C10 in parallel to the base resistance R2. In any case, the negative supply for the driver cannot be avoided for fast switching.

Double pulse test setup

The base drive circuit has been optimized with the double pulse test setup. Turn-on and turn-off waveforms can be analyzed separately without the need for a full thermal design.

The test set up is optimized, the inductor is a 1 mH coreless choke and the capacitors have been placed in shortest

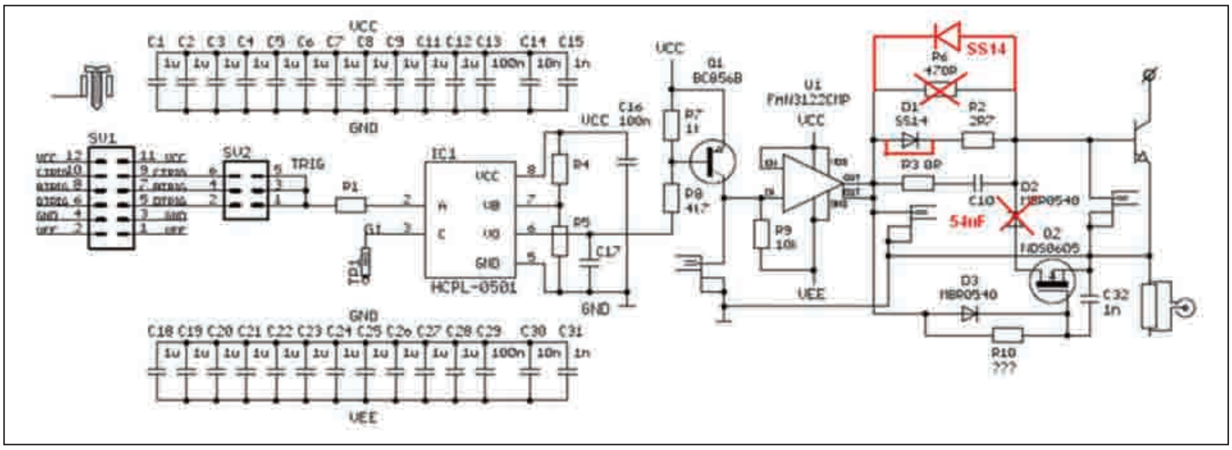


Figure 2: **Base drive circuit for SiC BJT**

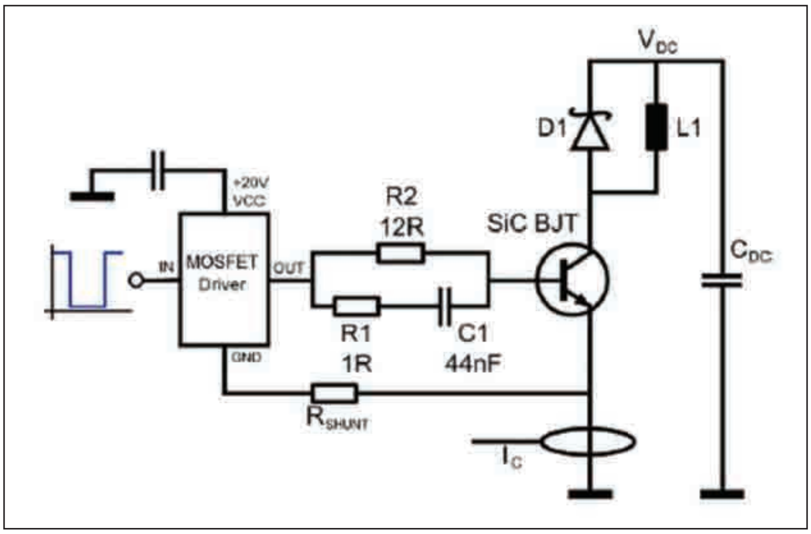


Figure 3: **Double pulse test setup**

distance to the semiconductors in order to reduce the current loop inductance.

By changing the position of the diode, the same test setup can be used for the boost function. In this case the diode will charge an additional bank of capacitors connected to the load. That means that at least the primary side circuit and the drive circuit are identical and the test results can be compared easily.

Some differences from SiC BJTs to conventional switches are characterized by the turn-on and turn-off waveforms shown in Figure 4 and 5. The drive circuit is supplied by V_{cc} = 7V and V_{ee} = -3V. The red curve M1 shows V_{be}, which is measured by the differential signal between base and emitter lead. When turning the BJT on, the signal starts to rise from -3V to +3V by charging C_{be}. At the threshold of 3 V the current starts to commutate from the diode to the BJT at a di/dt of around 1000 A/µs.

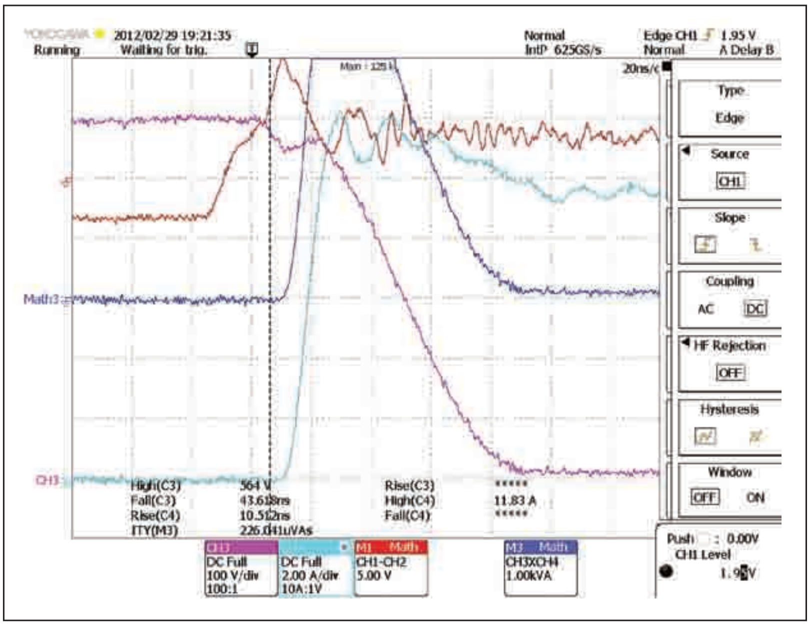
The relatively big C_{be} capacitance gives the BJT stability, as well at slightly noisy gate signal. The first drop of V_{ce} is caused by the induced voltage across the loop inductor (V_{ind} = -L_{loop} • di/dt).

As soon as the diode current drops to zero, the V_{ce} of the BJT starts to drop. A strong base driver is now needed to discharge the Miller capacitance of the BJT.

During turn-off, both the current and voltage waveform start to change at the same time. In the first nanoseconds the base current must charge the Miller capacitance. As soon as V_{ce} reaches the bus voltage, the change in the di/dt of the current drop is visible. Due to the ideal features of the SiC material the influence of the removal of the stored carrier charge is negligible, this causes just a delay of about 5 ns in the begin of the turn-off procedure.

It is often said that TO247 packages cannot handle the high switching speeds of the SiC devices. In order to double check we performed some tests. As the driver board is opto-isolated, the connection to the BJT is rather flexible. The GND-trace of the driver is connected to two different points of the emitter lead of the BJT.

The most significant difference is visible at highest currents and at maximum di/dt. During turn-on at a di/dt of 1000 A/µs,

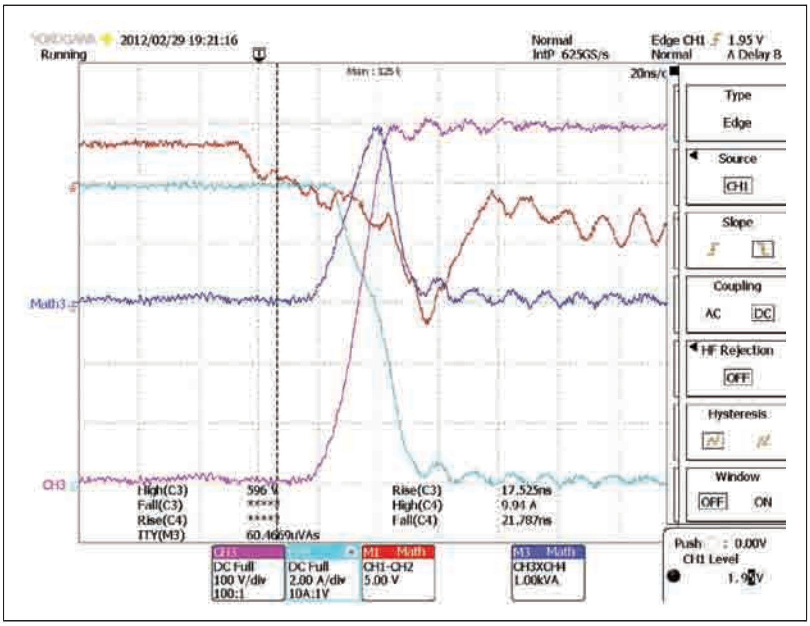

YOKOGAWA 2012/02/29 19:21:35
Running Waiting for trig.
Normal IntP 625GS/s
Edge CH1 1.95 V Normal A Delay B
20ns/div

High(C3) 564 V
Fall(C3) 43.618ns
Rise(C4) 10.512ns
ITY(M3) 226.041uVAs
Rise(C3) *****
High(C4) 11.83 A
Fall(C4) *****

CH3 DC Full 100 V/div 100:1
CH4 DC Full 2.00 A/div 10A:1V
M1 Math CH1-CH2 5.00 V
M3 Math CH3XCH4 1.00kVA

Type Edge
Source CH1
Slope
Coupling AC DC
HF Rejection OFF
Hysteresis
Window OFF ON
Push : 0.00V CH1 Level 1.95V

Figure 4: **Turn-on of the SiC BJT (E_{on} = 226 µJ, Ch3 magenta...V_{ce} = 600V, Ch4, blue...I_c = 10 A)**



LEFT Figure 5: **Turn-off of the SiC BJT (E_{off} = 60 µJ, M1, red...V_{be} = V_b - V_e, M3, dark blue...E_{on}, E_{off})**

we measured an increase of E_{on} losses from 117 µJ to 172 µJ and the peak voltage drop across this lead has been measured at 7 V. A similar effect can presumably be seen when considering the voltage drop across the emitter bond wire under the similar conditions. The good thing is the relatively large base-emitter capacitance which prevents the device from a parasitic turn-off. The usage of packages with separated power-emitter pins and drive-emitter pin will solve this problem and will make the device easier to control.

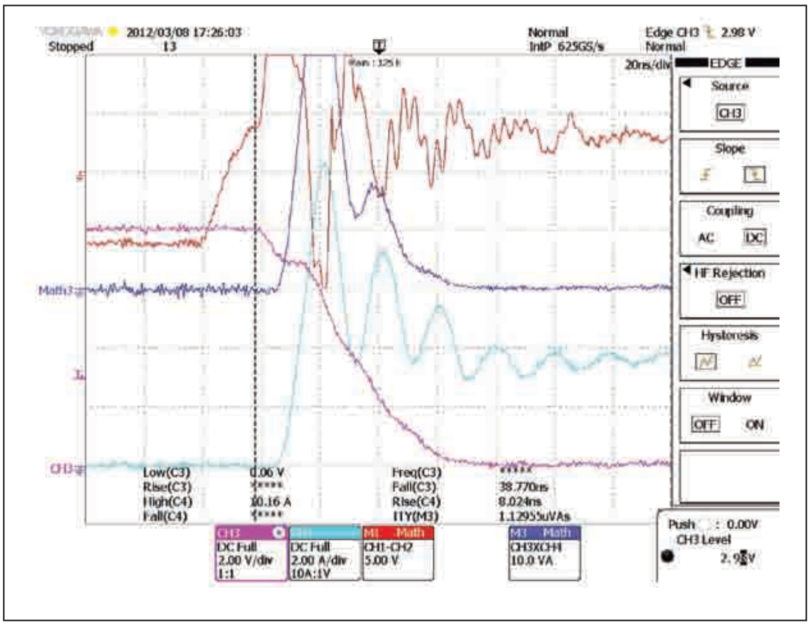
The boost converter

Three different boost configurations were reviewed. The first circuit was a continuous conduction mode (CCM) boost circuit using the 12 A/1200 V SiC BJT and 20 A/1200 V SiC diode. This was tested at the two switching frequencies 20 kHz and 40 kHz. The second circuit was a boundary conduction mode (BCM) boost circuit using the same devices. The ZVS approach of the BCM boost looks very promising in comparison to the hard switched CCM mode. Finally we operated our high speed IGBT FGL40N120AND in combination with the SiC diode at 20 kHz in CCM mode as a reference.

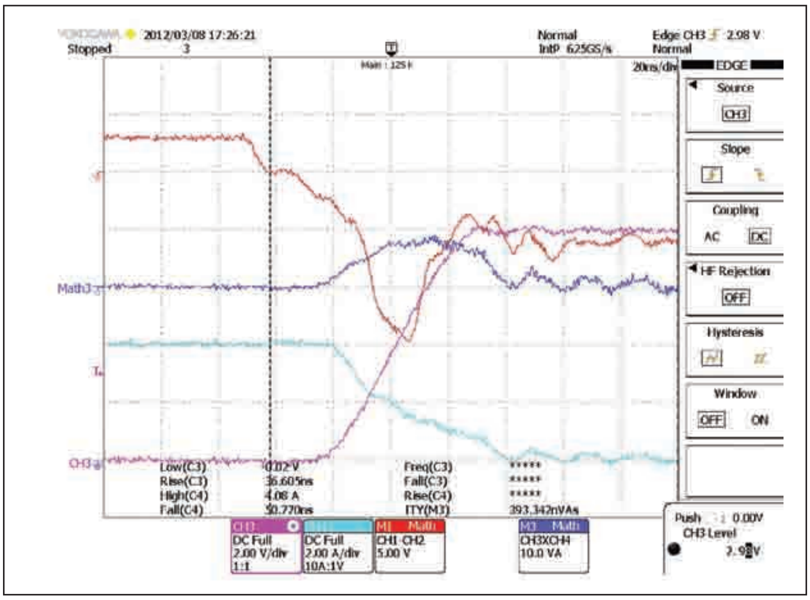
For the CCM operation we used a 10 mH coreless inductor. In order to reduce the drive losses the positive operation voltage the driver V_{cc} was reduced to 6 V. The negative driver supply V_{ee} has been increased to -6V without any impact on the drive losses. The waveforms at max power at V_{out} = 812 V are shown in Figures 6 and 7.

The big obstacle for BCM operation is high ripple currents and varying frequencies. A typical power range of a practical 2-phase interleaved PFC application is about 1 kW down to 90 VAC input voltage. Increasing the input voltage to 400 VAC, it is easily possible to increase the power range to 4 kW without changing the current level. By going from PFC to boost or from 2-phase to 4-phase interleaved operation a power level of 8 kW with this topology will be no problem. Figures 8 and 9 show the test results.

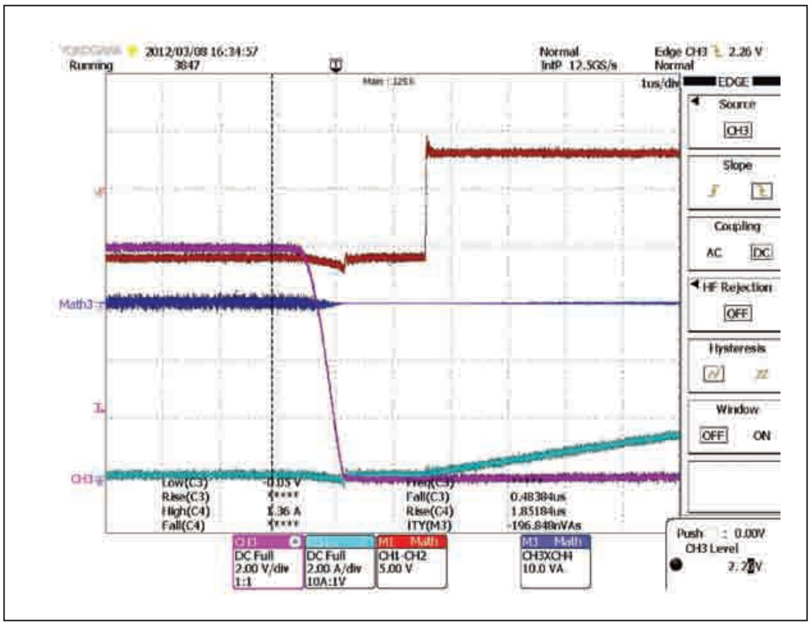
The very smooth decrease of the V_{ce} and the turn-on without any losses is clearly visible. The parasitic capacitance of the inductor and the junction capacitance of the SiC diode limit the dV/dt in Figure 9



ABOVE Figure 6: **E_{on} measurement in CCM (E_{on} = 113 µJ, Ch3 magenta...V_{ce}, Ch4 blue...I_c)**



LEFT Figure 7: **E_{off} measurement in CCM (E_{off} = 51 µJ, M1 red...V_{be}, M3 dark blue...E_{on}/E_{off})**



LEFT **Figure 8: Smooth turn-on of the SiC BJT in ZVS (E_{on} = 0 μJ, V_{out} = 800 V, Ch3 magenta...V_{ce}, Ch4 blue...I_c)**

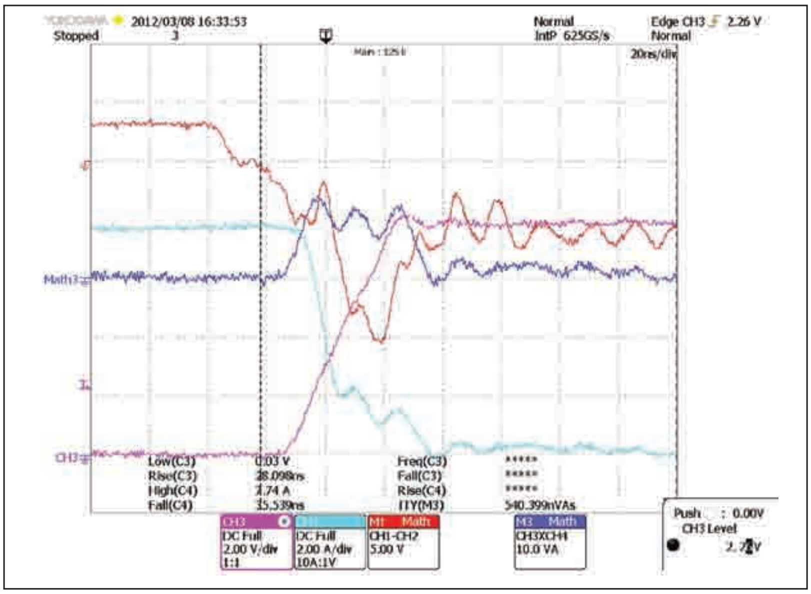


Figure 9: **Turn-off waveform in BCM at V_{out} = 800 V (E_{off} = 54 μJ, M1 red...V_{be}, M3 dark blue...E_{on}/E_{off})**

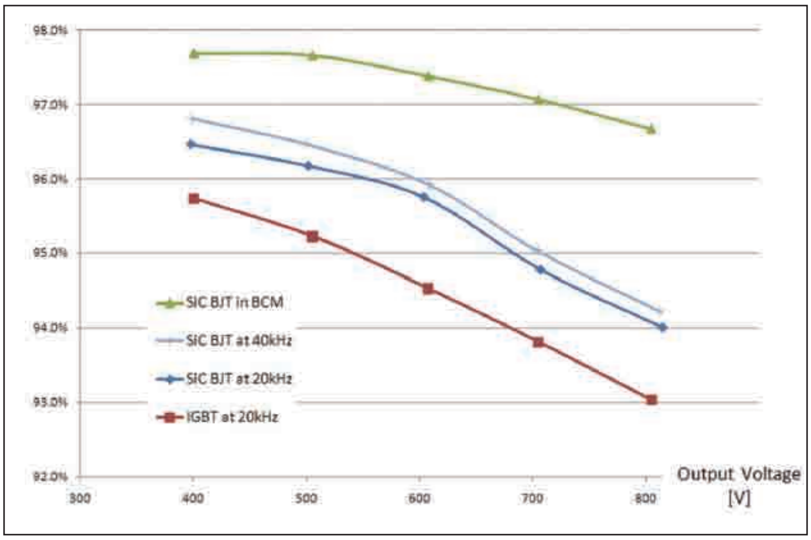


Figure 10: **Measured efficiency of the variations of the boost converters**

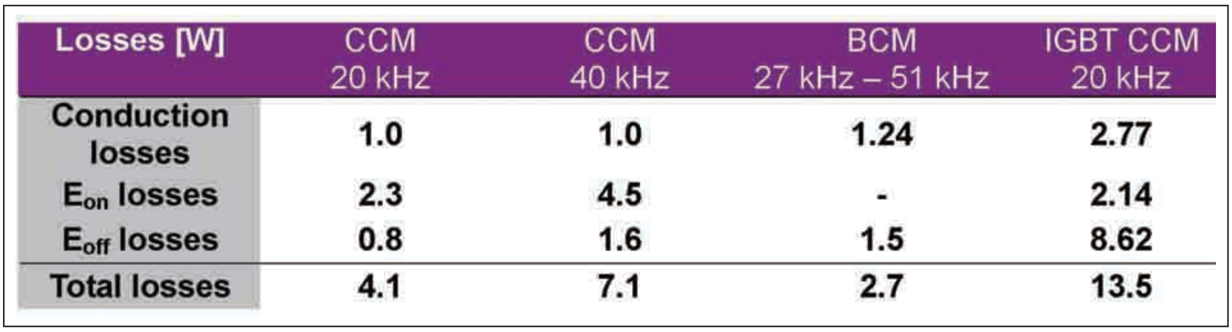
to 5 kV/μs. All transitions look very smooth and promising, especially regarding EMI performance. For the inductor we chose a Kaschke E-core with L= 0.68 μH and multistrand wire, which is optimized for high di/dt.

Finally we compared the very well known behavior of a fast switching 1200V IGBT to the SiC BJT in CCM mode. The identical power circuit operates at 20 kHz, the driver is as well the FAN3122, but for IGBTs it operates between V_{cc} = 15V and GND. The gate resistor is equal to 4.7 Ω. The IGBT at a T_B=100ns shows about 10x higher E_{off} losses. The E_{on} losses of the SiC BJT and IGBT are in the same range.

The boost measurements have been performed with a constant V_{in} = 210 VDC. The output voltage was adjusted by changing the duty cycle or/and the frequency in 100 V steps from V_{out} = 400 V to 800 V. The load is a parallel and series operation of incandescent bulbs of 880 W in total.

The BCM boost shows best results, the CCM boost at 20 kHz and 40 kHz medium and the Si IGBT comes third in this competition. The higher efficiency for the 40 kHz CCM circuit versus the 20 kHz CCM is attributed to the lower ripple current seen in the inductor and capacitor at 40 kHz compared with the 20 kHz solution. Figure 10 shows the measured efficiency of the variations of the boost converters.

Actually we would have expected in general a better total efficiency for all measurements. Similar to tests seen on very low $R_{DS(ON)}$ MOSFETs in DC/DC applications, the package and layout effects start to dominate as the losses of the semiconductors become less significant. Based on the accompanying



Losses [W]	CCM 20 kHz	CCM 40 kHz	BCM 27 kHz – 51 kHz	IGBT CCM 20 kHz
Conduction losses	1.0	1.0	1.24	2.77
E_{on} losses	2.3	4.5	-	2.14
E_{off} losses	0.8	1.6	1.5	8.62
Total losses	4.1	7.1	2.7	13.5

Table 1: **Loss calculation of the switches in the application at V_{in}=210 V, V_{out}=800 V, P_{out}=735 W (assumption for conduction losses: SIC BJT R_{on}=100 mΩ; IGBT $V_{CE(SAT)}$=1 V)**

scope measurements for E_{on} and E_{off}, a loss calculation for the switches has been performed (see table 1). The weak point of the test setup is a symmetric EMI filter, which should prevent noise getting in the power analyser. A big portion of the total losses are dissipated in this device. More than 80 % of the losses are dissipated in the passive components.

Conclusion

The SiC BJT offers significant efficiency advantages in boost applications compared with silicon IGBT technology. Similar to when using other high performance technologies, the passive and layout parasitic elements start to dominate the losses. This article is derived from a paper given at PEE's Special PCIM 2012 Session [5].

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SiC MOSFETs under High-Frequency Hard Switched Conditions

Silicon carbide (SiC) MOSFETs enable lower system costs by providing the ability to increase power density and frequency of operation, thereby reducing the size, weight and complexity of the system. The first commercial SiC MOSFET was released by Cree in early 2011 and initial demonstrations of its high frequency capability were presented at PCIM 2011. In this article results that make direct comparisons of the SiC MOSFET to Silicon (Si) MOSFETs and IGBTs are presented which show the large reduction in switching losses in the SiC MOSFETs. **Bob Callanan and Julius Rice, Cree Inc., USA**

In order to make this comparison meaningful in the context of real applications, the measurements need to go beyond the usual set of curve tracer data and double-pulse switching loss measurements. Applications where SiC MOSFETs are getting design wins include grid connected solar inverters, power factor correction (PFC) circuits, motor drives, or uninterruptable power systems (Figure 1). All of these candidate applications operate their switches at a specified voltage, current, switching frequency and case temperature.

A generic demonstrator operating the switch under the same specified conditions as these applications will robustly illustrate the relative advantages between technologies.

The original 10 kW demonstrator [1] was a half-bridge buck-derived DC/DC converter with the output current being recirculated to the input voltage link thus avoiding the need for a high power load and providing a capability to directly measure overall system loss. Operation at higher frequencies was not practical due to the limitations of the transformer windings. Furthermore, observation of the MOSFET voltage and current was difficult because neither of the MOSFETs were referenced to ground.

A new demonstrator was designed to overcome this limitation. The concept was to select a transformer-less DC/DC converter platform with a single ground-referenced switch that would afford the capability of recirculating the load current back to the input link. The decided

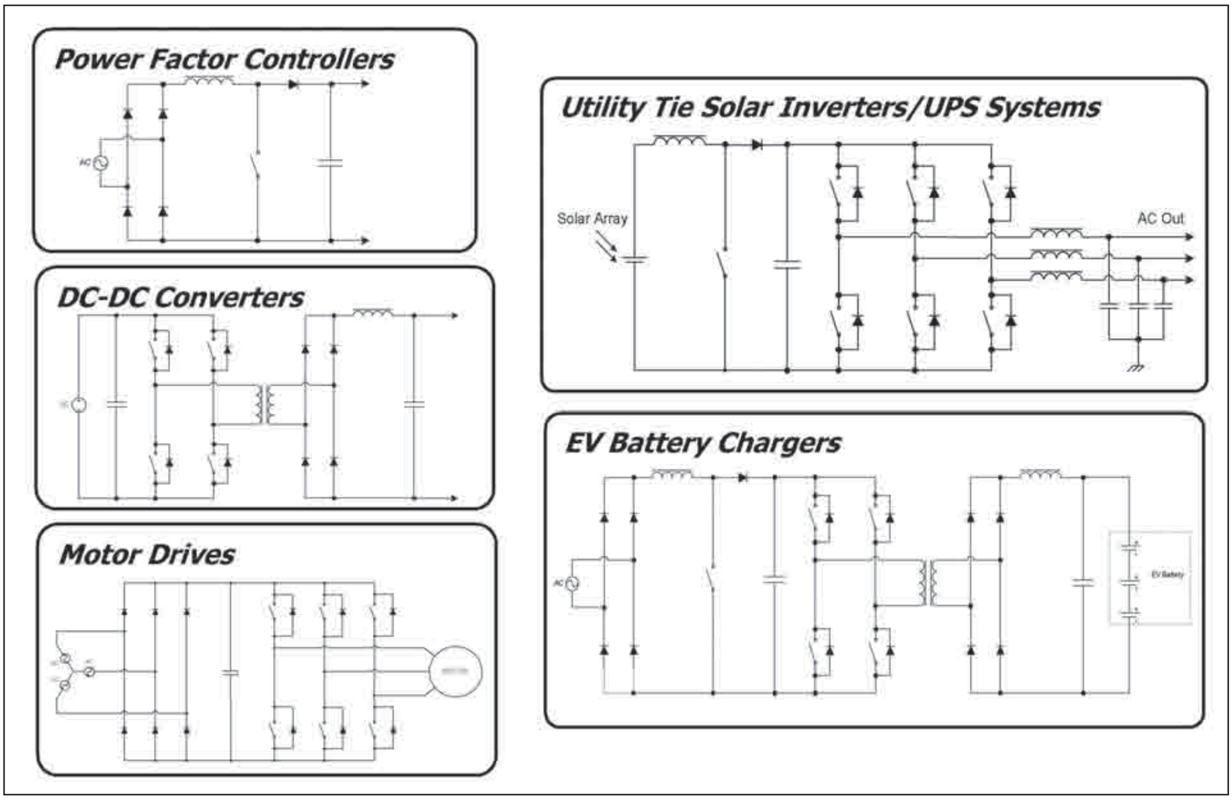

Figure 1: **Diversity of SiC MOSFET applications**

solution was a single ended primary inductor (SEPIC) converter to illustrate the relative performance of the Cree CMF20120D 1.2 kV 80 mΩ SiC MOSFET with state of the art 1.2 kV Si MOSFETs and IGBTs. This converter provides the ability to buck and boost without inverting the output voltage thus making it a natural candidate for this application.

Comparison devices

The basis for the comparison was to select the best available examples of a 1.2kV Si MOSFET and 1.2kV Si IGBT in a TO-247 package and compare them with the Cree CMF20120D 1.2kV SiC MOSFET.

A Si IGBT and a Si MOSFET were selected for this study. A representative 1.2 kV 40 A trench and field-stop Si IGBT [2] was chosen because its forward voltage at 20 A is very similar to that of the CMF20120D. The chosen MOSFET [3] is one of the best 1.2 kV Si MOSFETs in a TO-247 package currently on the market. Furthermore, the maximum current rating at 100°C is similar to that of the CMF20120D. It is also worth noting that the CMF20120D has the lowest gate charge and energy even though the gate voltage is 20 V.

SEPIC demonstrator design

The SEPIC topology has been chosen for the demonstration vehicle because it is simple and has a buck/boost characteristic. This allows the output current of the converter to be recirculated back to the input with the switch operating at a duty cycle slightly greater than 50 %. Under normal circumstances, the SEPIC converter is not widely used for high power operation chiefly because of high switch stress. In this converter, the voltage across the switch is twice the input voltage and the current through the switch is twice the output current. This is ideal for the purposes of demonstration because the input DC supply has to provide only half the desired switch voltage. Furthermore, the switch is referenced to ground so precise voltage and current measurements are simplified.

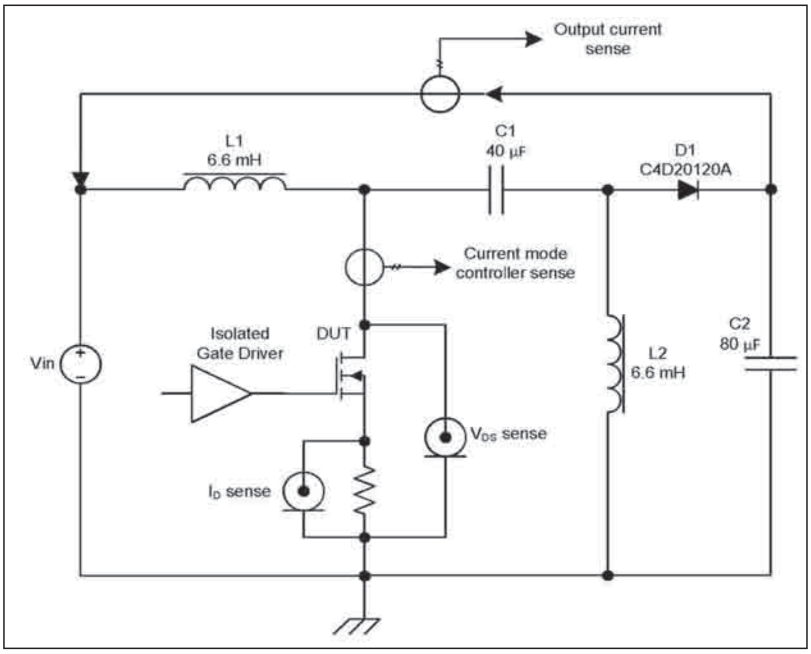

Figure 2: SEPIC converter schematic

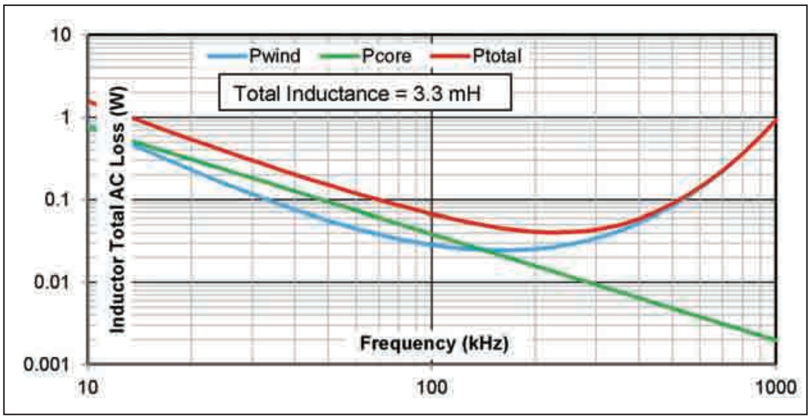

Figure 3: Inductor AC loss vs. frequency

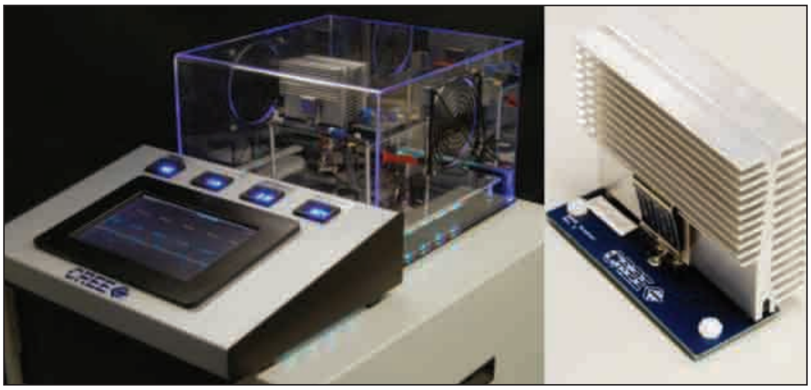

Figure 4: SEPIC demo box and daughter card

A simplified schematic of the SEPIC demonstrator is shown in Figure 2. The demonstrator is a standard SEPIC converter consisting of a switch (DUT), diode (D1), blocking capacitor (C1), output capacitor (C2) and two inductors (L1 and L2). The output current of the converter is fed back to the input source (V_{in}) as shown by the arrows. The controls consist of a simple peak current mode controller being fed from a current transformer to sample the drain of the DUT. The current mode controller's input comes from an error amplifier used to regulate the output current. The output (recirculated) current is sensed by a Hall-effect sensor. Diagnostics for the DUT include a high frequency current viewing resistor to observe the DUT current and a Kelvin connected voltage probe to view the DUT voltage. The gate driver is isolated to prevent a ground loop being formed around the current viewing resistor.

The inductors are designed for minimum AC loss with no regard to physical size to allow the inductor loss to be insensitive to higher frequencies. Therefore, the inductor loss is dominated

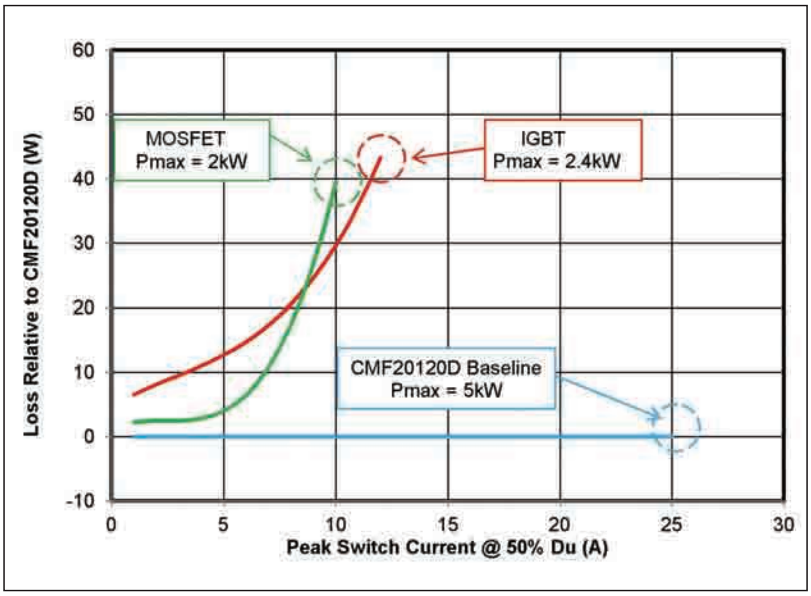

Figure 5: **Relative switch loss comparison at 30 kHz ($V_{DS}/V_{CE} = 800$ V)**

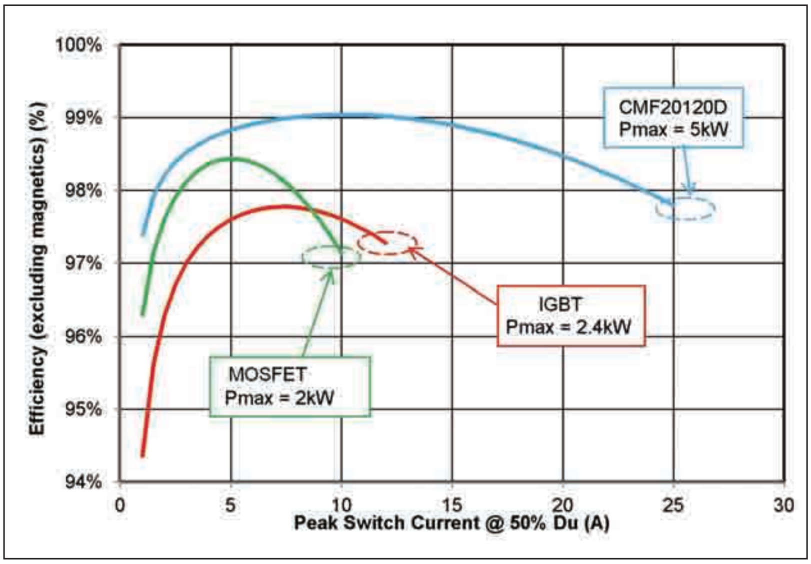

Figure 6: **Efficiency (excluding magnetics loss) at 30 kHz ($V_{DS}/V_{CE} = 800$ V)**

by the DC winding resistance. This greatly simplifies inductor loss calculations. The inductors in the SEPIC converter consist of individual 3.3mH units wound on a Ferroxcube U-U93 3C90 ferrite core. The windings consisted of 540 x AWG40 type 2 Litz wire. Three sets of air gaps were used to minimize fringing effect. The measured AC loss versus frequency of the 3.3 mH inductor is shown in Figure 3. As shown, the total AC losses (core + AC winding resistance) are less than 300 mW from 30 kHz to 300 kHz.

The actual hardware in Figure 4 consists of a lower rack assembly which houses the high voltage and logic power supplies along with the SEPIC inductors. The remainder of the SEPIC converter and control board are located above the rack assembly in a box. A monitor panel is located in front and contains meters to display the input voltage, total system loss, delivered current and delivered power meter. A VGA monitor is also included to display the DUT voltage and current waveforms.

The SEPIC is constructed to facilitate ease of changing switching devices. This is accomplished by mounting the DUT on a separate daughter board with heat sink that attaches to the main power board through a connector.

Comparison at 30 kHz

The first and easiest comparison that can be made with the SEPIC demonstrator is simply plotting the input power versus switch current for each switch. The switches are tested under identical conditions with identical components. Therefore difference in input power between different switches is a direct measurement in differences in switch loss. To simplify the comparison, the input power versus peak switch current for the SiC MOSFET was used as a baseline. This data was subtracted from the input power versus peak switch current data of the other devices. The result shows the increased switch loss of one switch type versus another. A plot of input power (system) loss relative to the SIC MOSFET versus peak switch current is presented in Figure 5. The input voltage to the SEPIC demonstrator was 400 V which resulted in the switch voltage of 800 V. The test was terminated when the thermal design limits were exceeded.

The results show that the SiC MOSFET achieves the highest switch current 25 A and delivered power is 5 kW. The IGBT reaches a maximum switch current of 12 A which equates to 2.4 kW of delivered power. The higher switching loss is the limiting factor. The Si MOSFET reaches a maximum switch current of 10 A equating to 2 kW. In this case, the higher conduction loss limits its efficiency and maximum current.

It is also useful to show the results of this test as a measure of efficiency instead of relative power loss. The switches under evaluation have fairly low losses and the inductors have a significant amount (albeit very predictable) of I^2R loss. This makes it somewhat difficult to see the differences in performance between switches in a straight efficiency plot using the input and output power. This problem can be mitigated by subtracting out the inductor loss from the total system loss. A plot of this efficiency versus peak switch current is shown in Figure 6. The efficiency plot shows that the SiC MOSFET is the highest efficiency switch and can deliver 5 kW in the demo. Second in delivered power is the IGBT delivering 2.4 kW. However, the efficiency is about 1.2 % lower than the SiC MOSFET. Lastly, the Si MOSFET delivers the least amount of power at 2 kW. However, the peak efficiency observed is only about 0.25% lower than the SiC MOSFET. Unfortunately, due to high conduction losses, the efficiency drops rapidly as current is increased.

Comparison at 100 kHz

The tests at 100 kHz compared only the SiC MOSFET and the Si MOSFET. The switching losses of the IGBT were so high that operation under hard switched conditions at 100 kHz was impractical.

A plot of input power (system) loss relative to the SIC MOSFET versus peak switch current is presented in Figure 7.

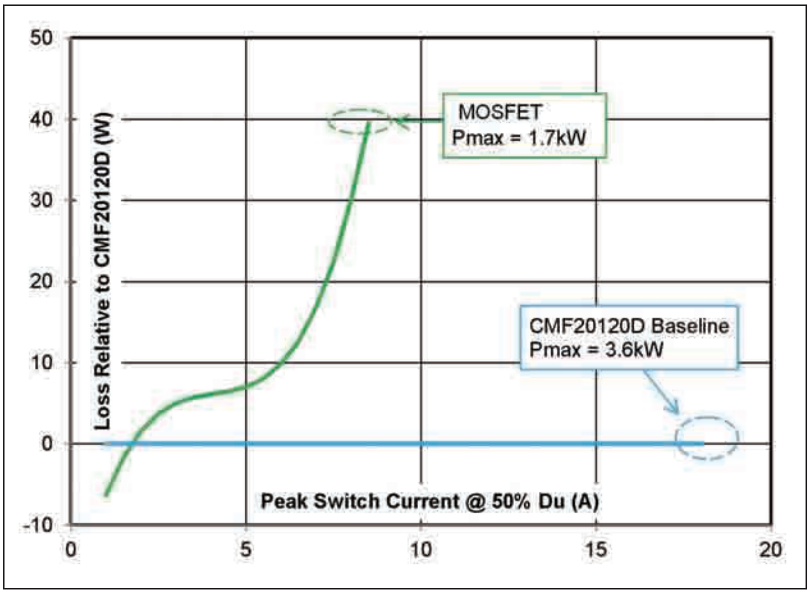

Figure 7: Relative switch loss comparison at 100 kHz (V_{DS}/V_{CE} = 800 V)

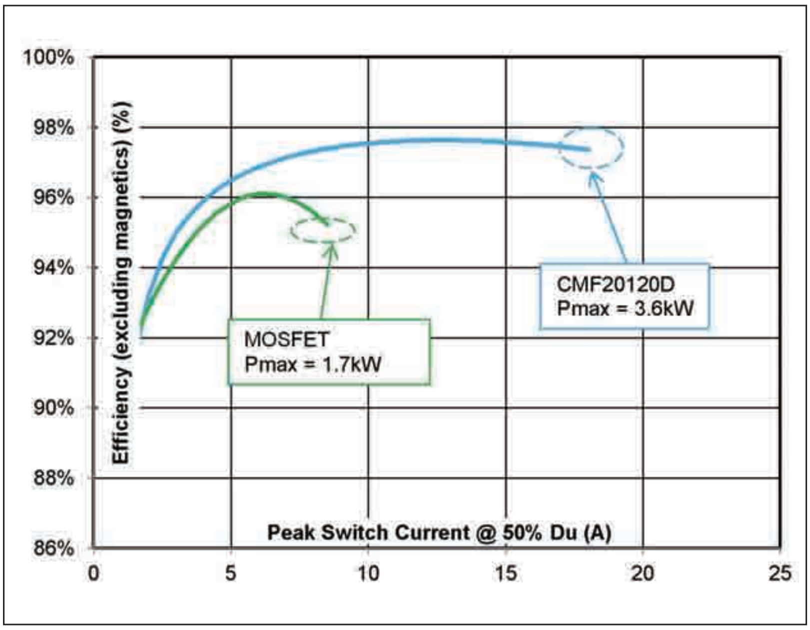

Figure 8: Efficiency (excluding magnetics loss) at 100 kHz (V_{DS}/V_{CE} = 800 V)

The input voltage to the SEPIC demonstrator was 400 V which resulted in the switch voltage of 800 V. The test was terminated when the thermal design limits were exceeded. The results show that the SiC MOSFET achieves the highest switch current of 17 A and delivered power is 3.6 kW. The Si MOSFET reaches a maximum switch current of 8.5 A equating to 1.7 kW delivered power. However, below 1.5 A the Si MOSFET has lower loss than the CMF20120D as indicated by the negative relative loss. This is attributed to the higher transconductance of the Si MOSFET affording slightly lower switching loss. However, the higher on-resistance causes conduction losses to increase dramatically thus dissipating higher power than the SiC MOSFET for the majority of the test currents.

The efficiency plot is shown in Figure 8. Once again the loss in the magnetics has been subtracted out in the overall efficiency to make it easier to see the differences in the devices. The results show that the SiC MOSFET achieves the highest efficiency overall. The delivered power at 18 A peak is 3.6 kW. The Si MOSFET reaches a maximum switch current of only 8.5 A equating to 1.7 kW delivered power, but its efficiency is slightly better than SIC MOSFET below 2 A.

Conclusion

A SEPIC converter platform to perform comparative loss measurements between switching devices under hard-switched conditions at high power can be used to emulate the actual switch stress in a given application without the need of a high power source and load. The source need only supply the circuit losses at half the desired switch test voltage. The demonstrator can be easily set to a particular switch voltage, current, frequency and case temperature to duplicate actual operating conditions that the switch will be exposed to in an actual application. The difference in loss between various switches can be robustly characterized by comparing the differences in DC input power. The loss and power handling capability of the CMF20120D 1.2kV 80 mΩ SiC MOSFET was compared with a 1.2 kV Si IGBT and a 1,2kV Si MOSFET. This article is derived from a paper given at PEE's Special PCIM 2012 Session [4].

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New 50 A SiC devices

AT PCIM Cree announced a new family of 50 A SiC devices, including the industry's first 1700 V 40 m_ SiC MOSFET, a 1200V 25 m_ SiC MOSFET and three SiC Schottky diodes (50 A 1700/1200/650 V). The new devices, available in die form, are designed for high-power modules for applications such as solar power inverters, UPS equipment and motor drives. Samples of all these high-power devices are available immediately, with production volumes targeted for fall 2012.

Wide Bandgap Power Devices in Megawatt Applications

Although researched for many decades, it is only recently that wide bandgap power devices have started to achieve an acceptable market entry level in terms of overall performance competitiveness in special applications with relatively lower power ratings. Therefore we will discuss the status of SiC in particular in connection with Megawatt applications and we will compare the potential benefits and challenges of introducing SiC technology. We will also discuss the widely proposed Si IGBT and SiC unipolar diode hybrid solution at 1.7 kV including experimental results and some important challenges to the acceptance of this concept in MW applications. **Iulian Nistor and Andrei Mihaila, ABB Corporate Research; Munaf Rahimo , Liutauras Storasta and Chiara Corvasce, ABB Switzerland Ltd., Semiconductors**

Driven by energy-efficient industrial and renewable energy applications, the demand for power semiconductors has been increasing rapidly. Hence, the longer-term prospects of the global power semiconductor market are very positive with forecasts showing 50 % market growth to each about $24.0 billion by 2015 [1]. In particular, the power module market has seen a tremendous growth, driven primarily by industrial motor drives, renewable energy, hybrid and electric cars, and consumer electronics. Today, the vast majority of the sold semiconductors and power modules are based on Silicon technology. Figure 1 shows the Silicon based power semiconductors and their power and frequency range in MW PE applications. While further innovations in Silicon based power semiconductors are continuously pushing the boundaries of performance [2-3], certain application requirements e.g. very high temperature operation (>200°C), very high switching frequency (>10kHz), and/or high voltages (>10kV) might prove to be more suitable for emerging Wide Bandgap (WBG) power semiconductors, such as SiC and GaN.

SiC technology overview

SiC has been referred extensively as the future material for power semiconductors, with significant developments in demonstrating the capability of the technology. For example with reference to Figure 1, SiC provides benefits in conduction losses for low frequency applications at very high voltages (>15kV) by avoiding the need for series connections of lower voltage Si devices. Similarly SiC is extremely suitable in applications at very high frequencies and low power levels due to the extremely low switching losses. The area of interest for MW applications is however at medium frequencies and medium voltages where currents can be significantly large.

However, there have been few aspects which have contributed to the fact that SiC is yet to fulfill its promised potential over the whole power range. They are all related to the advancement made in Silicon devices and applications in terms of power, losses, cost and system topologies.

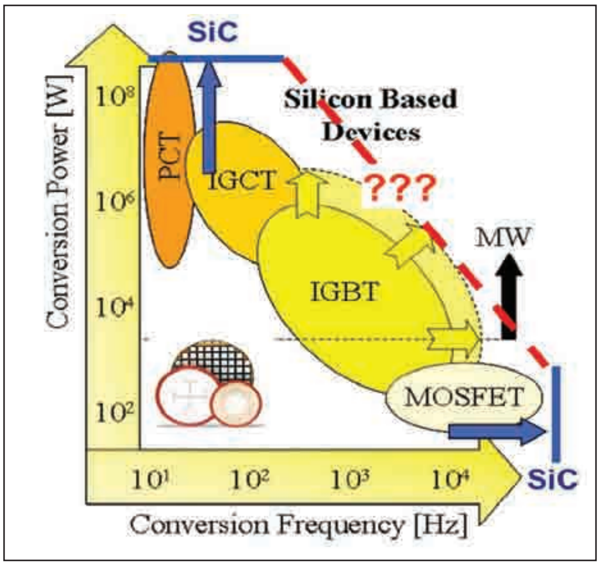

Figure 1: Power semiconductors and their power and frequency range in MW PE applications

Power: Single device/chip area remains limited in SiC due to defects and resulting yield aspects, temperatures above 200°C limited by package and increased losses for unipolar devices such as diodes and MOSFETS (strong positive temperature coefficient for on-state). Large area Si device concepts and processes are advanced with high operating temperature designs up to 175°C.

Losses: SiC bipolar devices suffer from high V_o and unipolar from strong on-state temperature coefficient. System and package designs not developed for low inductance and thus higher frequency applications and related EMI issues. Si devices are continuously advancing in terms of loss reduction and Integration. For higher power, Silicon devices are soft and are also targeting relatively higher frequency operation with fast versions. In the lower power range, the Super Junction MOSFET concept provides good performance.

Cost: With SiC system development for high frequency applications is required to compensate the higher device costs. Silicon devices continuously reaching higher performance/cost ratios through lower losses and integration solutions.

System topologies: Higher frequency trends evolving only in emerging and niche applications. Topology trends in established applications targeting lower frequencies and hence, lower on-state losses with existing Si based solutions.

While keeping these points in mind and still taking SiC as the main player in the

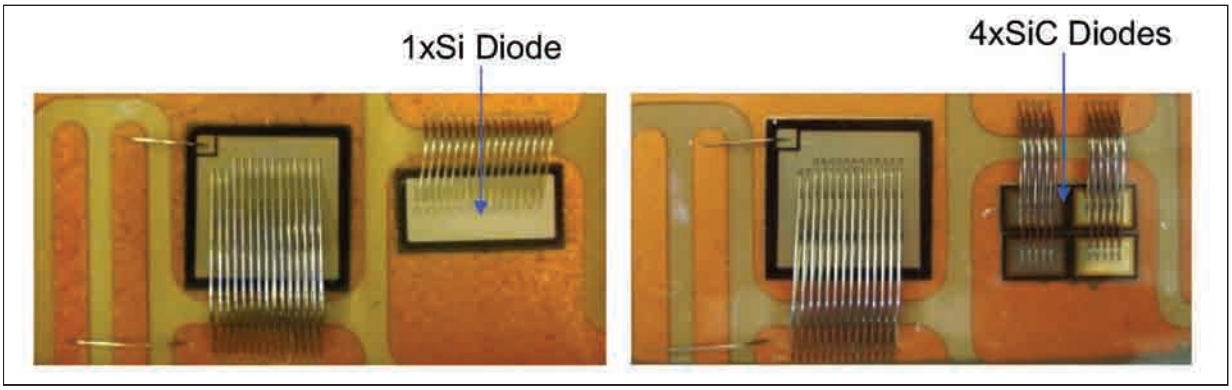

Figure 2: 1.7 kV/100 A Si IGBT chip paralleled with 1.7 kV Si Diode or 4 x 1.7 kV/25 A SiC Schottky diodes (right)

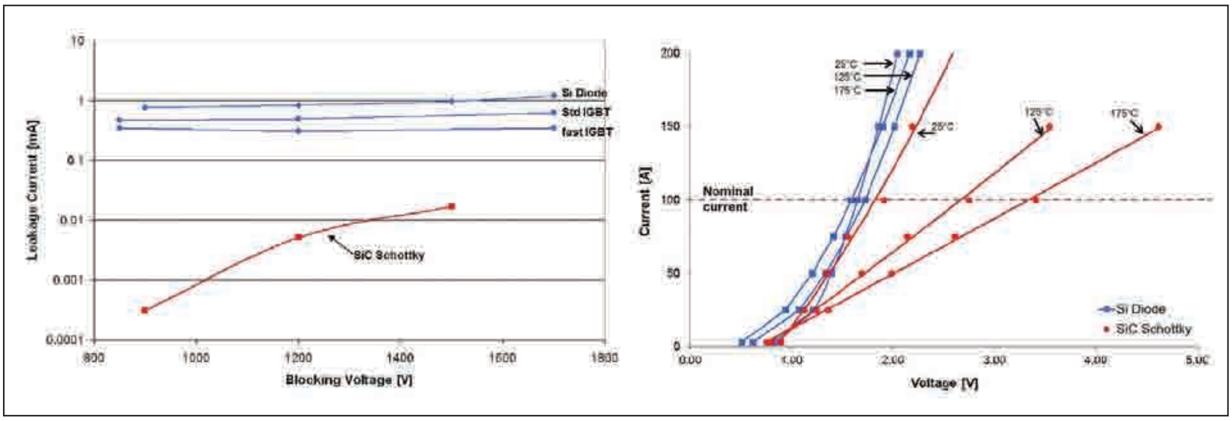

Figure 3: Static measurements on 1.7 kV Si/SiC Schottky diodes (leakage (left) and on-state (right))

high power WBG field, some new aspects are starting to "change the game" compared to the situation of the industry just a few years back. For example, most of the SiC technology developments were focused in the past either at voltages around 600V-1200 V or above 10 kV. Today we observe a development trend towards voltage levels of 1200V and 1700V, where many interesting applications for MW levels can be identified.

This trend also indicates that a certain performance/cost level is difficult to reach for SiC technology at voltages below 1200V, where the competition is fierce from Si SJ concepts and upcoming GaN on Si technologies. Furthermore from a manufacturing point of view, more material manufacturers have indicated that they are working on releasing 150 mm SiC wafers in the foreseeable future. It is therefore expected that such a step will definitely bring a much needed cost reduction of SiC technology. In addition, the first SiC 1200V MOSFETs have been released on the market, albeit at very high cost compared to Silicon semiconductors [4]. New market developments in renewable and automotive applications have brought forward the need for higher frequency/temperature devices.

In particular, the introduction of 1700 V SiC diodes with reasonably high current ratings (in excess of 20 A per chip) has provided an important step to exploit the hybrid solution with specially optimized fast Si IGBTs for MW applications. This approach shows strong potential for providing the best entry path for SiC in MW applications, since it combines a cost efficient solution using a Si switch with the benefits of the SiC diode technology. This concept has been reported before at different voltage levels [5,6], but these voltage levels were not very suitable for MW level applications. It is our target here to focus on the 1.7 kV voltage class and show that the optimization of the IGBT towards lower turn-off losses will provide a much improved solution in combination with SiC Schottky diodes for a total reduction of switching losses of nearly 40%

Evaluation of SIC potential

At substrate level one fast 1.7kV/100A IGBT chip has been paired either with one Si diode as a reference, and with four parallel SiC Schottky diodes to reach the same current ratings as shown in Figure 2. These substrates were fully characterized in static and dynamic electrical tests under nominal and SOA conditions and different temperatures.

The static measurements demonstrated the much improved high temperature performance of the SiC diode in terms of leakage currents as shown in Figure 3. The level of the leakage currents was very low and quite stable with the temperature when compared to the Si diode and different IGBT versions presented in the same graph.

In contrary to the exceptional reverse bias characteristics of SiC devices, the on-state tests show a strong increase with temperature for the unipolar SiC diode as shown in Figure 3 reaching relatively high on-state values when compared to Si diodes. This aspect raises concerns about the so called unipolar/bipolar voltage limit in SiC (about 200V in Si technology). In addition, such a device behavior will penalize the SiC diodes in rectifier applications below few kHz due to increased conduction losses.

On the expected positive side, SiC Schottky diodes show practically no reverse recovery losses compared to bipolar Si diodes as shown in Figure 4. In this case, the diode reverse recovery losses were reduced from 27.5 mJ for Si diodes to less than 1 mJ for SiC diodes. In addition, the recovery losses show little dependency on the test conditions including the commutating di/dt, the stray inductance and temperature. When the SiC diode is paired with a Si IGBT, this property

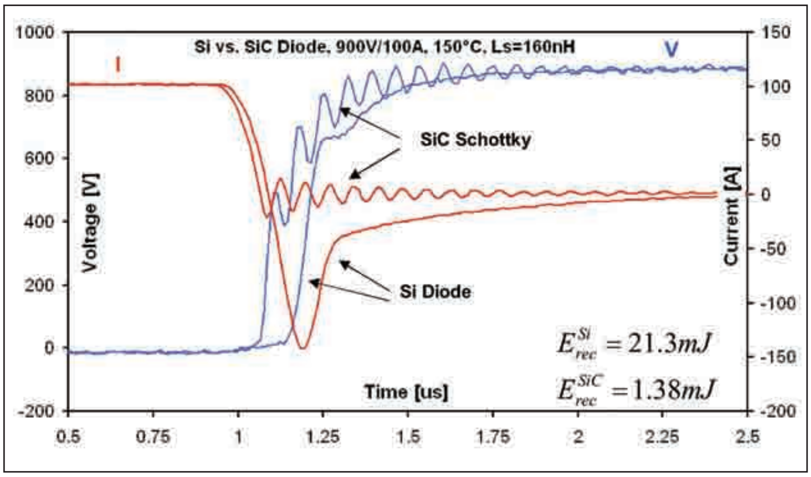

Figure 4: **Reverse recovery waveforms of 1.7kV Si Diode compared to SiC Schottky diode**

can prove to be advantageous in reducing the turn-on switching losses of the IGBT. However, the benefit obtained only from reducing the turn-on losses cannot justify the higher cost of using SiC device. Therefore the turn-off losses of the IGBT have to be reduced also to achieve further switching loss reductions in the combined solution.

An optimized 1.7kV fast IGBT chip has been developed on the SPT+ platform [7]. This optimized IGBT chip has approximately 25 % lower turn-off losses than a standard IGBT chip, and consequently its on-state is increased by about 10 %. With further reduction of the emitter efficiency, the turn-off losses could be reduced by 44 %. Such an extreme low injection efficiency design might bring undesirable performance in terms of short circuit ruggedness, therefore we estimate an optimum fast IGBT design to deliver 2.45 V on-state with 19 mJ turn-off losses at 100A. A comparison of turn-off waveforms between standard and fast IGBTs is shown in Figure 5.

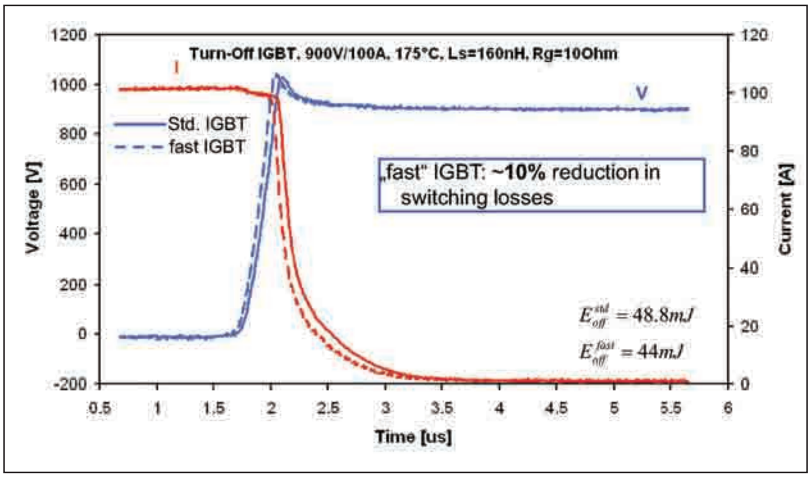

Figure 5: **Turn-off waveforms of standard and fast 1.7kV IGBTs (left) and turn-on waveforms of fast 1.7kV IGBTs in parallel with Si and SiC Schottky diodes showing the significant reduction in turn-on losses due to the absence of the reverse recovery charge in the unipolar SiC diode**

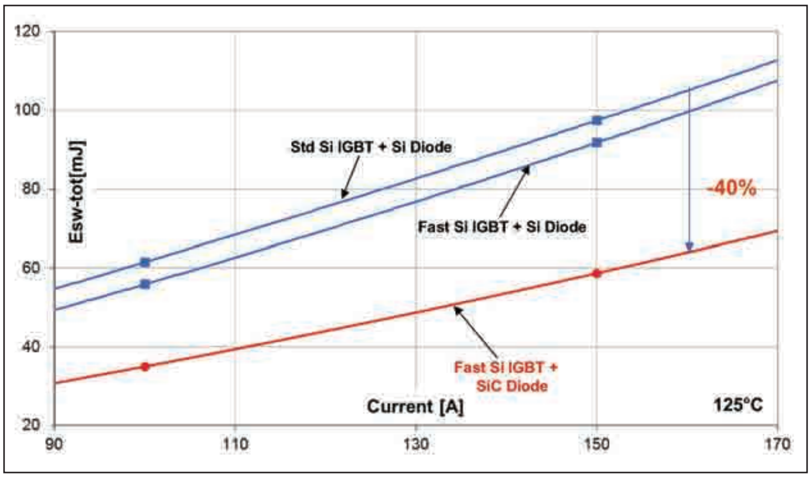

Figure 6: **Total switching losses comparison for 1.7 kV fast SPT+ IGBT in parallel with Si or SiC diodes**

It was shown in our measurements that by combining the fast IGBT with SiC Schottky diodes, a further reduction of up to 60 % of the turn-on switching losses could be achieved as shown in Figure 5 (right). Further reduction of turn-on losses would be possible by reducing the value of the gate resistor Rg , but with the risk of increasing oscillations in the system. At high Rg values, the turn-on losses are dominated by the IGBT chip itself. Reducing further the Rg increases the speed of the turn-on process, but also the dv/dt and di/dt resulting in oscillations that could impact the electro-magnetic noise of the system. Hence, special low inductance solutions are required at package and system levels to tackle this issue. Overall, we estimated that the pairing of the 1.7kV fast IGBT chip with SiC Schottky diodes has the potential to reduce the total switching losses ($E_{sw} = E_{on} + E_{off}$) by about 40 % compared to the full Si approach as shown in Figure 6. Because the switching losses have a direct impact on the switching frequency of the semiconductor and application, it can be inferred that the hybrid solution could operate at higher frequencies than its Si counterpart.

It also noticeable the penalty of SiC diodes at low switching frequencies due to the strong degradation of the unipolar behavior with temperature.

Although established for low voltage applications, the method of hard switching of semiconductors is still debated in MW applications. Some technical solutions such as Power Electronic Transformers and in general any DC/DC isolated converters rely on alternative approaches such as resonant type topologies, where the soft switching removes the constrains on the diode component [8]. Such resonant applications could still benefit from increased switching frequencies by minimizing the size of the high frequency Isolation transformer, but this would require a full SiC module including a MOSFET or JFET switch.

For other applications in MW range, such as MV drives and transmission of high power over large distances (HVDC), the trend points towards multilevel topologies. Such topologies rely on an increased number of semiconductor stages, each stage being switched on and off at a relatively low frequency (sub 1 kHz). In our view, for such multi-level approaches, the hybrid Si + SiC approach does not prove to be a suitable solution. Instead, a full SiC solution using higher voltage switches might prove of more technical interest in this case [9].

Conclusions

Overall, a reduction of up to 40% of the total switching losses is demonstrated by using a hybrid approach combining specially designed fast IGBT chips and SiC Schottky diodes. This has very important consequences on the system design, allowing a 3 to 5 fold increase in the operating frequency without derating of output power capability. In order for this increase of efficiency to be fully utilized, further developments haue to take place in reducing the package parasitics and system layout, for example by developing 1.7 kV phase leg IGBT modules. Given that the challenges related to the packaging will be solved in the coming years, we see the hybrid technology approach as a first entry point for SiC technology in MW PE applications. Nonetheless, in the long run this solution limits the extension of SiC only to diodes and the operating temperatures will remain limited by the Si IGBT switch and current packaging concepts. This article is derived from a paper given at PEE's Special PCIM 2012 Session [10].

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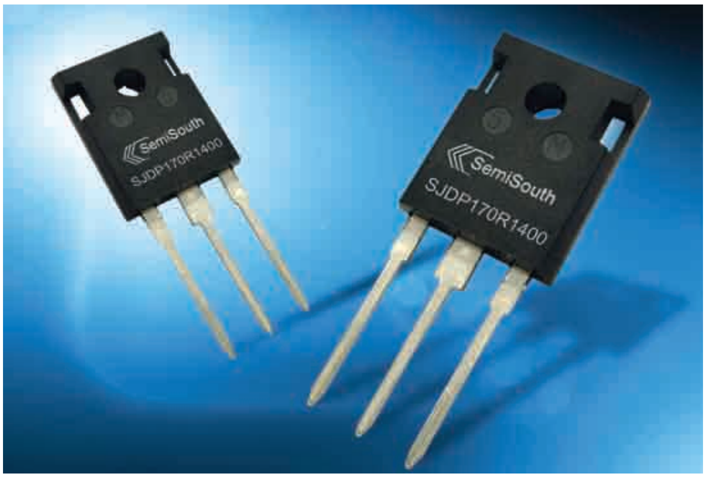
SiC JFETs for 3-Phase Power Supplies

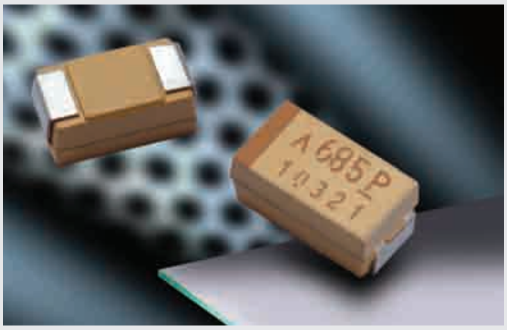


SemiSouth announced a 1700 V/1400 mΩ SiC JFET which simplifies start up circuit design in 3-phase auxiliary power supplies. Today's solutions either use an HV bleed resistor which results in a slow start-up at low line voltages and a high quiescent power loss, or are MOSFET-based which necessitate overload protection and can suffer from high power losses in the MOSFET under fault condition e.g. short circuit. By using a depletion mode JFET, designers can achieve a fast start-up using no extra components or no extra heat sink. The SJDT170R1400 will come in a newly developed SMD D2PAK-7L package in order to simplify PCB layout and optimize switching performance due to lower inductance. This package will have a high creepage distance of 6.85 mm in order to support 1700 V applications and is sized of 16 x 10 x 4.4 mm. SemiSouth is initially sampling the normally on 1700 V/1400 mΩ SJDP170R1400 in TO-247-3L packaging; the SJDT170R1400 in surface mount D2PAK-7L high creepage package will be sampled in Q3/2012.

The company is also sampling 650 V/55 mΩ SJDA065R055 SiC JFETs. Typical applications for these TO-220-packaged devices are solar inverters, SMPS, PFC circuits, induction heating, UPS and motor drives.

www.semisouth.com

HV SMD Polymer Tantalum Capacitors



AVX Corporation has developed 63 V and 75 V single-anode tantalum polymer capacitors. Part of the TCJ Series polymer tantalum capacitors, these new surface mount devices deliver high capacitance, high voltage and low ESR values in a small case size. Available in 1 µF/63 V, 4,7 µF/63 V, 10 µF/63 V and 4.7 µF/75 V, 6.8 µF/75 V rated voltages, the TCJ Series polymer tantalum capacitors maintain 20 % recommended voltage derating, thus extending the usable voltage range. This combination brings polymer tantalum technology to a number of new applications and enables the development of a new generation of power supplies.

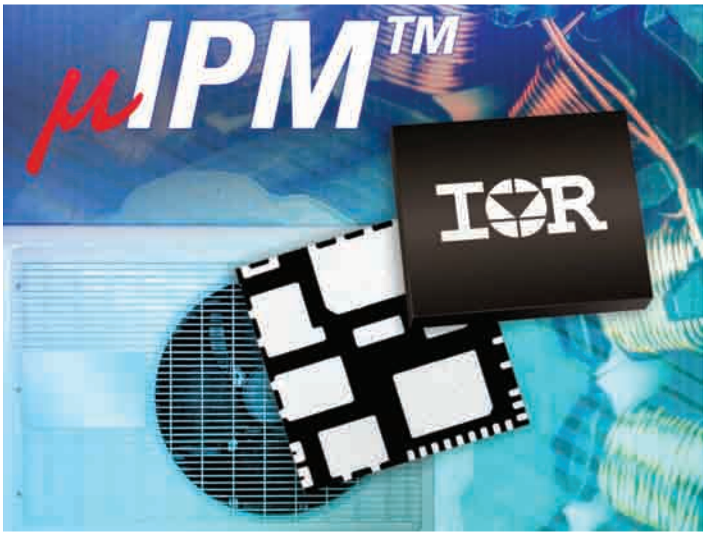
www.avx.com

SiC JFET with Driver

Infineon Technologies introduced the new CoolSiC 1200V SiC JFET family which have dramatically lower switching losses compared to IGBTs, which allow higher switching frequencies to be used without sacrificing overall system efficiency. In order to ensure that the normally-on JFET technology is safe and easy to use, Infineon has developed a concept which is called Direct Drive Technology. In this concept, the JFET is combined with an external low voltage MOSFET and a dedicated Driver IC which ensures safe system start-up conditions as well as fast and controlled switching. The CoolSiC JFET features a monolithically integrated body diode that has a switching performance comparable to an external SiC Schottky barrier diode. Samples of the CoolSiC JFET products as well as the Driver ICs are available in the second quarter. First OEM ramp-ups are expected in the first half of 2013.

www.infineon.com/coolsic

Micro Power Modules



International Rectifier introduced a family of integrated, ultra-compact µIPM power modules for appliance and light industrial applications including compressor drives for refrigeration, pumps for heating and water circulation, air-conditioning fans, dishwashers, and automation systems. By utilizing an innovative packaging solution, the µIPM family offers up to a 60 % smaller footprint than existing 3-phase motor control power ICs. Available in a 12 x12 x 0.9 mm PQFN package, the µIPM family comprises fully integrated 3-phase surface-mount motor control circuit solutions utilizing PCB copper traces to dissipate heat from the module, providing cost savings through a smaller package design and even eliminating the need for an external heat sink. By using standard packaging QFN technology, assembly is simplified by eliminating through-hole second pass assembly and improving thermal performance compared to traditional dual-in-line module solutions. The µIPM family offers a scalable power solution with common pin-out and package size. Featuring high-voltage FredFET MOSFET switches specifically optimized for variable frequency drives and driver ICs, the µIPM offers DC current ratings ranging from 2 A to 4 A and voltages of 250 V and 500 V.

www.irf.com

60/120 V MOSFETs for Synchronous Rectification

Toshiba Electronics Europe (TEE) has expanded its family of low-voltage, high-speed MOSFETs with 60 V and 120 V devices that save space and reduce losses in secondary synchronous rectification designs. Targeted at switch mode power supplies, the sixteen new trench MOSFET devices are based on Toshiba's eighth generation, U-MOSVIII-H process. This process delivers improvements in trade-off characteristics between low on-resistance and low input capacitance, as well as improving switching speeds and minimising radiated noise. Available in either TO-220 or TO-220SIS 'smart isolation' package formats, the new range comprises eight 60 V MOSFETs and eight 120 V MOSFETs. By offering lower FOM compared to previous generations, the new MOSFETs operate with lower conduction and drive losses. Among the new MOSFETs are the TK100E06N1 (TO-220) and TK100A06N1 (TO-220SIS) 60 V devices with typical on-resistance of 1.9mΩ and 2.2mΩ respectively. The 120 V series includes TK56E12N1 (TO-220) and TK56A12N1 (TO-220SIS) devices with respective typical on-resistances of 6.1 mΩ and 6.5 mΩ.

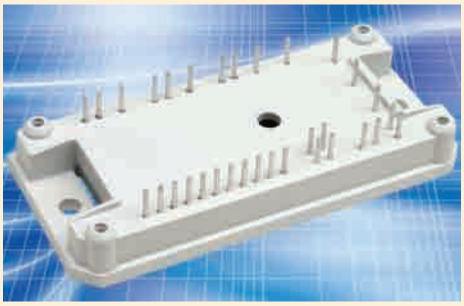
www.toshiba-components.com

User-Programmable Current Transducers

LEM's new HO series are open-loop devices, based on Hall-effect current sensing technology, that measure AC, DC or pulsed currents with a nominal value of 8, 15 or 25 ARMS, with a response time of 2 to 6 _s. Both of these parameters, and several others, are user-programmable by a simple serial digital bit-sequence, generated by the system's host microcontroller. Other parameters that are user-programmable include reference voltage, over-current detection limits, fault reporting and low power mode. The HO series delivers its output as a scaled analogue voltage; in most systems this will be converted to a digital value by an ADC which requires a reference voltage. The designer can program the HO-series transducer to output a reference of 0.5, 1.5, 1.65 or 2.5 V on a dedicated pin. Alternatively, the HO-series can be configured to make measurements relative to an external reference. The HO provides offset and gain drift figures twice as good (over the temperature range -25 to +85ºC) as previous-generation open-loop Hall-effect-ASIC based transducers. It achieves a typical accuracy of 1 % and 2.8 %, at +25°C and +85°, respectively, without offset, and with a high level of insulation between primary and measurement circuits.

www.lem.com

Modules for Single-Phase Solar Inverters



Vincotech offers a new family of power modules for transformer-based, single-phase solar inverter applications and switch-mode power supplies. These modules (flowSOL 1 BI + RI (T)) have been engineered for use in a new universal power module design with an IGBT or MOSFET in all inverters. The 600/650 V/50 A/80 mΩ modules are packaged in Vincotech's standard flow 1 housing measuring 66 mm by 33 mm and 12 mm in height. For transformer-less solar applications, the new flowSOL 1 BI (TL) modules rated 600/650 V/50 A/41 mΩ provide full reactive power capability and satisfy the highest demands for efficiency (up to 99%). They are quipped with MOSFETs plus Si or SiC diodes.

www.vincotech.com

Advanced Telecom Bus Converter

Ericsson has unveiled the first model in its second generation of digital Advanced Bus Converter (ABC) products based upon the FRIDA II platform. This fully regulated digital DC/DC converter is based on a 32-bit ARM microcontroller operating with advanced firmware. The FRIDA II firmware combines Ericsson IP together with a series of functionalities to optimize switching parameters and reduce energy consumption. The firmware is not just limited to energy management, but includes a number of features including the ability to handle input voltage transients with slew-rates of up to 0.5 V/µs, while keeping the output voltage within ±10 % and ensuring that the output voltage does not trigger over-voltage protection. It also offers the highly efficient management of pre-bias start-up operation and a fully controlled shutdown process, avoiding voltage spikes that could cause an avalanche condition in the secondary-side synchronous rectification MOSFET. Designed to power telecom and datacom applications, the BRM456 is available in two input voltages ranges: 36 V to 75 V, delivering output power of 420 W; and 40 V to 60 V, delivering output power up to 468 W. Output voltage can be adjusted across a range from 4.0 V to 13.2 V via PMBus commands, making the BMR456 suitable for Dynamic Bus Voltage operation resulting in the reduction of energy consumption when communication data traffic is low. The BMR456 delivers a typical efficiency of 96.5 % and exhibits flat curve behavior from 14 to 100 % load.

www.ericsson.com/powermodules

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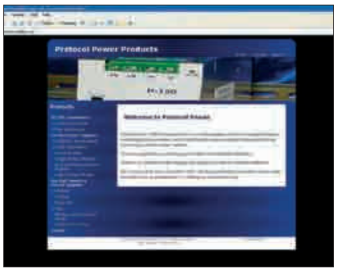

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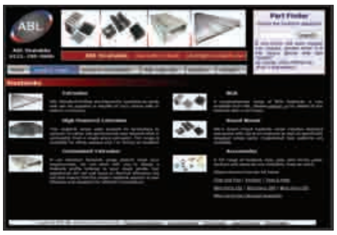

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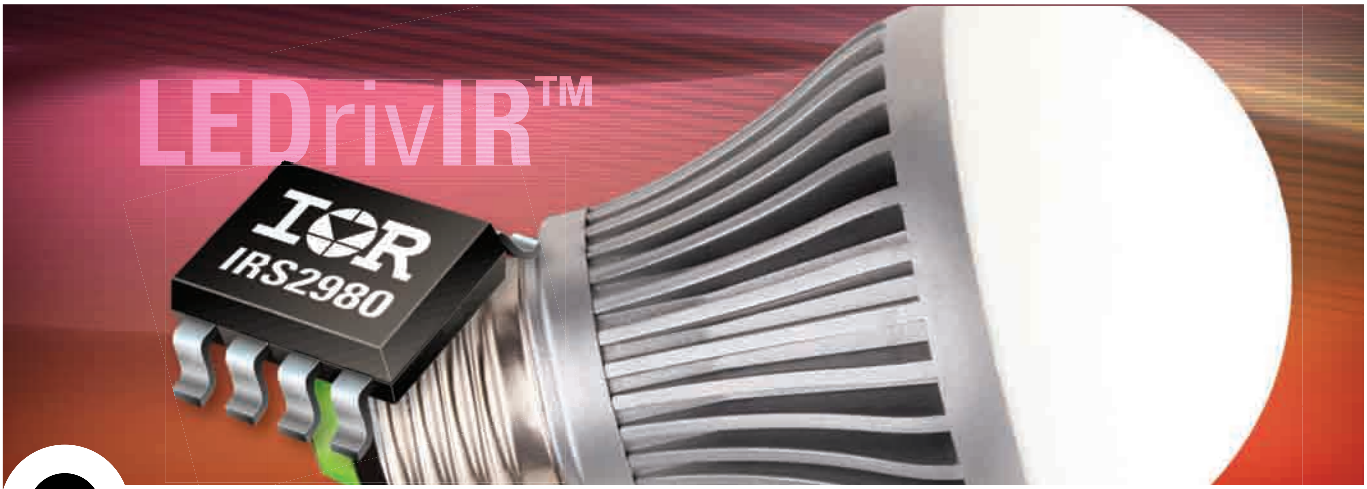
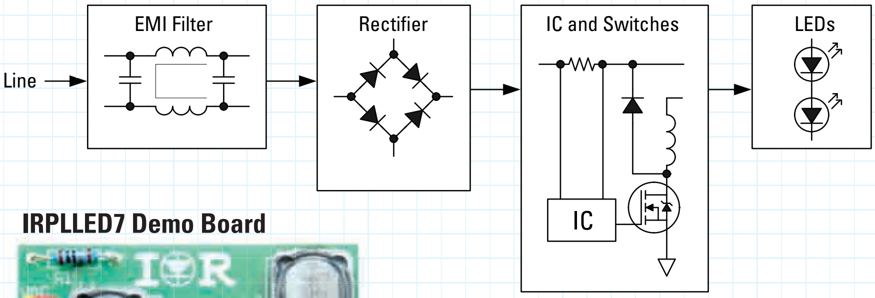
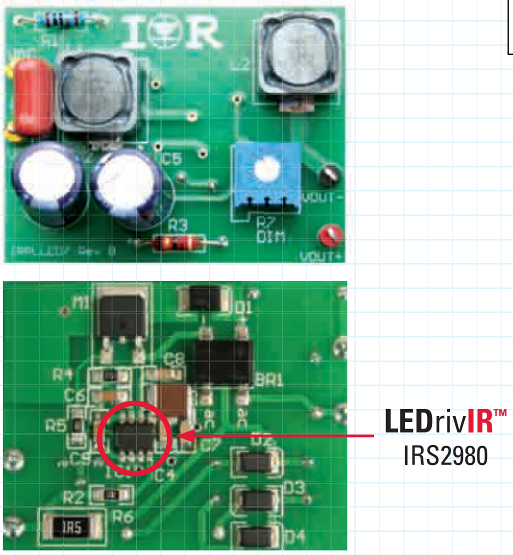


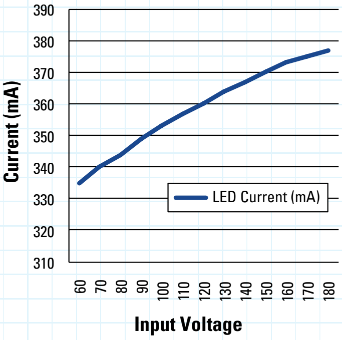
High-Voltage Buck Control ICs for Constant LED Current Regulation



IRPLLED7 Demo Board



IRPLLED7 Demo Board
LED Current vs Input Voltage



Part Number	Package	Voltage	Gate Drive Current	Startup Current	Frequency
IRS2980S	SO-8	450V	+180 / -260 mA	<250 μA	<150 kHz
IRS25401S	SO-8	200V	+500 / -700 mA	<500 μA	<500 kHz
IRS25411S	SO-8	600V	+500 / -700 mA	<500 μA	<500 kHz

IRS2980 Features

- Internal high voltage regulator
- Hysteretic current control
- High side current sensing
- PWM dimming with analog or PWM control input
- Free running frequency with maximum limiting (150kHz)

IRS2980 Benefits

- Low component count
- Off-line operation
- Very simple design
- Inherent stability
- Inherent short circuit protection

Demo Board Specifications

- Input Voltage 70V to 250V (AC)
- Output Voltage 0V to 50V (DC)
- Regulated Output Current: 350mA
- Power Factor > 0.9
- Low component count
- Dimmable 0 to 100%
- Non-isolated Buck regulator

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