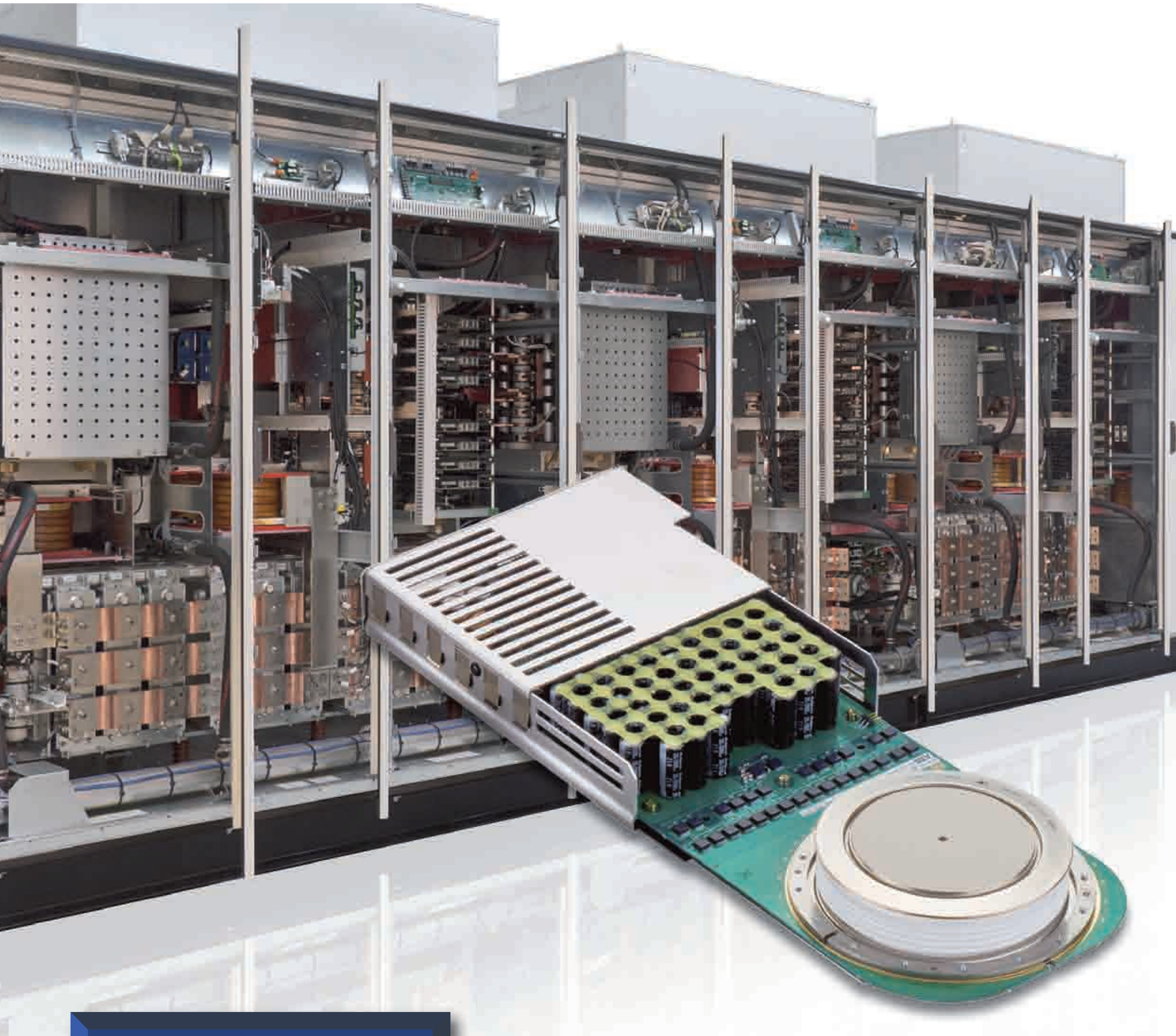
POWER ELECTRONICS EUROPE

ISSUE 5 – August 2012 www.power-mag.com

POWER SEMICONDUCTORS

Past, Present and Future of HPT-IGCT



THE EUROPEAN JOURNAL FOR POWER ELECTRONICS AND TECHNOLOGY

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Power semiconductor devices

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Circulation and subscription: **Power Electronics Europe** is available for the following subscription charges. **Power Electronics Europe**: annual charge UK/NI £60, overseas $130, EUR 120; single copies UK/NI £10, overseas US$32, EUR 25. Contact: DFA Media, Cape House, 60a Priory Road, Tonbridge, Kent TN9 2BL Great Britain.
Tel: +44 (0)1732 370340. Fax: +44 (0)1732 360034. Refunds on cancelled subscriptions will only be provided at the Publisher's discretion, unless specifically guaranteed within the terms of subscription offer.
Editorial information should be sent to The Editor, **Power Electronics Europe**, PO Box 340131, 80098 Munich, Germany.

Printed by: Garnett Dickinson.
ISSN 1748-3530

COVER STORY

Past, Present and Future of HPT-IGCT

The integrated gate-commutated thyristor (HPT-IGCT) is a state-of-the-art bipolar turn-off device for high power applications. The IGCT was introduced about 15 years ago and has established itself as a preferred technology for handling very high power. The applications range from industrial drives and track-side supplies to power quality and high-current breakers. The first device in the HPT-IGCT family was the asymmetric 4500 V device 5SHY 55L4500 released in 2009. In 2010, 5SHY 42L6500 followed, an asymmetric 6500 V device and in 2012, yet another asymmetric device 5SHY 50L5500 rated 5500 V was released. In this article we take a look at the newest member - the 5.5 kV asymmetric HPT-IGCT and we will also take a look at one interesting device in the pipeline.

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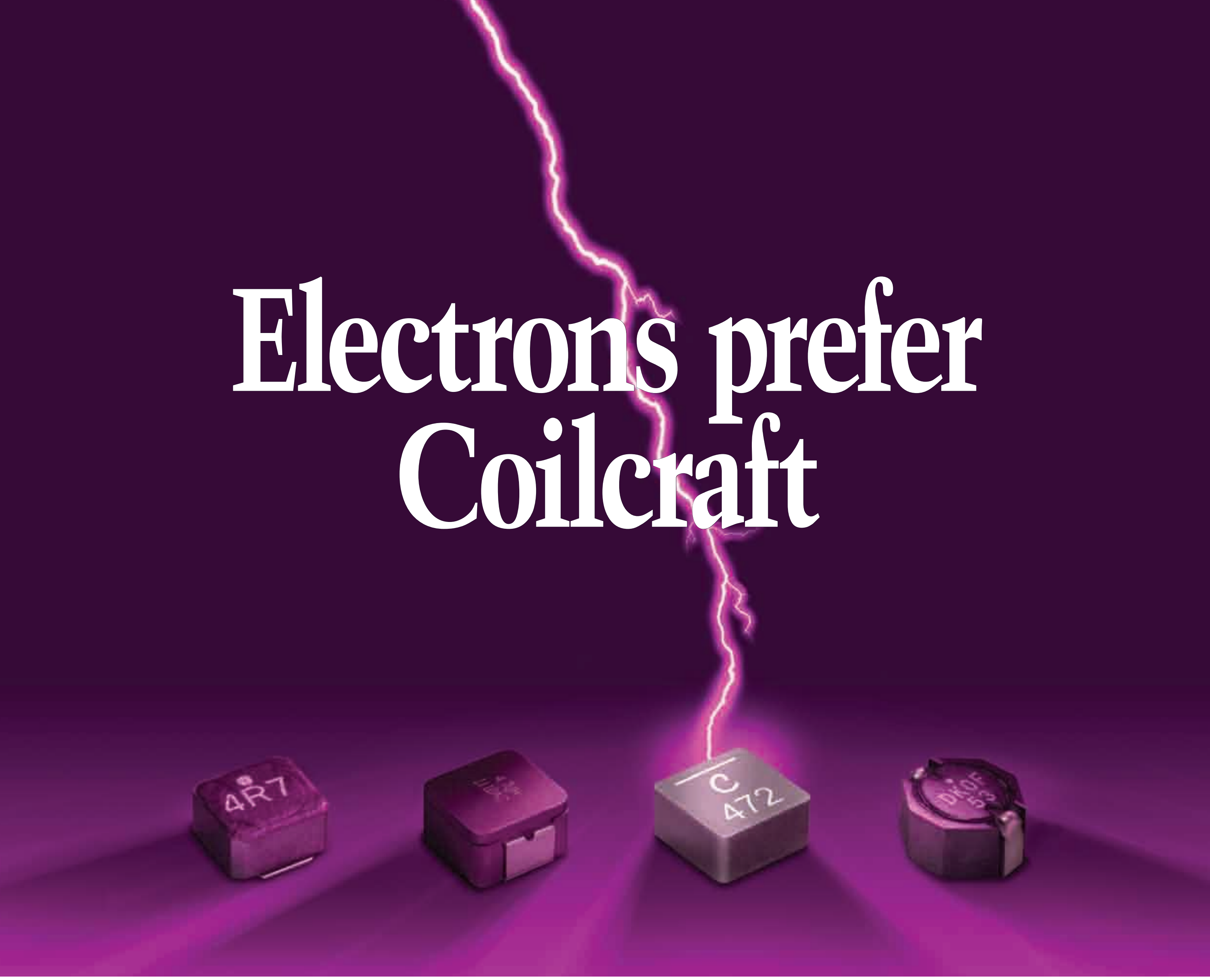

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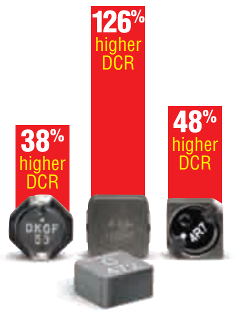

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Growth Ahead with Regional Shift

The global power discrete and module market is forecast to grow by $9 billion to reach $26.2 billion in 2016, according to a new report from IMS Research. With revenues growing 9 percent from 2010, it is clear that 2011 was, at best, an average year for the power semiconductor market. This follows the dramatic market fall in 2009 and spectacular recovery in 2010, so perhaps the industry was ready for a "normal" year 2011.

Although market conditions have remained flat in the first half of 2012, the longer-term prospects remain positive. According to market researcher Yole Développement the market for semiconductor devices (discrete, modules and ICs) dedicated to the power electronics industry will reach $20 billion in 2012. These figures underline the robustness of the power electronics industry in its potential application fields, though some regional shift may occur. With applications as diversified as hybrid cars, PV inverters, lighting, energy, and voltage ranging from a few volts to a few thousands volts, power electronics is and will remain one of the most attractive branches of the semiconductor industry over the next decade.

In example, 2011 global PV inverter shipments grew by more than 12 percent, despite the excess inventory overhang from the prior year, and reached 27 GW, but the European market shrank considerably. Europe's dominance of the PV inverter market is predicted by IMS to continue to wane due to its two biggest markets, Germany and Italy, facing significant reductions in their annual installations. Europe's share of PV inverter shipments and revenues was over 80 percent in 2010; however this is forecasted to fall to less than 40 percent in 2016 and revenues not to return to 2011 levels in the next five years. This in itself presents a huge challenge to suppliers, which are mainly European, with the majority of their facilities and customers located in that region. Analysis showed that whilst the European outlook is not so bright, the global picture for PV inverter suppliers looks somewhat better; highlighting the fragmenting nature of the industry that now needs to look to emerging markets for future growth. Global shipments are predicted to continue growing at a double-digit rate over the next five years, with revenues exceeding $9 billion by 2016. In 2012 the market is forecasted to grow by just 3 percent to hit $7 billion for the first time.

Recognizing these trend PCIM 2013 conference focuses on "Wind and Solar - Integration, Challenges and Solutions". Both are growing rapidly and thus provide huge opportunities for power electronics.

Regarding power semiconductors, IGBTs account for $1.6 billion in the medium to high voltage sector. And the SJ MOSFET market will reach $567 million by the end of this year. GaN and SiC also have a chance to outdo Silicon performance and enhance inverter capabilities. With access to lower-cost material, the SiC industry now has the chance to ramp up and get organized. However, apart from the PFC business, technological capabilities of SiC show that it will surely be dedicated to high power/voltage applications. Also, SiC companies have appeared in China, which will definitely provide competition and tougher access to local markets. The GaN industry is mostly a US business with some pioneers like MicroGaN from Germany, NEC and Powdec showing there is a trend to globalize the GaN manufacturing industry. From MicroGaN's perspective, today 4-inch GaN-on-Silicon wafers with the appropriate epi layer thickness are available, which make 600V devices feasible. The material quality improvement in 6-inch GaN-on-Silicon is closely monitored and it is a matter of homogeneity progress in the epi quality and thereby a matter of yield improvement to switch to 6-inch utilization. In order to enable commercialization with a smaller wafer diameter, MicroGaN developed a new technological approach, which cuts die size for given performance into half. This is only one example for European innovations which Power Electronics Europe has supported at PCIM Europe 2012 and will continue to support in 2013.

Have a good time by reading this issue!

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PEE Editor

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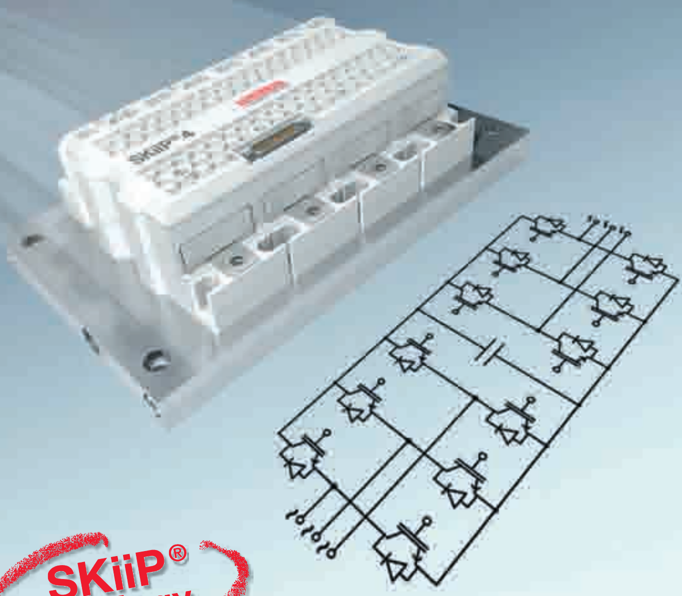

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New Power Technologies Ahead

"In 2012, the market for semiconductor devices (discrete, modules and ICs) dedicated to the power electronics industry will reach $20 billion," confirmed Brice Le Gouic, Activity Leader, Power Electronics at Yole Développement. With applications as diversified as hybrid cars, PV inverters, lighting, energy, and voltage ranging from a few volts to a few thousands volts, power electronics is and will remain one of the most attractive branches of the semiconductor industry over the next decade.

Already well-established in the market, IGBTs account for $1.6 billion in the medium to high voltage sector. In the new report "Status of the Power Electronics Industry", Yole describe a trend towards decreasing voltage range in order to target consumer applications such as TVs, computer adapters and cameras, in order to access more segments. At the same time, SJ MOSFETs present in these applications offer faster switching frequencies and competitive cost. "We estimate the SJ MOSFET market will reach $567 million by the end of the year."

GaN and SiC also have a chance to outdo Silicon performance and enhance inverter capabilities. However, materials are still expensive and the technology is not yet ready. On the other hand, both of these materials can benefit from their developed status in the LED industry, and plenty of LED players paying attention to the opportunity that power electronics represent. GaN and SiC are not mature yet for the power electronics market: the first one requires technological enhancement of the manufacturing process, especially for epitaxy thickness, and the second one is an expensive material that does not allow implementation within consumer-like businesses. Segmentation between technology and the power/voltage range will take place, and some segments will only accept one « best » technology.

Each technology has a particular industry structure

While SJ MOSFETs welcome new players and foundry service suppliers, the IGBT dies' industry is becoming consolidated thanks to the presence of large players involved in many applications, such as Infineon, Mitsubishi Electric and Fuji. However, the IGBT (and SJ MOSFET) modules business is increasing, and we see new players entering to provide solutions for cooling, interconnections, substrates, packaging, and gel.

On another note, the SiC industry, which has been led by CREE, is now an interesting playground for new players. With access to lower-cost material, the SiC industry now has the chance to ramp up and get organized. However, apart from the PFC business, technological capabilities of SiC show that it will surely be dedicated to high power/voltage applications. Also, SiC companies have appeared in China, which will definitely provide competition and tougher access to local markets.

At this point in time, the GaN industry is mostly a US business. International Rectifier, EPC, Transphorm, Microsemi and GaN Systems now propose fully off-the-shelf or customized products. However, some pioneers like MicroGaN from Germany, NEC and Powdec are showing there is a trend to globalize the GaN manufacturing industry. At the same time, the market is still soft and LED players are considering using their technological platform to enter the power electronics field, which will be very much low power/voltage-oriented.

Because power semiconductors are "just a piece" of the power electronics industry, the power semiconductor industry has to answer requirements from a bigger system: the inverter. For example, some expensive solutions are still not implemented, even if device and module performance are much higher than current output.

Geographical positioning is also critical in the power electronics area, especially with the boom in China and other emerging countries, but also because several applications (PV, wind, electric vehicles) are supported by local governments.

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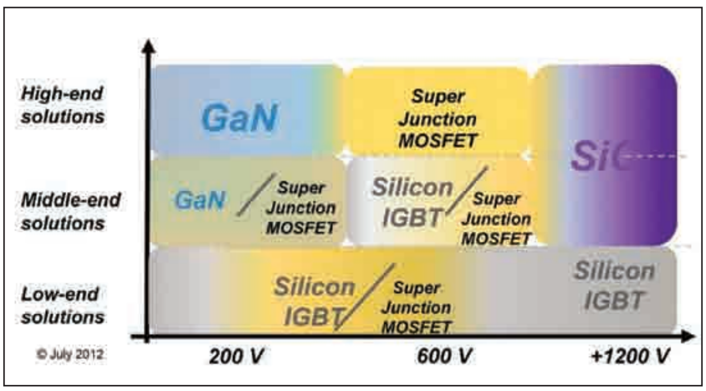

Power semiconductors positioning forecast 2015 Source: Yole Développement

Power Semiconductor Market to Grow $9 Billion Over the Next Five Years

The global power discrete and module market is forecast to grow by $9 billion to reach $26.2 billion in 2016, according to a new report from IHS/IMS Research. Following good growth in the first half of 2011, the market fell away in the second to finish with only 9 percent growth over the whole year. Although market conditions have remained flat in the first half of 2012, the longer-term prospects remain positive.

With revenues growing 9 percent from 2010, it is clear that 2011 was, at best, an average year for the power semiconductor market. This follows the dramatic market fall in 2009 and spectacular recovery in 2010, so perhaps the industry was ready for a “normal” year. However, with business confidence uncertain and the recovery stalling, what are the prospects for the future? According to IMS Research there remains cautious long-term optimism, with the market projected to grow by almost $9 billion to $26 billion from 2011 to 2016, a compound annual growth rate of 8 percent.

The market for power semiconductor modules again grew faster than that for discrete power semiconductors in 2010, increasing by 32 percent to close on $4.6 billion. The power module market growth is continuing in 2012 despite slowing demand, as reduced business confidence is felt in industrial market sectors. “Power module revenues are predicted to grow by 14 percent in 2012 , and to be 80 percent higher than in 2011 in 2016” stated senior analyst Richard Eden.

The power discrete market was worth an estimated $13 billion in 2011, having grown by just over 2 percent from 2010. Continued high demand for discrete IGBTs accounted for nearly all the growth. “The sudden surge in discrete IGBT demand was fuelled by sales of domestic appliances such as room air-conditioning and variable speed washing machines in the Chinese market,” added Eden. “In contrast, sales of standard power MOSFETs and thyristors actually declined slightly in 2011.”

A high proportion of discrete power semiconductors are used in relatively fast-moving commodity items such as flat-screen televisions, notebook computers and mobile phone adapters. Sales of these products depend heavily on consumer confidence and the health of the global economy. Sales of power semiconductors in those sectors either declined or achieved negligible growth in 2011, and are not forecast to deliver much growth in 2012. Power semiconductor market growth will therefore be driven by increased content, either to improve power conversion efficiency or add functionality. In contrast, growth is forecast to accelerate in the automotive, renewable energy and transportation sectors. Overall discrete power semiconductor market growth is predicted to remain less than 5 percent in 2012; the market is forecast to reach almost $18 billion in 2016.

The latest findings and analysis on this important market can be found in IMS Research’s “The World Market for Power Semiconductor Discretes & Modules 2012” report, due for publication in August 2012.

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Key Applications for 400 V DC Power Technology

Rising energy costs and power demand, combined with mainstream adoption of renewable energy sources, are driving adoption of new power architectures, such as 400 V DC, that enable more efficient networks and businesses.

Direct and alternating current (AC) technologies have been evolving since Tesla and Edison competed in the late 1800s to establish a distribution method for the electric grid. At that time, technologies were not available to safely and economically use DC power over long distances and AC power won out on the grid. Today, long-distance DC power use is cost effective, DC-based renewable energy is proliferating, and most technology equipment operates on DC power. The grid still distributes AC power, however, creating growing inefficiencies in our power-hungry world. “Recent advances in power conversion technologies, combined with rapidly increasing DC-based equipment growth, have created an environment where DC power distribution should be, and is being, actively considered,” said Mark Murrill, director of 400V DC power initiatives for Emerson Network Power. “Global architecture standards required for widespread implementation of 400 V DC are well under way, as demonstrated with the European Telecommunications Standards Institute EN 300 132-3-1 standard released in February 2012. As more and more vendors support this standard, the adoption of 400 V DC will begin to rapidly increase in various applications and further standards will be clarified and adopted.”

Emerson Network Power currently sees four primary applications for 400V DC technology: telecom central offices, data centres, commercial buildings, and transportation - each with its own drivers for adoption.

Reducing copper and costs in the central office

Unlike the grid, telecommunications networks have long used DC distribution, largely for its high reliability and good signal quality performance. As telecom equipment has moved to Silicon-based DC technology, alignment between existing DC power distribution and DC-driven equipment is already in place, but cost and efficiency gains are still possible. For example, 400 V DC is especially suited for high power delivery over long distances, because it reduces installation and operational costs and improves cable management versus -48 V DC. These benefits are realised due to at least an 80 percent reduction of copper wire used, affecting both the cost of and time needed for installation. In addition, reduced line losses typically will increase end-to-end energy efficiency as well, further reducing operating costs.

The logic behind 400 V DC power in the data centre is driven by the need for high availability, high efficiency and lower total costs. Since utility AC power ultimately must be converted to DC power for use by all IT equipment and because stored energy systems (batteries, flywheels, etc.) and renewable sources provide DC power, a typical DC power architecture requires fewer power conversions from grid to chip. Reducing these conversions not only saves energy, but also can increase critical power availability through simplified distribution and reduction of failure points in the power chain. Furthermore, DC power does not require phase balancing or considerations for harmonics, eliminating stranded power due to equipment de-ratings.

Additional DC power options for the data centre include those based on -48V DC, which is best suited for row-based solutions where loads are in close proximity to the UPS. This -48V topology is not comparable to a traditional, room-based AC UPS system, but now with the introduction of 400V DC power systems and components, for the first time the benefits of DC power are available in an enterprise-class power solution for the data centre. The degree to which companies can exploit savings from DC power varies from data centre to data centre. However, in theory at least, the advantages of using DC power in data centres seem obvious: servers use DC power, and the fewer conversion steps from AC power from the grid to servers, the greater the efficiency.

Transportation already using DC distribution

Transportation vehicles of many types (cars, ships, mass transit, locomotives, construction machinery and others) are integrating DC power for motor drive and other loads to increase efficiency and save fuel. For example, in the ship and locomotive industries, DC power is increasingly leveraged for propulsion and onboard loads. Similarly, as electric and hybrid vehicles such as cars and buses become more common, DC power is a logical choice for fast charging and use in vehicle systems. In these vehicles and others, DC will be used with current and 400V distribution technologies as they continue to move toward hybrid and all electric systems.

Renewable energy drives migration and benefits

Whether financially or civically motivated, building owners and operators today are increasingly using intelligent solutions that reduce energy consumption by leveraging renewable materials and energy sources. Using on-site, renewable power generation can reduce or even eliminate power draw from the grid. This is significant for 400 V DC because renewable sources generate DC power, which means using it for AC-powered applications within the building requires multiple conversions from DC to AC, reducing the efficiency of the renewable power generation. To avoid these extra conversions, architects and engineers are designing facilities with 400 V DC "microgrid" power distribution throughout or in selected areas of a building or campus. This solution increases system power efficiency, simplifies the electrical microgrid, and improves reliability while reducing operating costs.

To benefit from the emergence of 400V DC power distribution technology as a viable alternative to traditional power architectures Emerson Network Power has leveraged its expertise in the EMerge Alliance, an open industry association developing standards for the wider adoption of DC power distribution.

www.EmersonNetworkPower.com

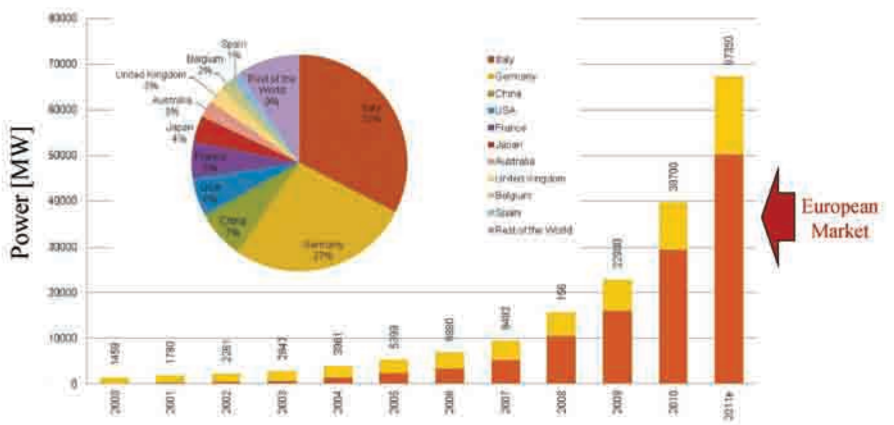
PCIM 2013 Call for Papers

The PCIM Europe 2013 (14. - 16.05.2013) Call for Papers is now open. The deadline for submitting abstracts is 15. October 2012. The event is the number one meeting place for all fields of power electronics and their applications. PCIM 2012 closed with 263 exhibitors, 6.874 visitors and 744 conference delegates - the highest numbers recorded so far. Besides new semiconductor technologies and devices such as Gallium Nitride (GaN) and Silicon Carbide (SiC) new assembly and interconnect technologies for power modules gained a lot of interest.

The topics to be covered in 2013 include recent developments in power semiconductors, passive components, thermal management products, energy storage, sensors and new materials as well as systems. This year's conference focuses on "Wind and Solar - Integration, Challenges and Solutions". Both are growing rapidly and thus provide huge opportunities for power electronics.

Proposals will be considered for conference lectures or posters. The accepted papers will be included in the official PCIM proceedings CD and the IET Inspec database. The conference language is English.

The conference directors will select the best papers for the nominations list from the submissions. The winner of the Best Paper Award (sponsored by Power Electronics Europe) will receive 1,000 Euro and the chance to participate at the PCIM Asia Conference in Shanghai, including flights and accommodation. For outstanding contributions from young authors not older than 35, three "Young Engineer Awards" of 1,000 Euros each will be granted. The prizes will be awarded at the PCIM Europe 2013 Conference Opening Ceremony.



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Thinner Ferrite Magnets Provide High-Performance Alternative to Expensive Neodymium Magnet Material

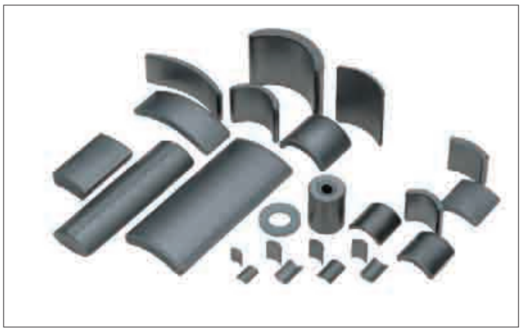
As manufacturers of renewable energy generation equipment such as wind turbines look for ways to increase their competitiveness, the development of a new, advanced magnet material promises to help reduce the cost of a key component of these electric power systems. Today, turbine generators and electric motors typically use neodymium magnets to produce a magnetic field surrounding a rotor, since to date neodymium has offered the best available combination of small size and low weight. This article shows how the new ferrite magnets from TDK Electronics can rival the performance of neodymium magnets while freeing turbine and motor manufacturers from the high cost and uncertain availability of neodymium magnets.

In recent years, rare-earth neodymium magnets have risen to the top of the market in terms of production value, but ferrite magnets continue to lead the field in terms of production volume. In fact, rising and volatile prices for neodymium materials coupled with uncertainty in a supply chain dominated by Chinese producers have led many end-product manufacturers to consider alternatives to neodymium magnets.

In contrast with neodymium, ferrite is an abundant and cheap raw material which is extracted in many parts of the world. Thus, improving ferrite magnet performance can be the key to addressing many issues facing society as a whole, including energy-saving requirements, environmental concerns, and resource conservation. Now TDK has developed a new production method using as its basis the FB12 material to create a mass production technique for FB13B/FB14H high-performance thin-shape anisotropic ferrite magnets that can be made as small as 1.0mm thick.

The world's first ferrite magnet - discovered by accident

The world's first ferrite magnet was discovered in 1930 by Dr Yogoro Kato and Dr Takeshi Takei, two professors at the Tokyo Institute of Technology. Dr Takei, a student of Dr Kato, was investigating how lowering zinc yield during the zinc refining process affected the physical properties of ferrite when he happened upon ferrite with high magnetism levels. One day in June 1930, Dr. Takei accidentally forgot to turn off his laboratory equipment before going home. The next day, the ferrite had taken on incredible magnetic properties, disrupting the magnetic



TDK thin ferrite magnets

balance (the magnetic field cooling effect). This marked the discovery of the world's first ferrite magnet.

Up to that point, magnets had almost always been composed of metal, but Dr Takei made the monumental discovery that like iron rust, ferrite's primary component was ferric oxide, making it a viable magnet material. His discovery was a ferrite magnet with the spinel-type crystal structure represented by the MOFe2O3 chemical formula, a magnet later commercialized as the 'OP magnet'. However, the product's low magnetic force limited its scope of application. Mass production of practical ferrite magnets began after the development of magnetoplumbite (MO6Fe2O3) ferrite magnets in the 1950s. Now, the main products in the field include Ba (barium) ferrite magnets and Sr (strontium) ferrite magnets.

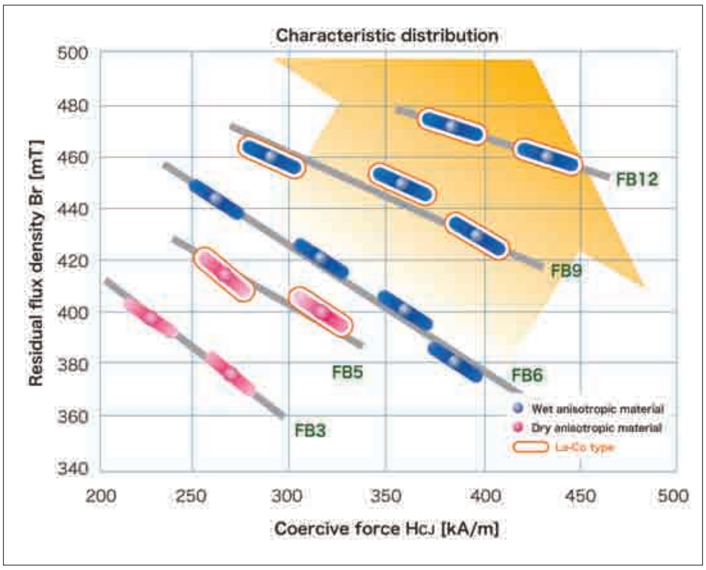
Due to the fact that ferrite magnets are ceramic (metal-oxide) magnets with oxygen atoms that do not affect magnetism, they will always demonstrate less magnetic force than metal magnets of the same volume. However, advances in material technology and sintering technology elevated the magnetic properties of ferrite magnets to rival those of alnico magnets (common alloy magnets) by the 1960s, paving the way for the use of ferrite magnets in speakers, inductors, motors and other applications.

FB series of high performance ferrite magnets

Sr ferrite magnets are often used in applications that require strong magnetic force. This is because Sr magnets offer the best residual flux density (Br) and coercive force (HCJ) of all ferrite magnets.

Sr ferrite is represented by the SrO6Fe2O3 chemical formula, but adding trace elements improves its properties. Although researchers made exhaustive searches for a wide array of different material compositions, leading many to believe that ferrite magnets had reached their potential, in 1997 TDK developed the La-Co (lanthanum-cobalt) type ferrite magnet (FB9 series), taking advantage of a new material composition to achieve remarkable improvements over conventional magnets' properties. Using this new composition, the FB9 series succeeded in improving maximum energy product by approximately 30 % over the traditional FB6 series.

The key to unlocking the maximum potential of the material lies in TDK's process technology, one of the company's core technologies. FB12, which entered the market in 2007, is another new material that surpasses the magnetic properties of the FB9 series by miniaturizing and homogenizing ferrite powder and establishing microstructure controls. FB12 has over 20 % greater maximum energy product than the FB9 series, makes dramatic improvements to demagnetization resistance in low temperature regions, and maintains stable power over a broad temperature range from -40°C to 150°C.

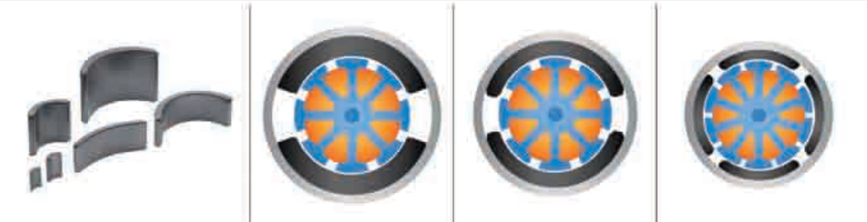


Ferrite characteristics improvement over generations

Contributing to motor miniaturization

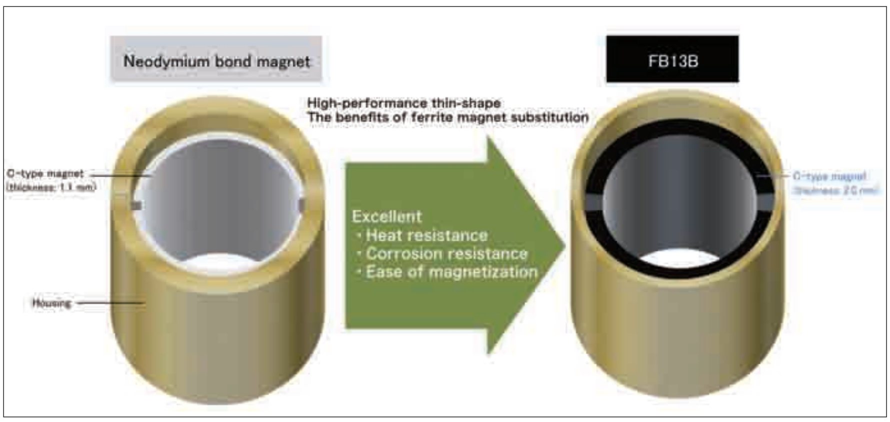
Since a ferrite magnet is a kind of ceramic, it used to be difficult to produce it in a thinner size than 3 mm through conventional production methods. However, motor and turbine manufacturers are under constant pressure to make their products smaller and lighter. This has led TDK to develop a new production method for ferrite magnets called 'NS1', which applies high density filling method with the FB12 material, enabling the production of thin-shape anisotropic

Using high-performance thin-shape anisotropic material (FB13B, FB14H) to reduce brushed motor size and weight



	FB6B	FB9B	FB13B
	2 poles	2 poles	4 poles
Motor diameter	Φ40	Φ37	Φ33.4
Motor volume	100%	86%	70%
Magnet wall thickness	5.0	3.5	1.9
Total magnet weight	65	47	26
Total magnet weight ratio	100%	72%	40%

Replacing a neodymium magnet with a high-performance thin-shape anisotropic ferrite magnet (FB13B, FB14H)



ferrite magnets with a thickness of 1.0 - 2.5 mm. The FB13B and FB14H ferrite magnets are products developed using the NS1 method. Motor miniaturization can be achieved by using high-performance thin-shape anisotropic hard ferrite material (FB13B, FB14H) in a multi-polarized motor design.

Achieving characteristics close to those of the neodymium bonded magnet type

Neodymium bonded magnets are highly prized in motor designs because they offer highly flexible configurations and thus can be adapted to different applications.

When used in harsh environments, however, neodymium bond magnets must be coated to improve their heat resistance and corrosion resistance. Thin-shape anisotropic ferrite magnets (FB13B, FB14H) take advantage of the properties of ferrite - excellent heat resistance and corrosion resistance - to eliminate the need for any additional coating. Magnetization can also be easily applied to the magnets after assembly as can be seen in the Table. Also a neodymium bond magnet can be replaced with a FB13B/FB14H magnet, the process involves adjusting the thickness of the housing/magnet wall, but does not require any changes to the rotor's diameter.

	Nd bond system		Conventional ferrite	NS1 method ferrite
	Anisotropy	Isotropy	FB6B	FB13B
Br(mT)	950	740	420	475
H_{cJ}(kA/m)	1100	717	300	380
H_{cJ} temperature coefficient (%/°C)	−0.50	−0.40	+0.30	+0.11
Heat resistance	△*1	△*1	◎	◎
Corrosion resistance	△*1	△*1	◎	◎
Thin-shape product configuration freedom	○	○	△	○
Ease of magnetization	△*2	△*2	◎	◎

◎ Excellent ○ Relatively superior △ Inferior
*1 Nd bond system: Requires a coating to improve reliability
*2 Nd bond system: Requires a powerful magnetic field (kA/m) to achieve full magnetization

Comparison of neodymium magnets, conventional ferrite magnets, and high-performance anisotropic material created via new methods

Special configuration enables further improvement in torque

Breaking through the limitations of conventional methods, the NS1 method allows a greater degree of ferrite magnet configuration freedom and ensures compatibility with special wall shapes.

The method can, for example, make it possible to use a C-type motor magnet in a wide-arc configuration that wraps around the rotor without having to modify the basic design of the motor or turbine. This maximizes the use of empty space in the motor case, and, by taking full advantage of the FB13B/FB14H's potential, achieves motor performance that rivals that of neodymium magnets. As shown in the graph below, the new material provides a significant boost in starting torque, but combining it with a wide-arc shape produces an even greater increase in torque, comparing favorably with the performance of neodymium magnets. By optimizing particle orientation and thus improving magnetization orientation, the magnet achieves the best ferrite magnet properties.

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Zero-Voltage Switching in Point of Load Devices

Vicor introduced a new Picor PI33XX Cool-Power® ZVS buck regulator series that integrates a Zero-Voltage Switching (ZVS) topology, providing conversion efficiency up to 98 % peak. PI33XX buck regulators can convert input voltages ranging from 8 V to 36 V to output voltages from 1 V to 16 V and output current up to 10 A for power delivery up to 120 W in a 10 mm x 14 mm x 2.56 mm LGA System in Package (SiP). Power can be further increased by interleaving up to six PI33XX buck regulators using single wire current sharing without the need of any additional components.

The use of a ZVS topology enables high-frequency operation that maximizes efficiency by minimizing the significant switching losses associated with conventional buck regulators that use hard-switching topologies. The high switching frequency of the PI33XX series also reduces the size of the external filtering components, improving power density, while enabling fast dynamic response to line and load transients. The PI33XX series sustains high switching frequency all the way up to the rated input voltage without sacrificing efficiency and, with its 20 ns minimum on-time, supports large step down conversions up to 36 V input.

PI33XX series buck regulators require only an external inductor and minimal ceramic capacitors for input and output filtering to form a complete regulator (see demo board). No frequency compensation, parametric settings or incremental external components are required. A wide operating temperature range of -40°C to 125°C allows for use in almost any environment.

For designers challenged by complex distribution power schemes, Picor PI33XX offer an optional I²C™ extended fault telemetry capability allowing for six distinct types of fault reporting. Additional device-programmable I²C™ features include margining, enable pin logic polarity, and phase delay. Device programming is performed via the Cool-Power Development Tool.

Losses and topology

Regulator MOSFET switching losses are the losses attributed primarily to the high-side MOSFET during turn-on, Miller gate charge, and body diode conduction losses. High-side MOSFET turn-on is when the power MOSFET has the highest voltage and current switching and thus the highest power loss attributed to it. These losses further magnify themselves within a design as higher input voltages are converted or regulated.

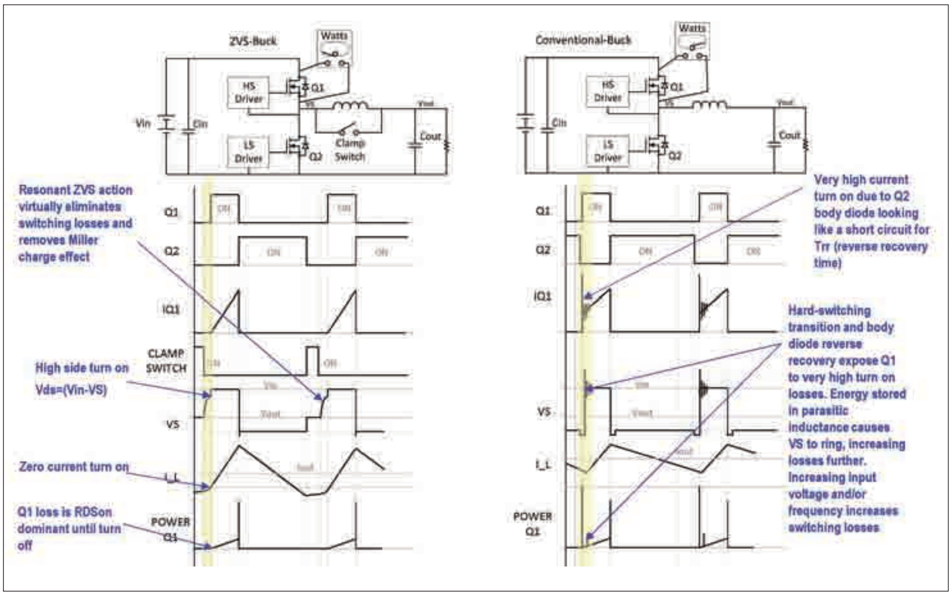
The higher the input voltage, the higher the voltage across the primary MOSFET, and the higher the losses at turn-on. These switching losses prevent dramatic improvements in overall power system solutions. For example, within industrial process control systems a desired regulation of 24 V to 3.3 V typically is achieved by first regulating from 24 V to 12 V followed by a second regulator converting 12 V to 3.3 V. In contrast, a single regulation stage can regulate 24 V to 3.3 V with an efficiency level at or higher than the two stages and thus improve cost, board space, and reliability.

Switching losses also limit the switching frequency of the regulator. The higher the switching frequency the more time the MOSFET switches and the more losses occur. The inability to switch at a high frequency limits the use of smaller passive components, penalizing the density of the regulator. The PI33XX with its ZVS topology allows for operation at a higher frequency and at higher input voltages without sacrificing efficiency. The ZVS topology is a soft switching topology in contrast to a hard switching topology deployed in conventional regulators.

The PI33XX devices operate up to and over 1.5 MHz, which is typically 2x to 3x that of conventional high density regulators. Higher frequency operation not only reduces the size of passive components but also reduces the burden en external filtering components and allows for fast dynamic response to line and load transients.

ZVS switching topology

A direct comparison can be made between a conventional buck topology and the PI33XX with ZVS buck topology. First, with the typical approach at the start of a complete switching cycle, the high-side MOSFET is commanded to turn on. Just prior



LEFT: Comparison between ZVS switching technology (left) and conventional buck topology

to turn on, there is inductor current flowing in the output inductor and the synchronous MOSFET. In order to avoid cross conduction of the MOSFETs, there is a delicate balance between turning off the synchronous MOSFET and turning on the high-side MOSFET.

The result of this design trade-off is often body diode conduction. Conduction of the body diode requires that the stored charge accumulated while it is conducting at some peak current be swept away before the diode can support any reverse blocking voltage. As such, the drain-to-source voltage of the MOSFET is practically clamped at the input voltage (strongly dependent on parasitic inductance) while very high current flows through the body diode and through the high-side MOSFET until a depletion region forms and the body diode starts to support reverse voltage.

Until that time, the instantaneous power dissipated in the high-side MOSFET is quite high. Part of the losses is incurred due to the reverse recovery current and the rest are due to discharging the MOSFET output capacitance. In addition, there are also reverse recovery losses in the low-side synchronous MOSFET body diode. These losses increase as the switching frequency or input voltage increase. The power curve for Q1 in the switching waveforms for the conventional buck regulator shows the effect of turn-on. The peak instantaneous power at turn-on can be a dominant loss contributor for the high-side MOSFET in high-switching frequency applications. There have been attempts to remedy the switching loss associated with body diode conduction ranging from switching faster to adaptive gate drivers even to MOSFET improvement through various improved Figure of Merit (FOM) devices.

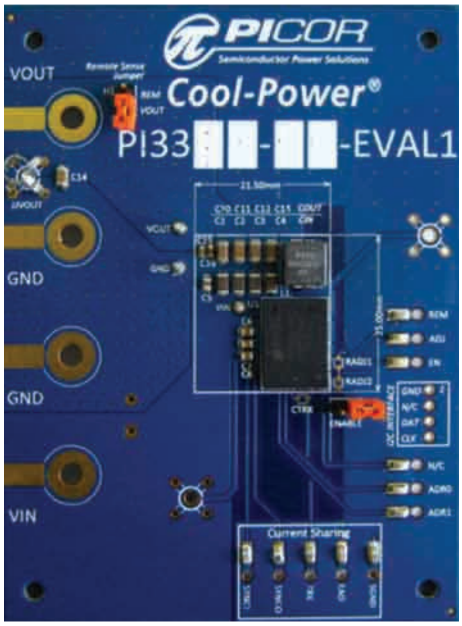
The PI33XX starts its switching cycle with nearly zero current flowing in the output inductor. The voltage across Q1 is nearly zero as a result of ZVS action. The inductor current ramps up from zero to a peak value followed by Q1 turning off. The inductor current is commutated to the Q2 body diode for under 10 ns and Q2 turns on. The stored energy in the inductor is delivered to the load. The turn-off of Q2 is delayed until the inductor current is driven negative by current from the output capacitor, thus storing energy in the inductor.

Next, the clamp switch turns on, allowing the stored energy to circulate until Q1 needs to turn on again and clamping V_s to V_{out}. To facilitate ZVS, the clamp switch opens. The stored energy then resonates with the output capacitance of Q1 and Q2. Resonant current flows into Q1 from source to drain and into Q2 from drain to source. This resonant action discharges Q1 output capacitance and charges Q2 output capacitance. Then Q1 can turn in a lossless manner.

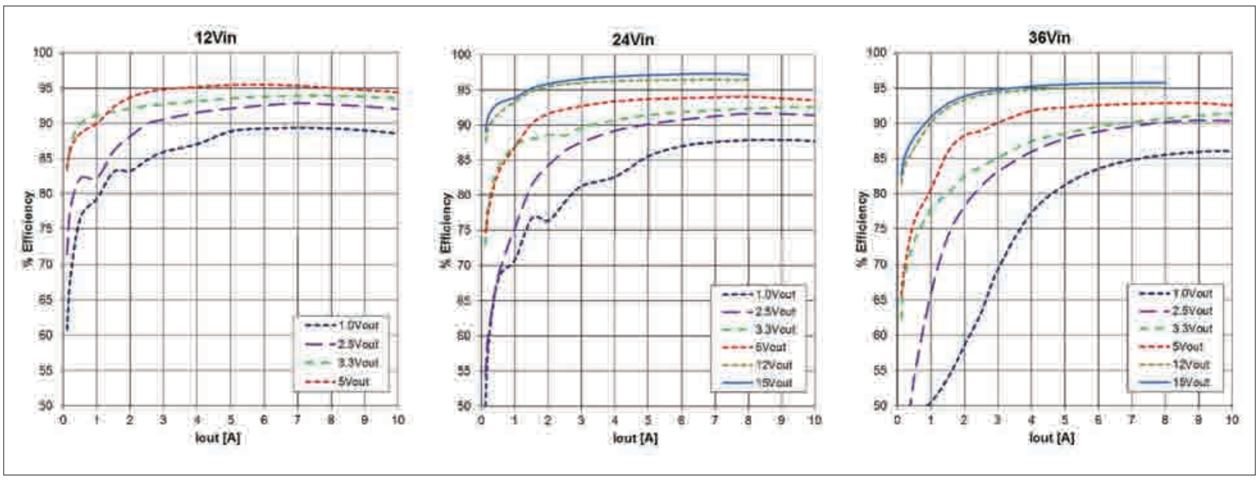
The PI33XX addresses the high turn-on losses of the conventional regulator by eliminating high current body diode conduction prior to turn on of the high side MOSFET, bringing the drain/source voltage of the high-side MOSFET to nearly zero and produces no high current spikes or damaging ringing. The ZVS action applied to Q1 removes the Miller effect at turn-on of Q1, allowing the use of a smaller driver and lower gate drive at turn-on.

Regulation from a higher voltage, at a higher efficiency, and in a smaller form factor is realizable with implementation of an improved switching topology. By utilizing the ZVS topology within the PI33XX, a buck regulator is offered that demonstrates high performance regulation up to 36 V input voltage exceeding the performance found in conventional hard switching, high density regulators.

http://www2.vicorpower.com/zvs_buck2



Picor ZVS buck regulator demo board



RIGHT: Efficiency curves for different input voltages at light and full load

Past, Present and Future of HPT-IGCT

The integrated gate-commutated thyristor (HPT-IGCT) is a state-of-the-art bipolar turn-off device for high power applications. New devices employing this technology have been released during the past few years and in this article we take a look at the newest member in ABB's product portfolio - the 5.5 kV asymmetric HPT-IGCT. The development of the HPT-IGCT continues, however, and in this article we will also take a look at one interesting device in the pipeline. **Tobias Wikström and Björn Backlund, ABB Switzerland Ltd, Semiconductors**

The IGCT was introduced about 15 years ago and has established itself as a preferred technology for handling very high power. The applications range from industrial drives and track-side supplies to power quality and high-current breakers. The IGCT is available as reverse conducting devices with an integrated free-wheeling diode and as asymmetric devices. The first devices, as well as most devices made today, use a flat p-base but a new family of devices, referred to as HPT-IGCT, using a corrugated p-base, has been developed recently.

IGCT basics

The first device in the HPT-IGCT family was the asymmetric 4500 V device 5SHY 55L4500 released in 2009. In 2010, 5SHY 42L6500 followed, an asymmetric 6500 V device and in 2012, yet another asymmetric device 5SHY 50L5500 rated 5500 V was released. All these devices use the same package (see Figure 1) with a copper pole piece diameter of 85 mm.

The main strengths of the device lie in its thyristor-like on-state with maximal possibilities for engineering the on-state plasma distribution for optimal trade-off between on-state and turn-off losses, its rugged mechanical design and good thermal coupling to the cooler. Two disadvantages of the IGCT compared to the IGBT, the only competitor device in the power range of the IGCT, is the relatively large effort needed to control the device -

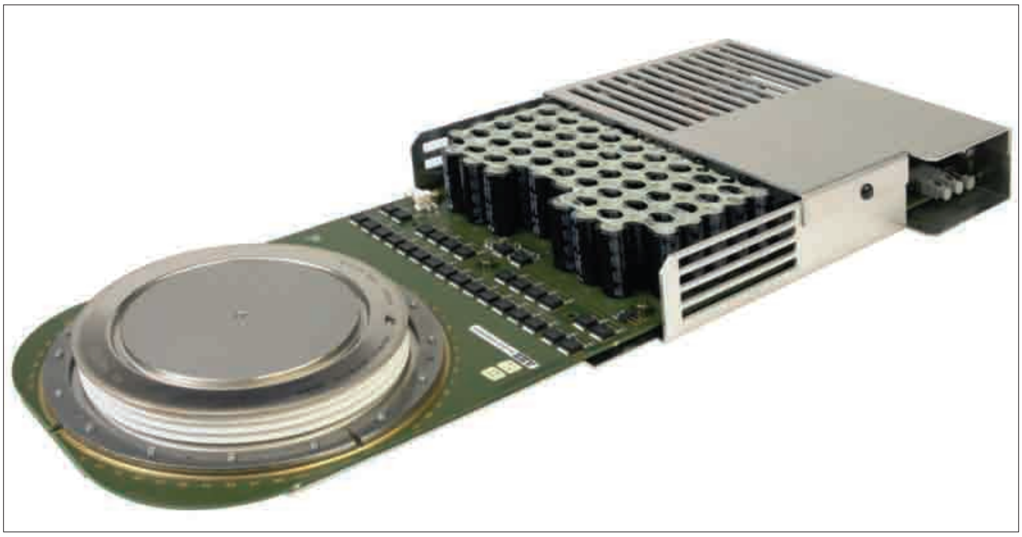


Figure 1: The HPT-IGCT, consisting of the silicon switch in a hermetic ceramic housing on the left, closely coupled to the gate driving circuit on the right

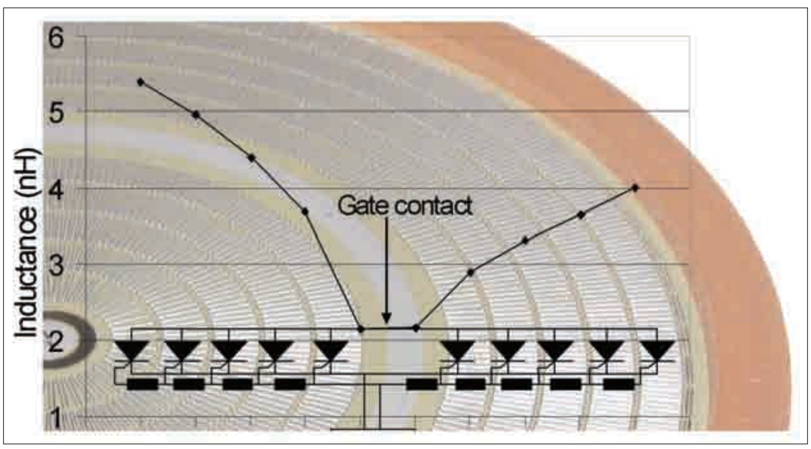


Figure 2: Inductive situation (simulated values) of the individual segment rings on an IGCT wafer showing how inductances can be distributed over the wafer. The rings far away from the gate contact are more heavily loaded by inductance than the rings in the vicinity. Hence, the gate signal will propagate at some finite speed and disfavor the gate-remote regions

tens of Watts for a 3.6kA device - as well as the inability to control the anode voltage during turn-on. The former is due to the fact that it is a current-controlled device. The latter is due to it being a thyristor and, as such, it is either off or on and the transition between those states is only stable in theory. Hence, implementing it in most common inverter topologies means protecting the antiparallel diode at turn-on. Nevertheless, thanks to its low losses and efficient cooling, it is and continues to be the preferred choice for many manufacturers of very large power inverters. Other requirements for applications such as breakers for large currents can only be met using the low on-state of the IGCT.

The maximum controllable current (MCC) of the IGCT does not scale linearly with device area. The reason is the inductive (and resistive) coupling to areas remotely placed from the gate contact. The area scales with the square of the diameter, whereas the MCC merely scales linearly, using the same technology. A graphical summary of this situation is presented in Figure 2. The technology can be improved by decreasing the total inductance in the package (i.e. the minimum, 2 nH, in Figure 2.), improving the local ruggedness to facilitate more current redistribution and increasing the driving gate voltage. The high-power technology was built using the first two.

High power design elements

The enablers for very high current turn-off are a combination of improving the local ruggedness of the silicon device itself by employing p-base corrugation, and increasing the gate's reach by minimizing the impedance, mostly in the gate driver circuit itself.

Finding the optimum for the p-base corrugation used for improving local ruggedness means trading off many parameters, such as blocking capability, thermal budget, process limitations and ruggedness. In general, the higher the device voltage, the deeper and more highly doped the p-base has to be made.

The improvements to the gate unit include improved lifetime of the capacitors used, using a 6- instead of 4-layered PCB substrate, increasing the parallel connection of the turn-off channel by increasing the number of MOSFET switches and capacitors, as well as optimizing the layout of the components on the gate unit. With careful selection of the used components, it is also possible to reduce the losses in the gate unit.

A further improvement to the gate unit is the possibility to equip the IGCT with an anode-voltage sensor feature to improve the applicability of the device, facilitating early error detection.

The IGCT technology can utilize all commonly used lifetime adjustment techniques. Using electron irradiation, proton irradiation, or both, one can tailor the electron-hole plasma distribution to the best shape and tune the trade-off between static and dynamic losses to the best fit for the application. Thanks to the vast surplus of charge in the on-state, lifetime attenuating techniques can be utilized within a broad range. The 5.5kV device was designed using electrons and proton irradiation from the anode side, which significantly reduces the overall losses.

5500 V device capabilities

Dynamic electrical testing was carried out in a circuit displayed in Figure 3. The clamp circuit used to protect the freewheeling diode is close to the application and facilitates rapid and reliable testing, as opposed to measuring replicas of inverters.

Safe operating area (SOA) and losses

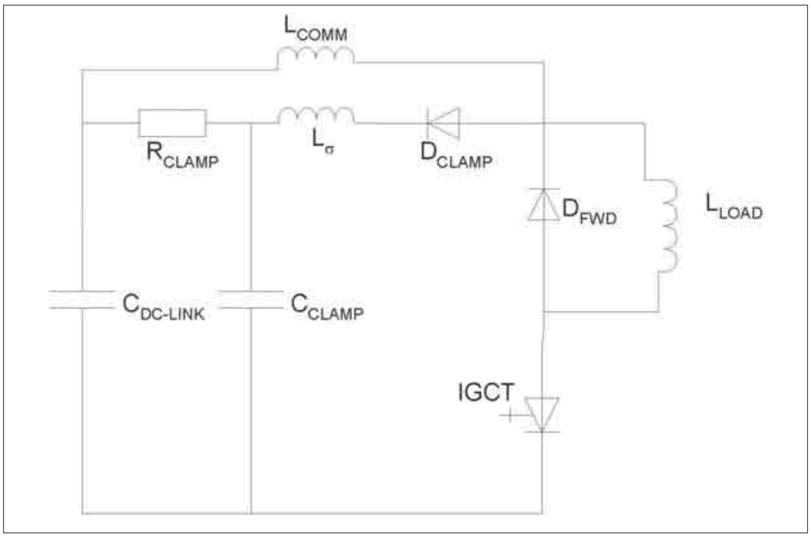


Figure 3: Circuit used in dynamic testing of the IGCTs (parameters: C_{CLAMP} = 8μF, L_{σ} = 300nH, R_{CLAMP} = 0.6 Ω, L_{COMM} = 6 μH)

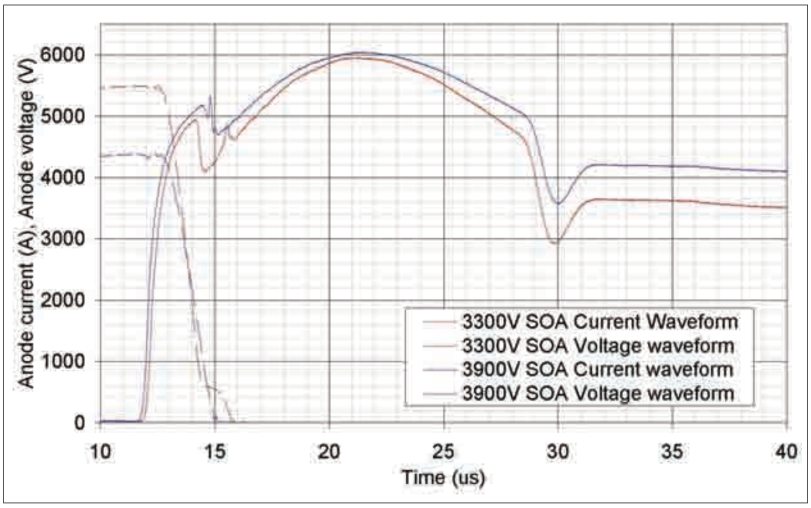


Figure 4: Current handling capability of the 5.5 kV HPT IGCT. At 3.3 kV DC-link voltage, more than 5.5 kV can be controlled (device testing stopped without destruction). At 3.9 kV, the tests stopped at around 4.4 kA, as the over-voltages involved exceed 6 kV, and hence the specified device capability by more than 500 V

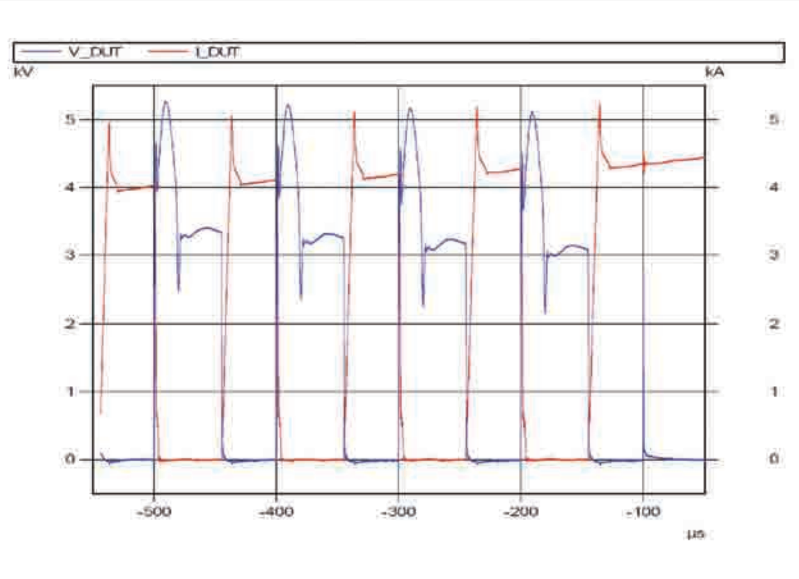


Figure 5: **Waveforms from the 10 kHz burst measurement. This example failed at the fifth pulse, at 4.4 kA**

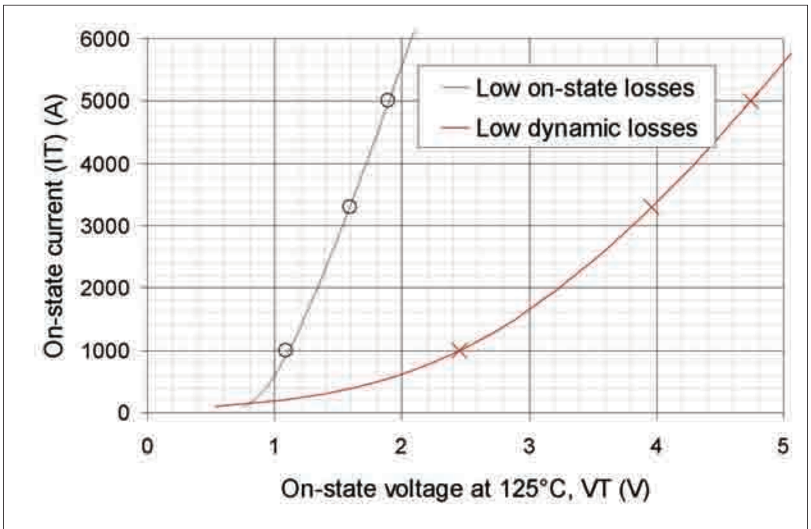


Figure 6: **Flexibility of on-state voltage tailoring in IGCT technology**

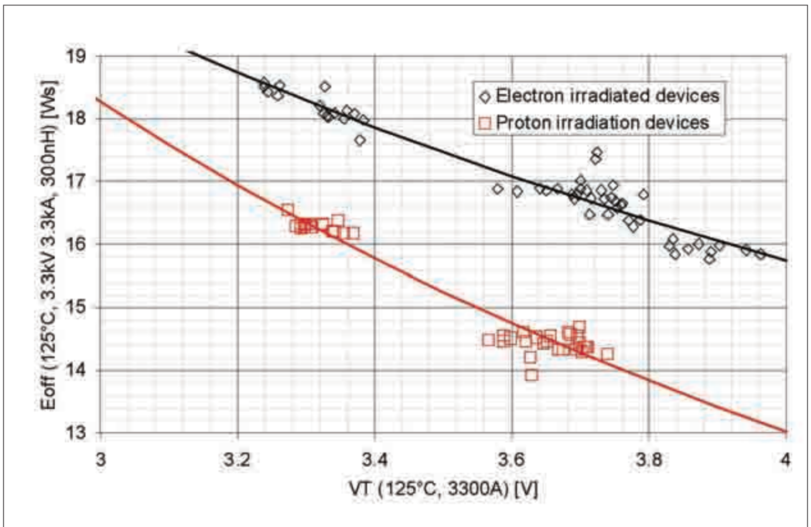


Figure 7: **Loss trade-off for the 5.5 kA IGCT switching 3.3 kA at 3.3 kV with a T_j of 125°C. Additional circuit parameters are listed in the caption of Figure 3**

were evaluated in the dynamic circuit, both at single pulse as well as at burst frequency (10 kHz) for special applications. Samples of waveforms from SOA measurements are presented in Figure 4. Noteworthy is that SOA testing was interrupted when the maximal voltage reached 6 kV during testing. Beyond 6 kV, one would risk a blocking failure in the clamp-circuit discharge following the switching transient, which would not add any information, as this condition would be far beyond specified capabilities.

The burst capability of the device was tested - five pulses at 10 kHz. As the temperature coefficient of the MCC is negative, the failures always occur at the fifth pulse. Due to limitations in the test circuit, it is not possible to test at constant current and voltage. Instead, the current increases and the voltage decreases as the pulse train progresses. In this mode, the IGCT withstands a current of around 4 kA at a voltage between 3 - 3.3 kV. Of course, when switching at this speed, the process is more or less adiabatic which means that the wafer temperature is significantly higher than the allowed 125°C after pulse number 5, if the starting temperature is 112°C. A typical pulse pattern from the burst tests is presented in Figure 5.

To optimize the losses in the 5.5 kV HPT-IGCT, both proton and electron irradiation are used. Figure 6 shows the high flexibility that is possible using different irradiation doses.

Using these lifetime tailoring techniques, a profound influence can be seen on the loss trade-off (Figure 7).

Before a newly developed device is released, it must undergo extended reliability testing. The performance of the device in the presence of cosmic rays is especially of interest with new Silicon specifications and Thyristor designs. Testing was done in a proton beam, for which a sound correlation to actual cosmic rays has been established, with the obvious advantage that the testing is done in a matter of hours instead of years (Figure 8).

In the pipeline - the 150 mm IGCT

The quest for ever higher power ratings makes the option of expanding into larger Silicon diameters viable. Since bipolar devices using 150 mm Silicon since have been in production for some time now, the means are available. In addition, the improved scalability of the HPT technology is an important enabler for taking such a step. The first 150 mm reverse conducting 4.5 kV HPT-IGCT prototypes have recently been

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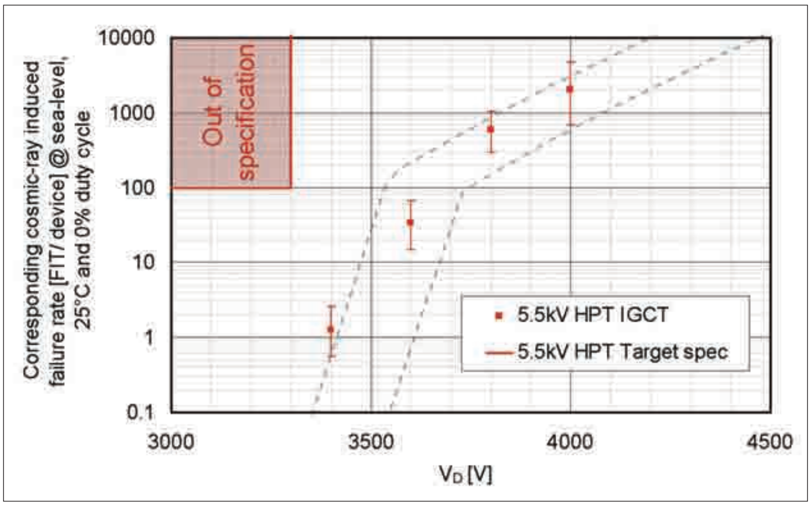


Figure 8: Corresponding failure rates due to cosmic rays measured using biased devices in a high-energy proton beam. The specification can be used arbitrarily; however, the 100 FIT level has become the accepted standard where failures due to cosmic rays will become a significant factor in the field

Figure 9: Prototype of 150mm 4.5 kV RC-IGCT

manufactured and a sample is shown in Figure 9.

This device is expected to have a rated SOA capability in excess of 7 kA against a DC voltage of 2.8 kV at similar conditions as presented in Figure 3. With this device, it will be possible to make 3-level inverters up to about 20 MW without the need for series or parallel connection of power semiconductor devices. With the free-wheeling diode already integrated in the IGCT package, assembly designs can be improved. Critical to the performance is the size and uniformity of the inductance for the segment rings. However, by employing the design elements from the existing HPT-IGCTs, the wafer has the targeted performance in respect to uniformity and absolute inductance.

Today, the added challenges lie in the design of the housing package and the gate unit. On the wafer design front, the main challenge is to provide a soft integrated diode performance under different operational conditions including the best IGCT versus diode area ratio selection. Hence, there is still some work to be done before the device is ready, since extensive electrical and environmental qualifications also lie ahead before the first devices can leave the factory.

Comparison of 1200V SiC Power Switching Devices

Silicon Carbide (SiC) power semiconductors being actually commercialized and are promising devices for the future. To outline their characteristics the switching and conducting performance of two types of SiC normally-on JFETs, a SiC normally-off JFET two types of SiC MOSFETs and a SiC BJT have been analyzed by means of measurements at exactly the same boundary conditions and compared to each other. Beside of the switching and conducting behaviors the requirements for driving these devices have been investigated.

W.-Toke Franke, Danfoss Solar Inverters, Denmark

Since 2002 the first silicon carbide diodes (SiC) are available on the market. Already at that time the diodes outperform their Silicon counterparts regarding to switching characteristics and conducting behavior. Since then a significant development process in the field of wide bandgap semiconductors could be observed. Today a number of SiC based switching power semiconductors in the voltage range from 600 V to 1700 V and maximum currents up to 50 A are introduced to the market or are about to be launched.

Typical devices in the voltage range of 1200 V are EMJFETs, DMJFETs, MOSFETs and BJTs [1, 2, 3]. These power semiconductors have been investigated concerning their conducting and switching characteristics at exactly the same conditions. Their current capability is between 12 A and 25 A. Furthermore the requirements for driving these devices are discussed as they differ from the well-known Silicon power devices [4].

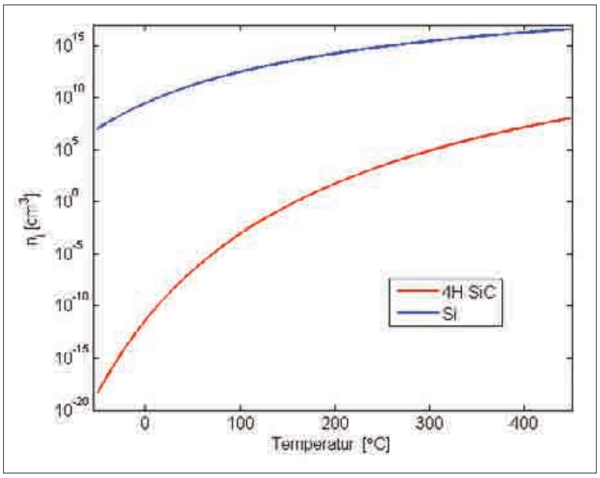


Figure 1: Intrinsic charge carrier density vs. temperature

Properties of Silicon Carbide

The great interest for silicon carbide power semiconductors is based on the physical features of the 4H-SIC polytype, which has some advantages over Silicon in the relevant criteria for power semiconductors. The most important parameter is the bandgap of 4H-SiC that is about three times as large as for Si. Table 1 shows that the charge carrier density of SiC is at room temperature 19 orders of magnitude smaller than for Silicon [5, 6]. In Figure 1 the intrinsic charge carrier density versus temperature is shown. It is clearly visible that the charge carrier density of SiC is significantly below typical doping density ($1{\cdot}10^{15}$ cm^{-3}) even at high temperatures. However, with Silicon this number is already reached at about 250°C. The impact of this for semiconductors is a significantly lower generation of charge carriers within the space-charge region and thus leads to lower leakage currents in off-state.

Theoretically, SiC power semiconductors can be operated at very high temperatures due to this feature. The limiting factors are the packaging and connection facilities to realize the electrical and thermal interfaces to the outside. Besides that the large band gap enables Schottky barriers with high potential barrier so that high voltages with low leakage currents could be blocked.

	Si	4H-SiC
Band gap E_G [eV]	1,12	3,26
Critical el. Field strength E_{crit} [kV/cm]	300	2800
Intrinsic charge carrier density n_i [1/cm^3]	$1{,}4{\cdot}10^{10}$	$5{\cdot}10^{-9}$
Thermal conductivity λ_{th} [W/cm K]	1,5	3,9
Saturated drift velocity of electrons $v_{n,sat}$ [cm/s]	$1{\cdot}10^{7}$	$2{\cdot}10^{7}$

Table 1: Physical properties of Si and SiC

SiC bipolar transistor

The Silicon bipolar junction transistor (BJT) is no longer relevant in power electronics, although its production is simple and inexpensive. However, the effort for driving the BJT is high and therefore cost-intensive, since a high base current is required. On the other hand is the SiC BJT with 1200 V blocking voltage, a

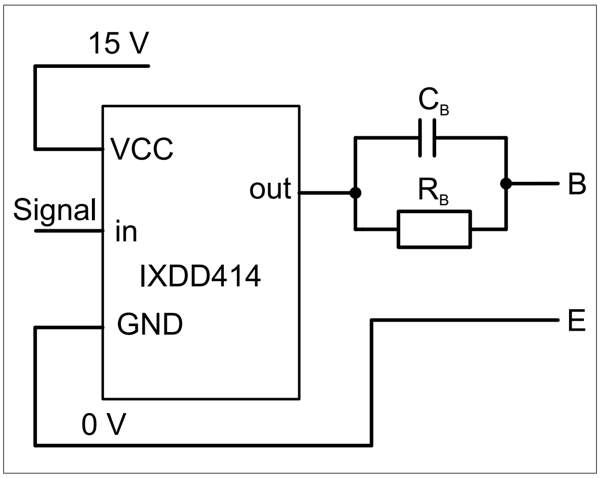


Figure 2: **Driver for bipolar transistor**

temperature range of up to 200°C and 12 A or 40 A collector current. The required base current is low compared to Si transistors. The current gain β is defined by the ratio between collector and base current ($\beta = i_C/i_B$) and can be traced back to the physical characteristics of the transistor.

A gain higher than 1 can be obtained when the doping concentration of the emitter is significantly above the doping concentration of the base and the base width is in the range of the diffusion length.

The use of SiC as a substrate for the bipolar transistor has a number of advantages compared with the Silicon-based transistors - significantly shorter switching times and despite the larger band gap lower saturation voltages and higher current gains could be realized.

In order to keep the bipolar transistor in the conducting state the driver has to provide a base current. Because of the voltage drop across the base-emitter pn-junction, power is consumed throughout the on-state. A possible driver circuit is shown in Figure 2. The base current is limited by the resistor RB and for fast switching a capacitor CB is connected in parallel to R_B. C_B acts like a short circuit during switching, so that the base region could be flooded and cleared out fast with charge carrier respectively for turning on and off.

SiC depletion mode MOSFET

Characteristic for the depletion mode JFET (DM-JFET, Normally-On JFET) is that it is turned on at a gate voltage of 0 V [7, 8]. This characteristic is contrary to all semiconductors established on the market [9] and leads to considerable efforts for the driver: If the JFET is directly driven, it must be ensured that the driver is also supplied with power in case of a failure on the AC or DC side, to hold the JFET in blocking state. If the JFET is directly driven a gate voltage of -15 V is required to block the device and 0 V to hold the device in conducting state. For further reduction of the on-resistance a positive voltage of up to 2 V can be applied.

An alternative to drive the JFET directly is to operate it in a cascode (see Figure 3).

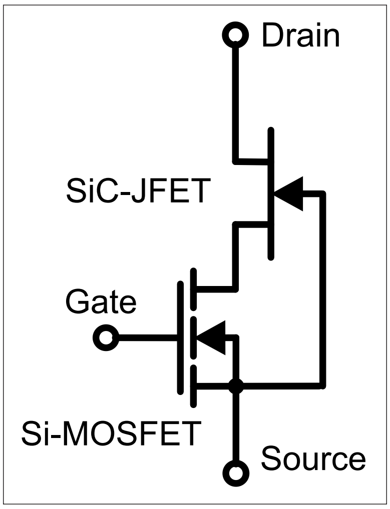


Figure 3: **Cascode consisting of a SiC JFET and a Si MOSFET**

Therefore a Si-MOSFET with low blocking capability (e.g. 30 V) and a very low R_{DSon} the gate of the JFET is connected to the source terminal of the MOSFET and its gate is driven by a conventional MOSFET driver. When the MOSFET is blocking the potential of the source terminal of the JFET is lifted. Since the gate of the JFET is on the source potential of the MOSFET, it results in a negative gate-source voltage of the JFET and it blocks as well. The voltage drop across the MOSFET is limited to the gate voltage that is required to block the JFET. The cascode is turned on by turning on the MOSFET. In this case the voltage drop across the MOSFET is almost 0 V and hence the gate-source voltage of the JFET is also 0 V, the JFET is conducting.

The advantage of the cascade is that the JFET can be driven as a conventional MOSFET.

However this topology also has two disadvantages: Firstly, a positive gate-source voltage cannot be applied to the JFET and therefore the optimum conducting performance cannot be achieved. Secondly, the full dynamic potential cannot be utilized, because the switching performance is mainly given by the Si-MOSFET.

However, the leading manufacturers of these devices Semisouth and Infineon introduce driver concepts in their application notes that combine the advantages of the cascode with the direct driven approach. The effort for the driver thus increases considerably.

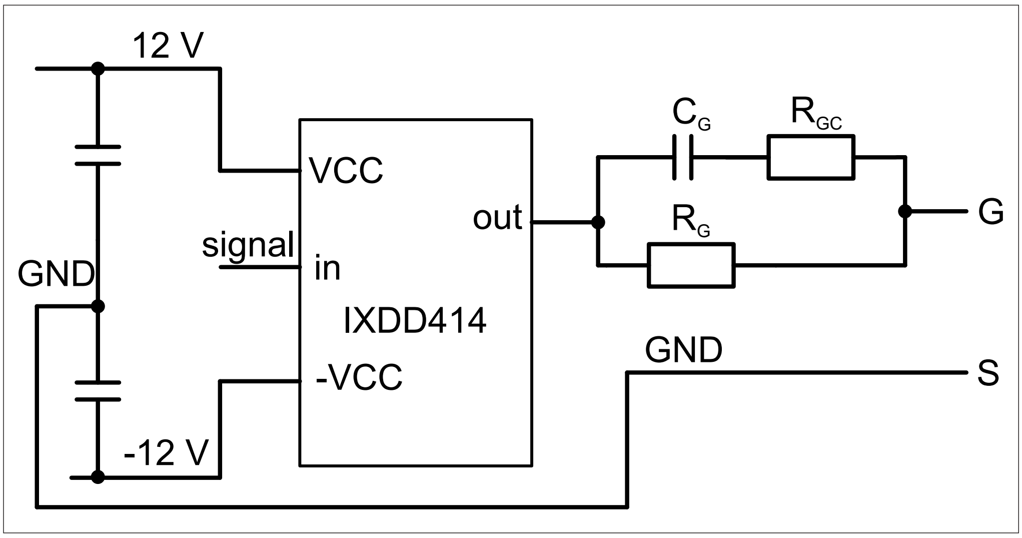
SiC enhancement mode MOSFET

The enhancement mode JFET (EM-JFET, Normally-Off JFET) differs from the DM-JFET by blocking at a gate voltage of 0 V [10]. Initially it resembles the performance of the established power semiconductors. However, the driving is not comparable. Due to the JFET structure it starts conducting at a gate-source voltage of 1,5 V. At about 3 V it is fully turned on; however the pn-junction between gate and source starts conducting at about 2 V and lead to a gate current that has to be provided by the driver. This gate current is considerably lower than the base current of bipolar transistors, but due to the voltage drop it causes power loss. To turn on the EMJFET optimally, a voltage pulse of 12 to 15 V must be supplied to the gate for about 200 ns. This voltage pulse can be realized as described for the bipolar transistor by a parallel connected capacitance to the gate resistor (Figure 4).

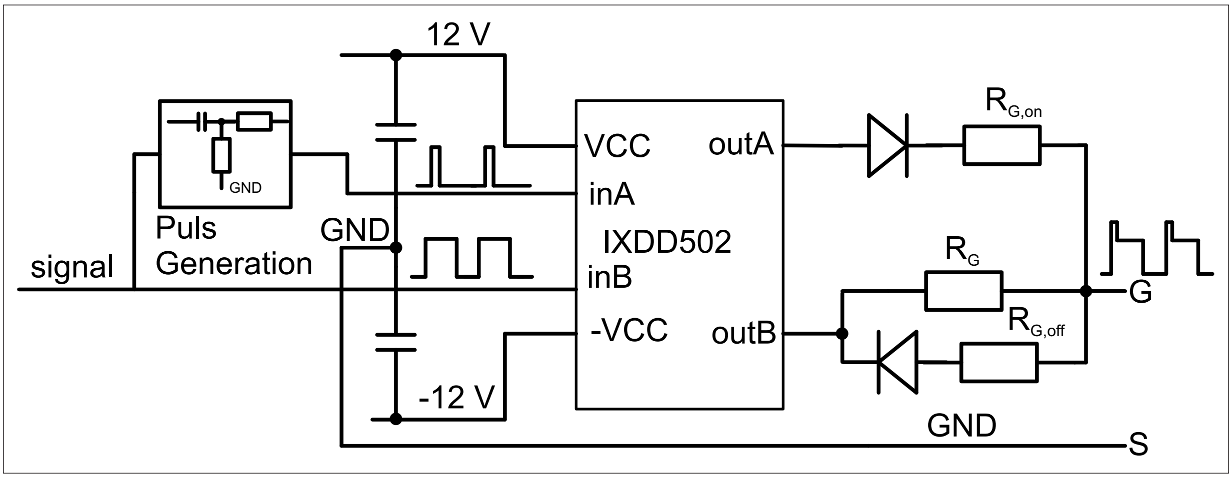
The gate resistor must be dimensioned to limit the maximum gate current during on state and to dissipate the power losses. A more efficient method that also allows any modulation index is a 2-stage driver. Here the voltage pulse is provided by an additional driver stage [11] as depicted in Figure 5.

SiC MOSFET

The SiC MOSFET differs from Si MOSFET mainly due to its higher blocking voltage. In principle blocking voltages up to several kV can be achieved with SiC MOSFET due to the high critical electric field strength at even superior dynamic performance. The gate driver requirements of the actual generation differ only slightly from the Si MOSFET. The MOSFET is turned off at 0 V, however it is recommended to bias the gate in blocking state in order to avoid unintentional turn on by electromagnetic coupling. The MOSFET is fully turned on at



RIGHT Figure 4: EMJFET driver



BELOW Figure 5: EMJFET Driver with additional voltage pulse for optimized performance

20 V. As with all other SiC power semiconductors, the complete dynamic potential can only be exploited if the driver is correspondingly fast and the electrical connection is extremely low inductive, to avoid over-voltages due to the extremely short rise and fall times of current and voltage.

Comparison of SiC power semiconductors

While IGBTs are dominating the 1200 V voltage range of Silicon based switches today, older switching device structures as BJT and JFETs are relevant for SiC again. Since these structures are relatively simple to manufacture they are applicable for SiC, as the experiences in the production process are still minor in comparison to Silicon. To be able to select the right component for a specific application its properties must be well known. In general it is a fact that components of the same type but from different manufacturers cannot just be replaced since they differ in the physical internal structure and thus also differ regarding driving, switching and conducting behavior.

Driving a SiC MOSFET is similar to driving a Si IGBT. The handling of the bipolar transistor is safe due to its base current, however it requires a non-negligible driving power which has on the one hand to be provided by the driver and on the other hand leads to additional losses in power semiconductors.

The EMJFET can be driven also rather safely, but the driving losses are much smaller compared to the BJT. However, the complexity of the driver increases due to the different gate voltage levels (peak switch-on voltage, conducting voltage, and negative reverse voltage). For the DMJFET it can be chosen between driving the JFET directly or in a cascode that leads basically to a Si MOSFET driver. They both require complex driver structures if maximum performance of the JFET should be utilized and at the same time safe operation in all circumstances are applied.

The DC-current capacities of the analyzed power semiconductors at room temperature are stated in Table 2 according to the datasheets in order to evaluate the measurement results. Except for the bipolar transistor all power semiconductors are in the same power range.

The conducting behavior is illustrated in Figure 6. The first three graphs show the U-I characteristic of the power semiconductors at 25°C, 80°C and 150°C junction temperature. Since the Cree MOSFET is only specified up to 125°C, the 150°C curve was extrapolated for better comparability. It can be seen that the MOSFET has low temperature dependence and thus also at typical operating temperatures it can carry almost the full rated current. For the JFETs and the bipolar transistor a halving of the current by increasing the temperature is observed. Regarding the bipolar transistor it is remarkable that in contrast to Silicon BJT and IGBT no collector-emitter saturation voltage is visible, but shows a resistive V-I-characteristic as known from unipolar components.

The other two curves show the reverse conducting performance while turned on. Since the BJT cannot be operated with negative current, it was not considered. The temperature dependence is similar to that in forward conducting mode. Noticeable is the current waveform of the MOSFET from Rohm which has V-I-characteristic similar to a bipolar component. This could be explained by the existence of an antiparallel diode.

The total switching losses are shown at

Manu-facturer	Com-ponent	Current rating @ 25 C	$R_{DS,on}$	Gate voltage off-state	Gate voltage on-state
Cree	MOSFET	33 A	80 mΩ	0 V (-5V)*	20 V
Fairchild	BJT	12 A	-	0 A	300 mA
Infineon	On-JFET	31 A	100 mΩ	-16 V	0V (2V)*
Rohm	MOSFET	26 A	90 mΩ	0 V (-6 V)*	18 V
Semisouth	On-JFET	27 A	85 mΩ	-15 V	0V (2V)*
Semisouth	Off-JFET	27 A	100 mΩ	0V (-15 V)*	3V (15V)**

All are able to block 1200 V

*recommended during operation

**for max 200 ns for faster turn on

Table 2: Reviewed devices in accordance with the datasheets

650 V and different currents at 25 and 150°C in Figure 7. It was decided not to differentiate between turn-on and turn-off losses since due to the very short switching times the losses could be moved between turn-on and off depending on the parasitic inductance and capacities in the commutation path. For all components the same SiC Schottky barrier diode was used. For the Cree MOSFET the losses at 150°C were extrapolated. All power semiconductors have been investigated with an identical test setup (double pulse experiment [4]). The drivers were as far as possible designed identical and they have been configured to allow the fastest switching times without instable ringing so that the lowest switching losses could be achieved.

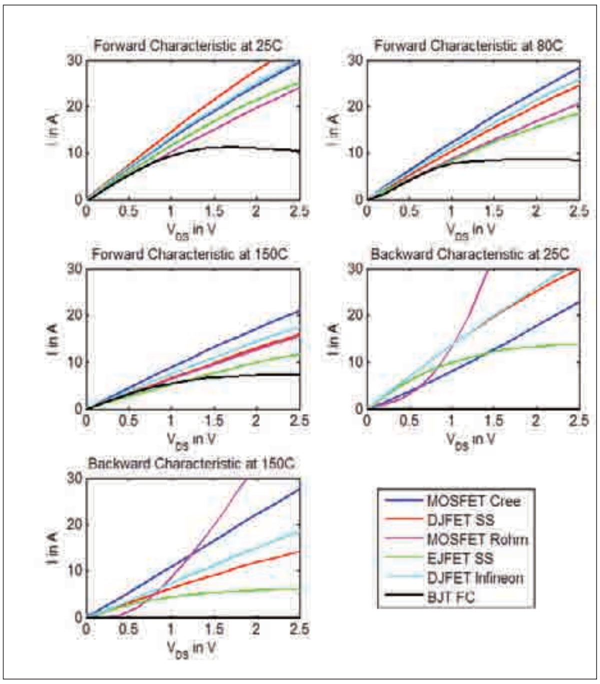


Figure 6: Conducting characteristic of the SiC power semiconductors at different temperatures and positive/negative current

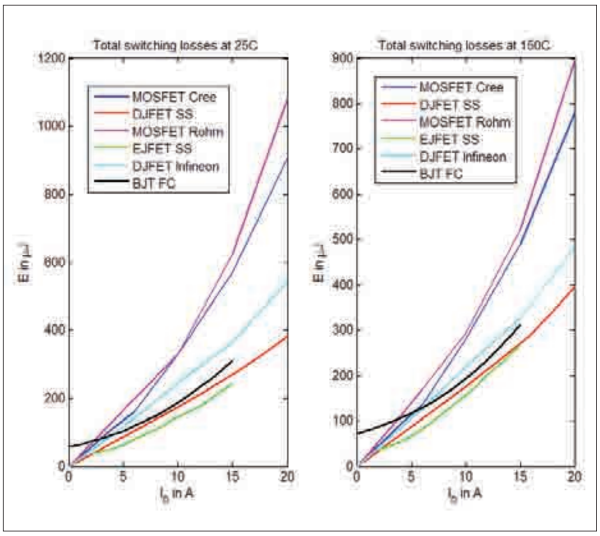


Figure 7: Switching losses at 25°C and 150°C versus current at 650 V

Regarding the dynamic performance the JFETs and the bipolar transistor show significantly lower losses than the MOSFETs. Especially for the bipolar transistor but also for the JFETs the test setup and the use of discrete components, with their parasitic effects turned out to be the limiting factor. Therefore the switching times had to be artificially slowed down by applying ferrite beads.

The temperature dependence of all investigated power semiconductors is low and some even show a slight reduction in switching losses at high temperatures.

Regarding cost, the processing of the raw material Silicon Carbide is significantly more expensive than Silicon. Firstly, the manufacturing process itself is more complicated as it requires many process steps at higher temperatures and longer time. Secondly, the number of defects per wafer is much higher, so that only a small proportion of the raw material can be used for the production of semiconductors [12]. This is also the reason why SiC switches are manufactured with rather low current capacities, because the probability of producing a defect-free chip is better the smaller the chip area is and thus the current capacity. At present the cost per chip varies and should therefore be requested directly from the manufacturer at interest.

Conclusion

All relevant SiC power semiconductors were investigated in terms of their electrical features. A final assessment, which of these power semiconductors is the best cannot be given because this depends very much on the final application. In fact each SiC power

semiconductor has its specific advantages. Therefore a universally valid recommendation for one of these power semiconductors cannot be given.

This work was supported by the project "SUNRISE - Opbygning af innovationskapaciteten vedrørede solcelle-anlæg" and partly funded by Region Syddanmark (journal 09/12927) and the EU. It was first presented at PCIM Europe 2012 under the title "Comparison of Six Different SiC Power Switching Devices in the 1200 V Range".

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Asymmetrical Parasitic Inductance Utilized for Switching Loss Reduction

High efficiency of power conversion circuits is a design goal on its own. The reduction of switching losses is the basis for higher switching frequencies which lead to a reduction of the size and weight of the passive components. The improvement from 96 % to 99 % efficiency will reduce the effort for cooling by factor 4. With the utilization of parasitic inductance and consequent execution of basic rules of power electronics is a new power electronics solution based on standard Si components disclosed which extends the traditional designs. The presented new power module concept combines a low inductive turn off with the utilization of the parasitic inductance for a reduction of the turn on losses and the usage of three level switching circuits with the paralleling of fast switching components with components with low forward voltage drop.

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The goal of this development project is the reduction of switching losses in power applications >100 kW with screw type modules. The limitations in such applications are mainly parasitic effects as stray inductance [7, 8] and reverse recovery behavior of the diodes [5]. The over-voltage spike caused by the parasitic inductance will limit the turn-off switching speed. The losses and the increased electromagnetic influence (EMI) caused by the reverse recovery behavior of the freewheeling diode is the drawback for increased turn-on switching speed. In a first step, the parasitic inductance is reduced to a minimum to solve the issue with turn-off. In a second step are the turn-on losses reduced. This is achieved with the utilization of the parasitic inductance for turn-on by keeping the low inductive turn-off behavior. The third activity for a switching loss reduction is the introduction of a neutral point clamped (NPC) inverter topology. Finally a special topology for paralleling MOSFET with IGBT is introduced to show the advanced prospects of the idea. The feasibility of the new concept is proven with a power module concept incorporating all the discussed arrangements.

Theory about switching losses with inductive load

The power dissipation in power electronics is caused by conductive losses and switching losses. The conductive losses are defined by the forward voltage drop in the semiconductor. The switching losses are dependent on the switching speed of the transistor, the reverse recovery behavior of the diode, serial inductance, and additional parasitic effects.

In a system with inductive load (see Figure 1) is the freewheeling diode conducting at turn on and the output voltage equals the negative DC-bus voltage (DC-). The transistor starts now to conduct. As soon the transistor takes over the complete output current, the output voltage will develop to the positive DC-bus voltage (DC+). The diode faces reverse voltage and will conduct in reverse direction. This will cause losses in the diode (EREC) and it will increase the current in the transistor. This current peak is often the root cause of EMI in the system. After the diode is completely recovered and blocking, the current in the transistor will fall back to the level of the output current. The turn-on process is now complete. An increased serial inductance with the transistor will reduce the turn-on losses. The energy stored in the serial inductance is calculated according [9] to $E_L = 1/2 \times L \times I^2$.

At turn off will the voltage at the transistor develop up to the DC-bus voltage level. The diode will take over the output current. The over-voltage will cause additional losses and it endangers the transistor to be destroyed. The usage of fast transistors is limited on the inductance and the maximum current, as the voltage peak is dependent on the turn-off speed. The

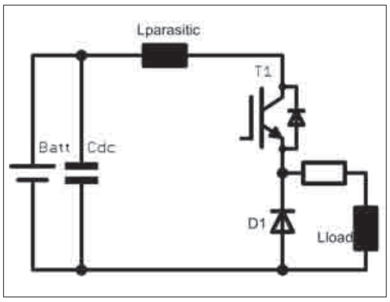


Figure 1: **Switching circuit with inductive load**

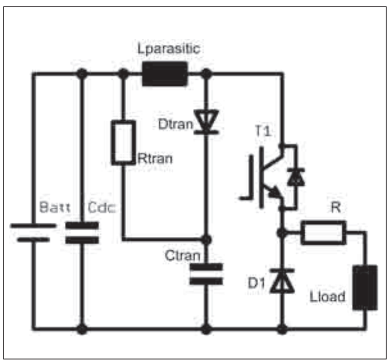


Figure 2: **Asymmetrical inductance in a switching circuit with feedback to the main DC-link**

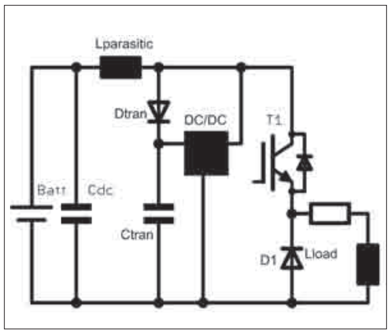


Figure 3: **Asymmetrical inductance in a switching circuit with regeneration of the stored energy**

stored energy in the serial inductance of the DC-input causes a voltage over-shooting according [1] to $V_{CE(peak)} = V_{CE} + L \times di/dt$.

Low inductive module technology

With the new low inductive module technology [3] we achieve:

- Fast and reliable turn-off of high current power modules and
- switching loss reduction (turn-off).

The reduced voltage overshot at turn off allows the usage of fast components. The reduced inductance will not reduce the switching losses at turn-on. The turn-off losses will decrease but the turn-on losses of the transistor and the reverse recovery losses in the diode will increase even more [4]. The efficiency of low inductive circuits will increase with the utilization of fast components. The goal of low turn-on losses without increasing EMI requires ultra fast freewheeling diodes.

Asymmetrical inductance

Increased inductance at turn on and ultra low inductance at turn off is the new goal. This approach is named "Asymmetrical Inductance". The way to achieve the new switching behavior, is the utilization of the parasitic inductance $L_{parasitic}$ at turn-on and bypassing it during turn-off. The diode D_{tran} (see Figure 2) assigns the stored energy of the parasitic inductance during turn-off to the integrated capacitor C_{tran}.

The stored energy circulates in $L_{parasitic}$, D_{tran} and R_{tran} until it is dissipated in the parasitic resistor. With this circuit we are able to release the semiconductor from switching losses but some energy has to be dissipated in passive components. The regeneration of the stored energy with a DC-DC circuit (see Figure 3) is an option to increase the efficiency.

Verification of the asymmetrical inductance

The idea is verified with the comparison of different parasitic inductance on a traditional power module setup and asymmetrical setup with integrated snubber capacitors (see Figures 4 - 6).

Test conditions were RG = 2Ω (+/-15V), V_{DC} = 600V, I_{OUT} = 400A with Infineon HS 3 / 1200V / 400A.

Results: E_{ON}=16,92 mJ, E_{OFF}=27,78 mJ, E_{REC}=31,78 mJ. The switching losses are fine but more important is the voltage over-shooting at turn-off. The most critical case is turn-off at low temperatures. At 25°C is an over-voltage of 180 % measured which limits the usage to 650 V. Safe turn-off at over-current conditions is not anymore possible. In our test the module failed at 720 A / 600V / T_J=25°C.

The identical measurement is now performed with asymmetrical inductance of 50 nH at turn-on and 5 nH at turn-off (Figures 7 - 9).

Results: E_{ON}=15,487 mJ, E_{OFF}=25,66 mJ, E_{REC}= 28,27 mJ. The switching losses of the new asymmetrical setup are lower. Surprisingly are not only the turn off losses reduced, all switching losses are reduced. The reason for the turn-on loss reduction is the reverse recovery behavior of the circuit.

At turn-on is the current of the transistor T1 increased by the reverse recovery current through the diode D1. After completed recovery is the current reduced but in the parasitic inductance $L_{parasitic}$ is the additional energy stored which causes an over-voltage at the collector of the transistor compared with the positive voltage in the transient capacitor C_{tran}.

The energy will flow into the capacitor.

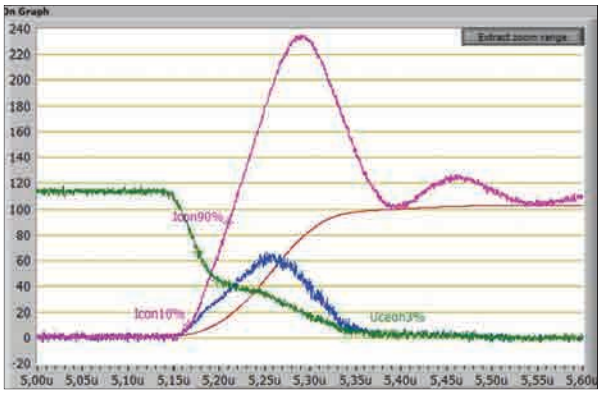


Figure 4: IGBT turn-on characteristics with symmetrical inductance L[ON] = L[OFF] = 50 nH

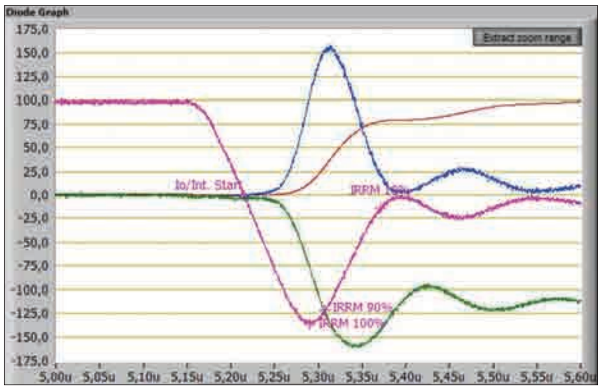


Figure 5: Diode characteristics with symmetrical inductance L[ON] = L[OFF] = 50 nH

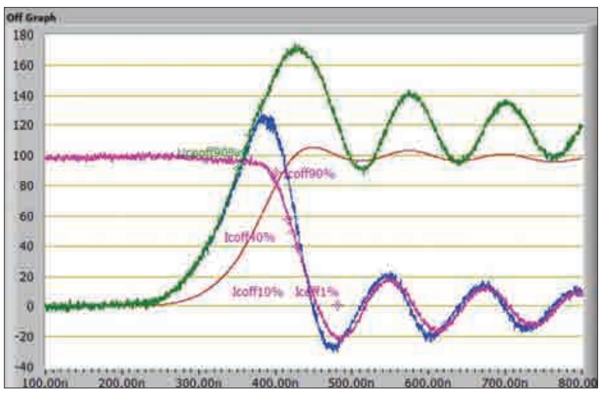


Figure 6: IGBT turn-off characteristics with symmetrical inductance L[ON] = L[OFF] = 50nH

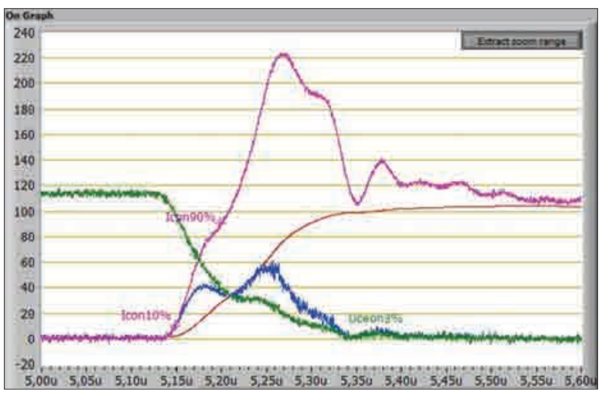


Figure 7: IGBT turn-on characteristics with asymmetrical inductance L[ON] = 50 nH, L[OFF] = 5 nH

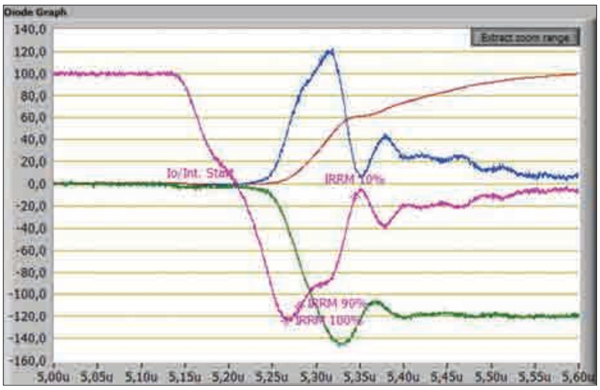


Figure 8: **Diode characteristics with asymmetrical inductance L[ON] = 50 nH, L[OFF] = 5 nH**

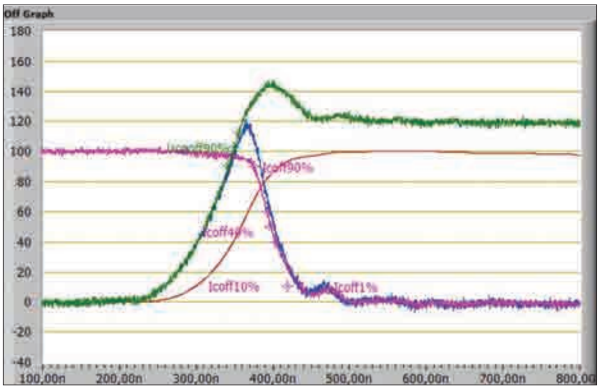


Figure 9: **IGBT turn-off characteristics with asymmetrical inductance L[ON] = 50 nH, L[OFF] = 5 nH**

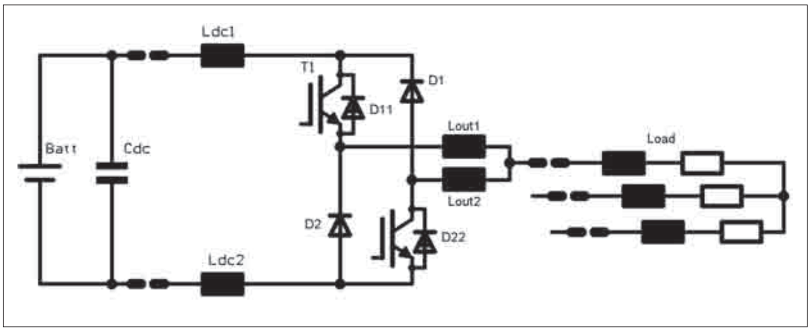
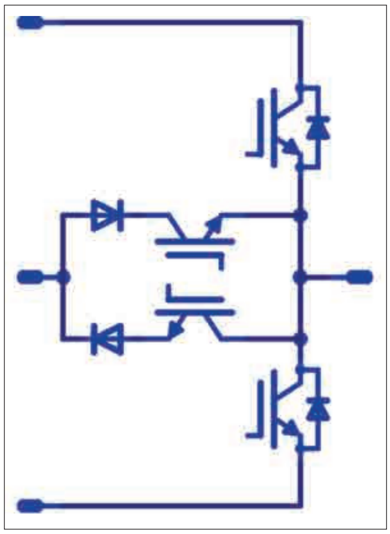
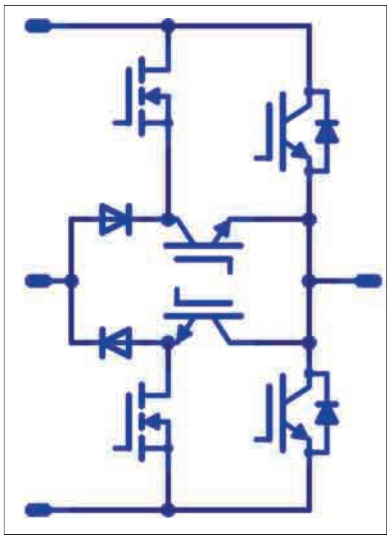


Figure 10: **Pseudo half-bridge topology with decoupled branches for improved switching behavior**



ABOVE Figure 11: **Mixed voltage NPC circuit**



ABOVE Figure 12: **Advanced paralleled NPC circuit**

This will reduce the reverse current in the diode and the voltage drop in the transistor which results in a significant reduction of the switching losses.

With the asymmetrical inductance circuit, it is possible to increase the inductance further to take advantage out of the turn-on loss reduction.

In a setup with $L_{parasitic}$[ON] = 90 nH, $L_{parasitic}$[OFF] = 5 nH we get E_{ON}=12,44 mJ, E_{OFF}=25,77 mJ, E_{REC}=26,70 mJ.

Decoupling of upper and lower transistor

The circuit in Figure 10 is a solution for reducing the turn-on losses due to the output capacitance of the complementary switching device and the elimination of cross conduction during turn-on. The goal of this idea is the decoupling of the output transistors. The output is divided into two branches and the parasitic inductance of the output connection is utilized to decouple the components. The corresponding diodes are direct connected for achieving a low inductive commutation loop.

Multi level topology

The usage of multi level topology as neutral point clamped inverter (NPC) or mixed voltage NPC inverter cuts the voltage at the switching transistor into half which reduces the switching losses accordingly [2]. On top on this loss reduction have the freewheeling diodes to be sized only for half of the voltage e.g. 600V instead of 1200V. But for 600V are many components with ultra fast reverse recovery behavior available.

The target of "Advanced Paralleling" is to merge the advantages of standard NPC with mixed voltage NPC [6] (see Figure 11). Here the output current faces only one junction, this leads to reduced static losses.

Parallel switch is the paralleling of a fast component (e.g. MOSFET) and a component with low voltage drop (e.g. IGBT). The loss reduction is achieved by rendering the static losses of the switch to the IGBT and the dynamic losses to the MOSFET. Even smarter is to use a so-called mixed voltage NPC topology and to parallel with just 600V MOSFETs a 1200V IGBT (see Figure 12).

In the advanced paralleled NPC is the original idea of paralleling MOSFET with IGBT maintained (see Figure 13). The MOSFET and the IGBT are turned on simultaneously. The MOSFET as the faster device will take over the current at turn-on. The IGBT will turn on with zero voltage. The voltage drop in the IGBT is lower so the IGBT will take over the major share of the current. At turn-off is the gate signal of the MOSFET delayed. The IGBT will turn off, the MOSFET will take over the current and will turn off with a delay of some 100 ns.

The measurements are showing that the advanced paralleled NPC topology is able to cut the switching losses into half.

The inverter reaches now more than

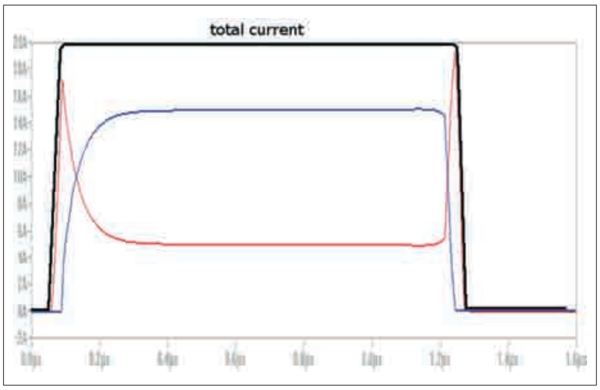


Figure 13: **Current sharing in the parallel switch system (red current in the MOSFET, blue current in the IGBT)**

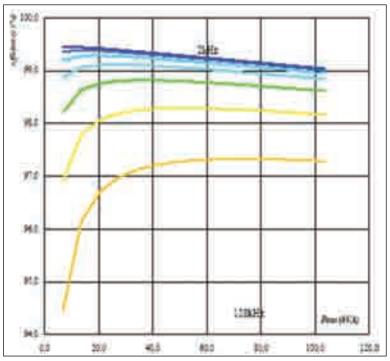


Figure 14: **Advanced paralleled NPC - efficiency vs. switching frequency in steps from 2 kHz to 128 kHz doubling in each step - 2 (blue), 4, 8, 16, 32 (green), 64 (yellow), 128 kHz (orange)**

99% efficiency with a PWM switching frequency of 16 kHz. At 64 kHz switching frequency is the efficiency still above 98% (see Figure 14)!

Power module concept

The combination of all this ideas leads to the following power module specification:

- 200 kVA output power at 20 kHz
- Asymmetrical parasitic inductance with energy regeneration
- Decoupling of low side and high side switches
- Three-level topology
- Paralleling of fast MOSFET or IGBT _s with components having low static losses.

With these ideas in mind we developed a power module concept:

- 1200V/500A power rating
- Asymmetrical parasitic inductance with onboard snubber capacitors (5nH turn-off inductance) and DC-DC regeneration circuit
- Separated outputs for high- and low-side circuit for decoupling of the corresponding switches
- 3-phase advanced paralleled mixed voltage NPC topology.

The result is shown in Figure 15 and Figure 16. The inductance shown in the schematics is the parasitic inductance of the power module setup.

Conclusion

Beside the advantages of new technologies as SiC or GaN switching components it is still possible to increase the efficiency with standard Si Components. To extend traditional power designs we have to remember the basics of power electronics.

The low inductive module concept ensures the fast and reliable turn-off in high current power modules and reduces the voltage over-shoot. The power module setup with very low internal parasitic elements it is able to utilize the external stray inductance for a reduction of switching losses without investing in expensive high-speed semiconductor technology. The asymmetrical inductance leads to lower switching losses, reduced EMC and minimized effort for the inverter mechanics. Low inductive bus bars are not needed anymore. A flexible low cost cable connection in the DC link can be used. The increased serial inductance will just cause additional reduction of the turn-on losses. The parallel switch technology achieves highest efficiency at elevated switching frequencies of 50 kHz and more.

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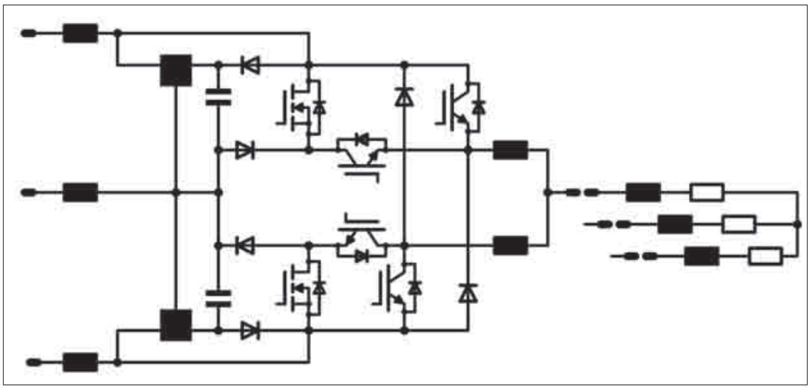

ABOVE Figure 15: **Power module concept for a 3-phase advanced paralleled NPC with asymmetrical inductance and regeneration circuit**

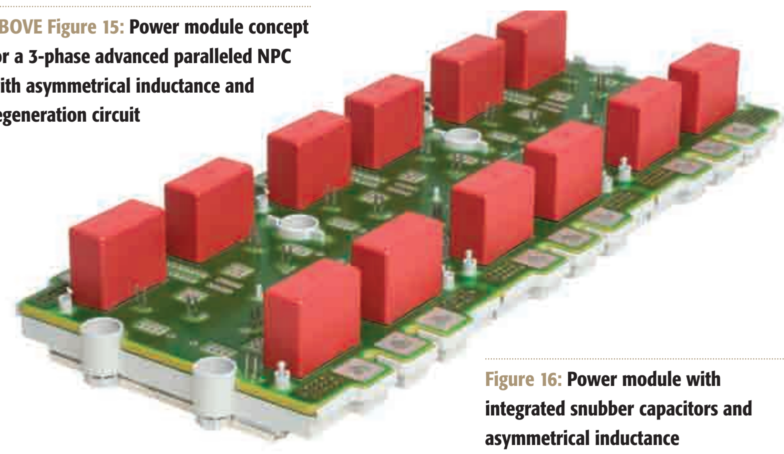

Figure 16: **Power module with integrated snubber capacitors and asymmetrical inductance**

Static Loss Measurement Methods for Quality Improvement

Steady increase of power for electric converter units leads to the constant enhancement of characteristics and load capacity of power semiconductors. Thus, requirements to the maximum current load of power thyristors and diodes, limited by heat-release losses in a semiconductor element and the intensity of heat removal from the die, are also increasing. Power semiconductor manufacturers do their best to the maximum reduction of conducting losses and preserving all the remaining characteristics at the required level by precise measurement of forward voltage drop. **Alexey Poleshchuk, Automation Lab Engineer, Proton-Electrotex, Orel, Russia**

Sufficiently small spread of parameters within 10-15% range can have a key influence on comparative load capacity of semiconductors due to the restrictions of maximum heat removal from the die. On the other side, it's often necessary to commute the currents higher than current-carrying capacity of large diameters dies (90 mm and more). In this case it's necessary to connect power semiconductors in parallel in a single unit where the devices should be precisely selected according to their characteristics in order to provide symmetric semiconductor load and annealing of heat release.

The above-mentioned tasks determine the necessity of maximum precise measurements of semiconductor characteristics, responsible for the static losses of conductivity (in this case - peak on-stage voltage (V_{TM}), for their correct classification and selection in groups for parallel connection. In order to measure V_{TM} at the operating currents in semiconductors with large diameters it's necessary to have the equipment able to form current pulses of desired amplitude and form with high accuracy and frequency. Thus not only current pulse amplitude is significant for characteristics measurement, but also its length, form and further treatment of the received data are important as well.

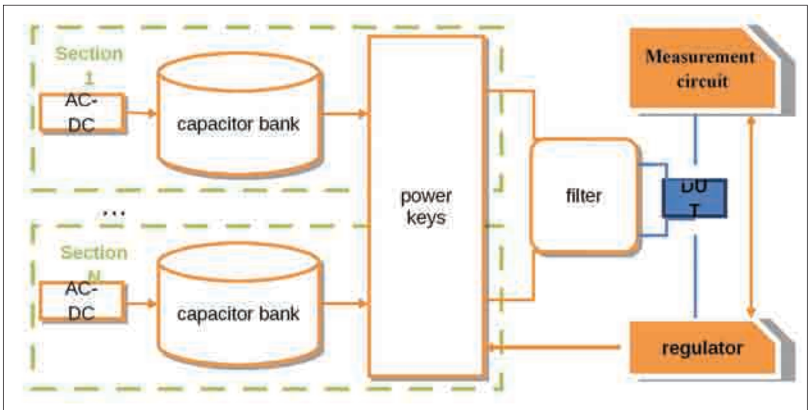

Figure1: Functional scheme of measuring module

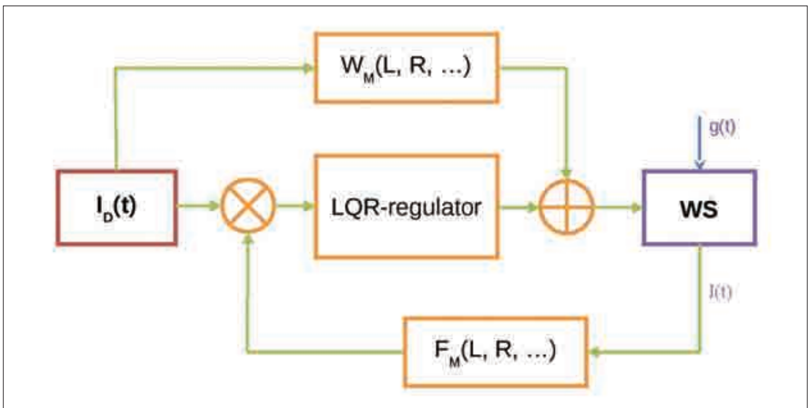

Figure 2: Simplified schematic of current regulator

Current pulse formation

The developed equipment uses the parallel buck-converter topology operating as a current supply to form a current pulse with variable form. A set of capacitor banks (batteries) commuted by high-speed IGBT modules serves as the energy supply for the pulse and is aimed to form current pulse with the desired form and amplitude after filtering. Module construction with parallel connection of cells allows sizing unit power within broad limits of 1 to 9 kA and maintaining independent automatic diagnostics of the condition of each battery.

By using the adaptive circuit of signal digitalization and digital control of power keys it's possible to obtain almost any form of current pulse, including trapezoidal, half sinusoidal, step trapezoidal and S-shaped.

The main requirement to the control circuit is the maximum precise generation of the desired current pulse with length small enough, as well as provision of its repeatability within the series of tests.

Moreover, the characteristics of the circuit runs are rather stable and do not change during the measurements. This allows realizing current regulator that performs current control in the circuit on the base of previously formed mathematical model (model following control). The scheme in Figure 2 consists of

* $I_D(t)$ - desired form of current pulse;
* W_M - model of the object controlled, current circuit;
* F_M - filter of measured current value;
* I(t) - actual current value in a circuit;
* g(t) - external perturbation;
* LQR-regulator - regulator, minimizing an error of current pulse formation.

With the more or less identified system model it's possible not only to increase the processing speed of the desired signal, but to sensitize optimal filter and regulator to increase stability of the control circuit towards external clutter and noises. The latter is extremely important taking into consideration rather high level of electromagnetic noise, generated by the power keys.

Automatic identification of the circuit characteristics is based on determination of such parameters as ohmic resistance (R) of circuit, inductivity (L), effective capacitance of energy storage units (C) by providing the series of test pulses and aftertreatment of results for the system self-adjustment according to the present circuit characteristics. Besides, diagnostics of the capacitors batteries condition is performed to exclude their ageing effect and further system unbalance.

The above-mentioned opportunities provide deviation of actual current from the desired in dynamics less than 2-3% and repeatability of measurement results at the level of 0,6 - 0,9% (Figures 3, 4).

Treatment of digital measurement results

Main aim of the performed measurements is to receive more adequate V_{TM} (F_M) results of bipolar power semiconductors at the desired value of current and pulse form. Actual value of current fluctuates around target value during the measurements due to the pulse method of current regulation that provides a certain scatter into the measured values which appears to be the noised external disturbances. In order to get a more exact voltage value it's necessary to make an additional mathematical treatment of the measurement results. The known equation approximates the type of voltage-current characteristics of the power unit [1]:

$$V = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

While small deviations from the measurement point the formula can be

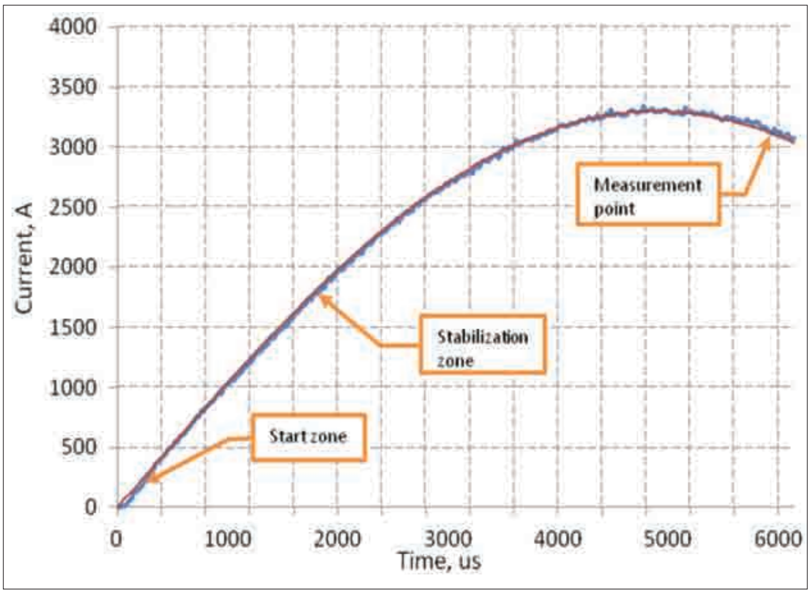

Figure 3: **Sinusoidal pulse 3.3 kA max**

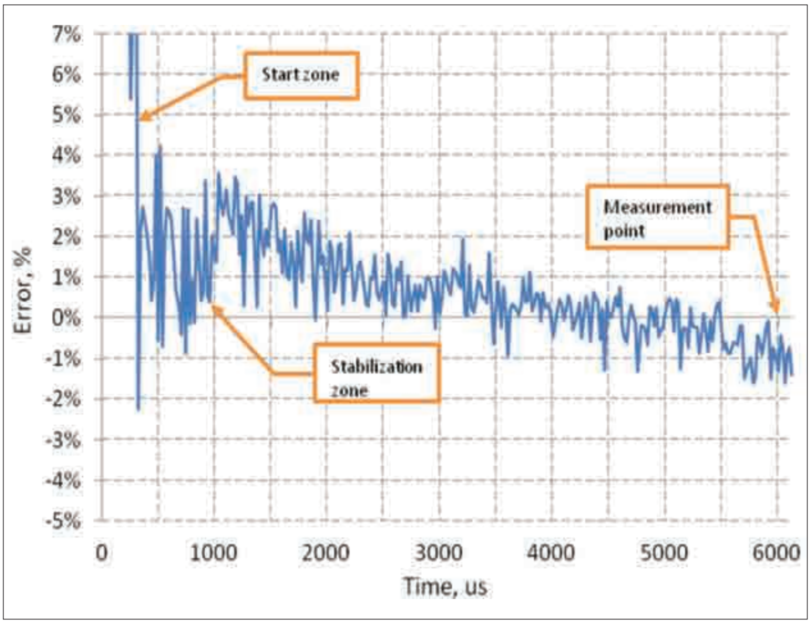

Figure 4: **Deviation between measured and desired results**

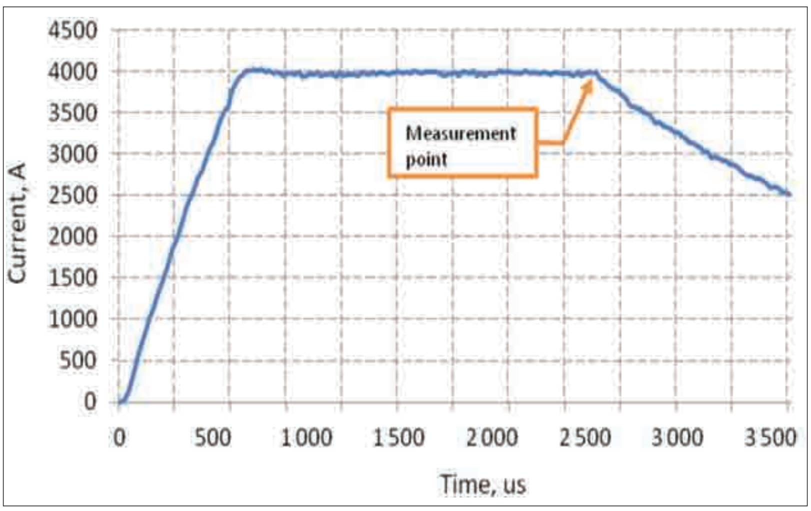

Figure 5: **Trapezoidal pulse duration of 2000 microseconds**

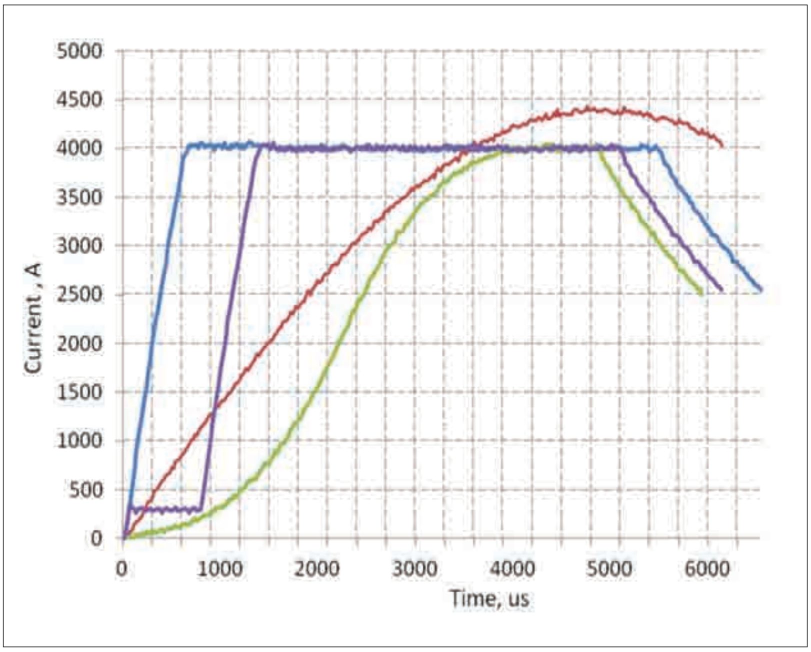

Figure 6: Different pulse forms for V_{TM} measurement at I_{TM} 4 kA

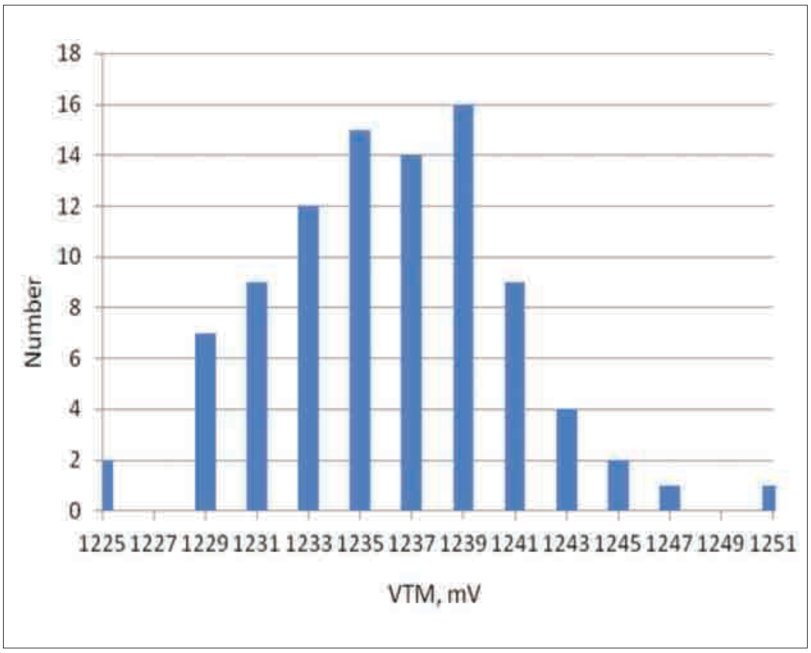

Figure 7: Scatter of measurement results for one device at I_{TM} = 1570A, 25°C. Average value of selection is M = 1235.53 mV, σ = 4.74 mV, that makes less than 0.7 % of the measured value

successfully linearized. Method of the smallest squires can be further used to the received sum of measurement results in order to obtain the most reliable estimate of the measured parameter. Measurement is performed not less than in 10-20 points of the neighborhood of the desired current value for the successful realization of the described method.

Measurement at different forms of test pulses

V_{TM} value may vary depending on the current pulse form due to the different heating-up of a semiconductor element as well as due to dynamic processes in the device. Main task is to provide equal complete opening of a power semiconductor for the running current, together with the minimization of its characteristics variation due to the heating by the running current. That's why it may be reasonable to use different test pulses forms: from sine-shaped to S-shaped (Figures 6 and 7).

Conclusion

Measurement of power semiconductor conducting losses allows for assembling of parallel stacks that have advanced operational reliability and more symmetric load of each device. For large diameter elements that have rather large turn-on time, the mentioned equipment allows to select optimal test mode that will minimize self-heating of an element together with provision of complete turn-on of a die into the conducting state across the surface.

The described measuring unit is a part of the complex for semiconductor static characteristics measurements. The complex ensures testing of thyristor and diode elements produced by JSC "Proton-Electrotex". Further developments will target at test equipment for large currents (20-30 kA) and test equipment for IGBT modules.

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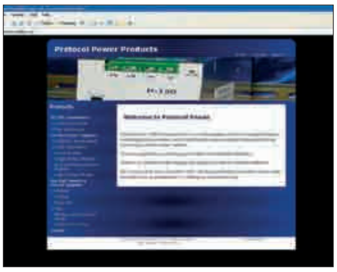

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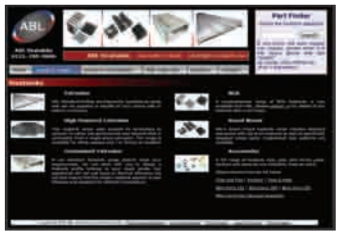

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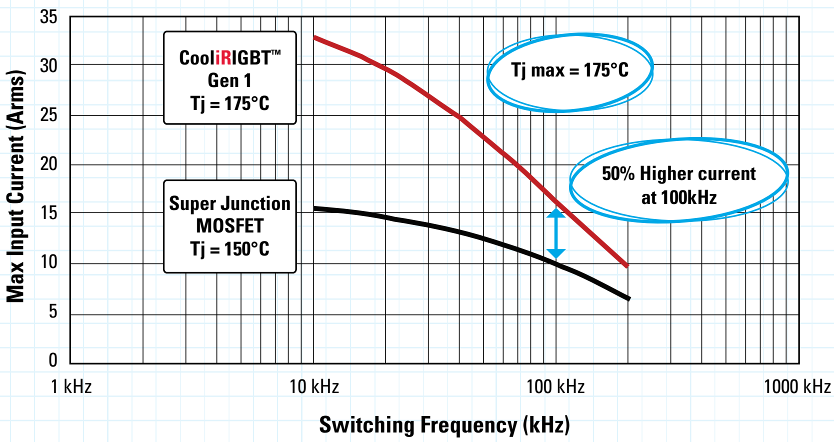

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