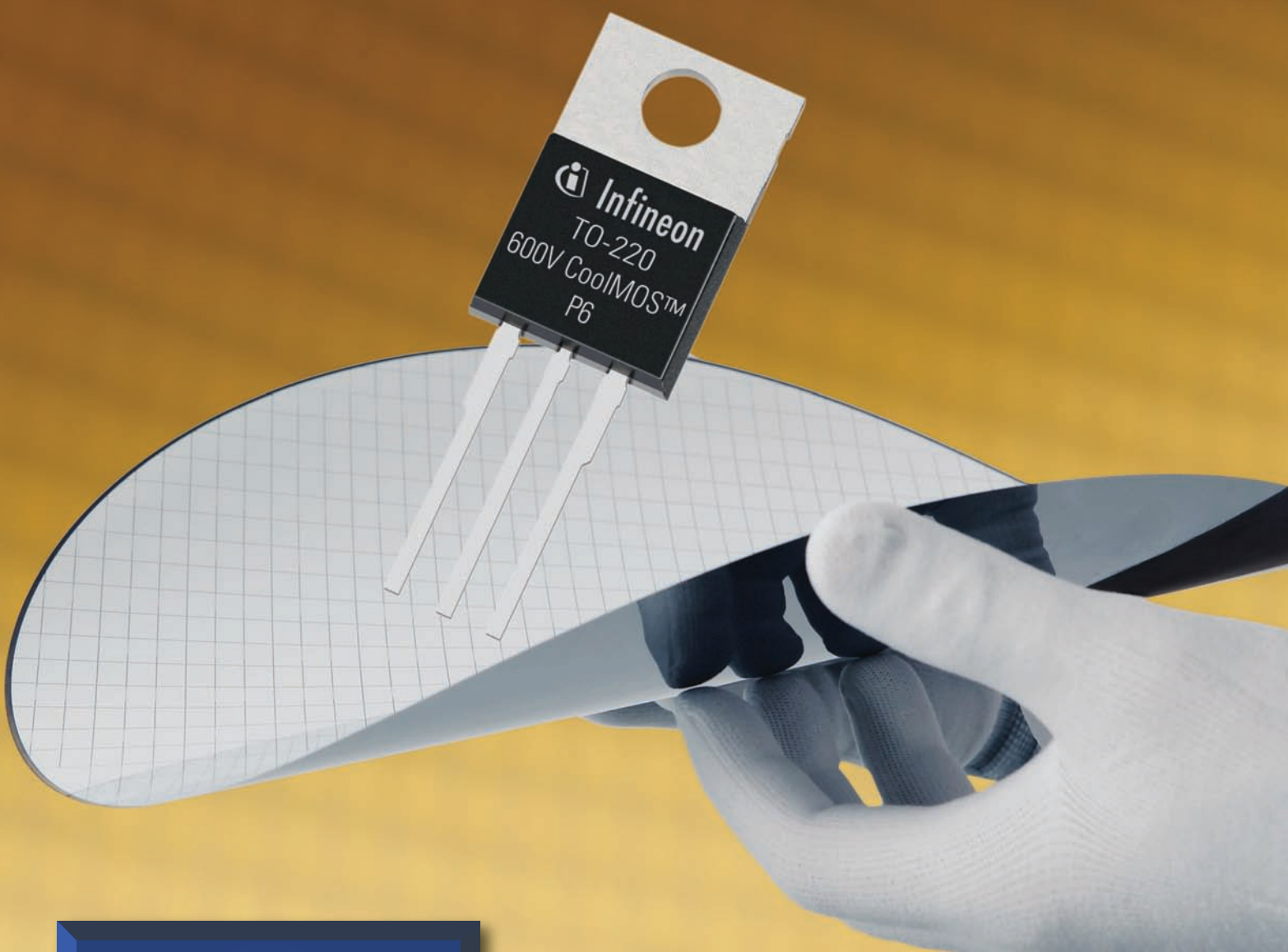


# POWER ELECTRONICS EUROPE

ISSUE 3 – April/May 2013 [www.power-mag.com](http://www.power-mag.com)

## SEMICONDUCTORS

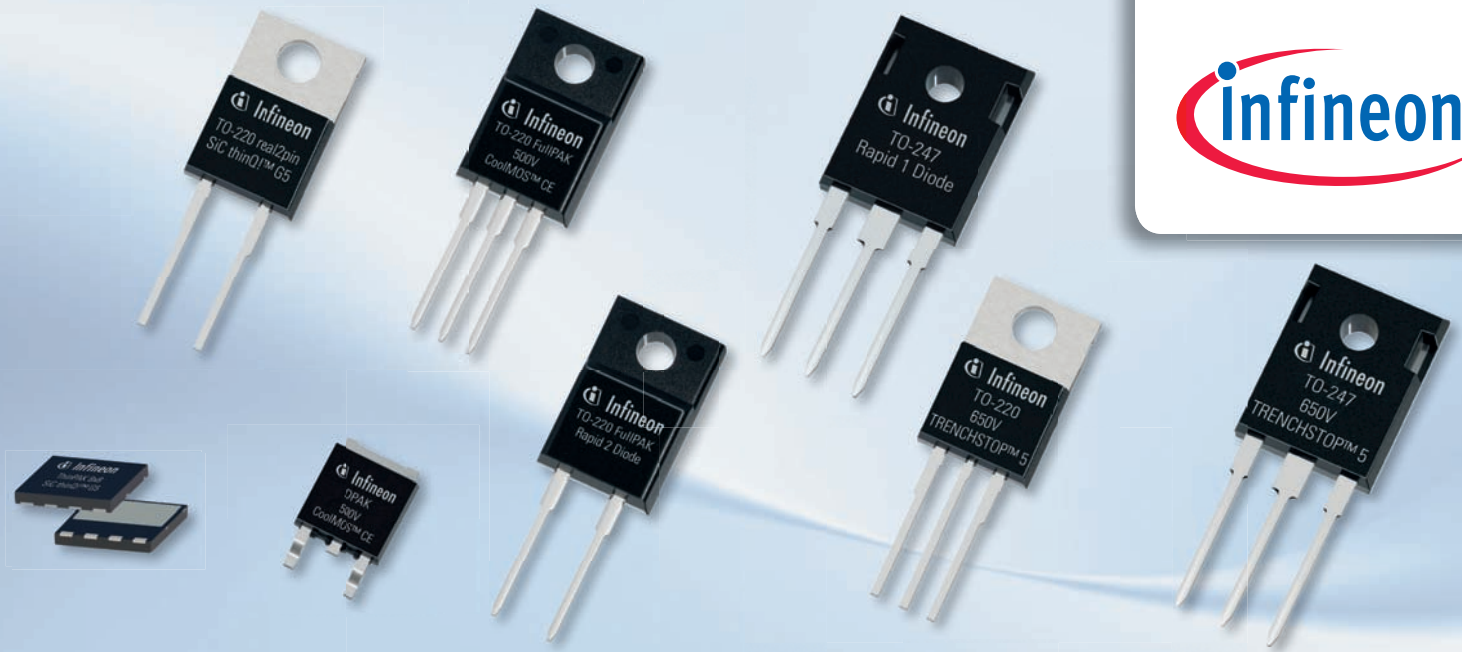
Power Semiconductors  
on 300-Millimeter Wafers



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FOR POWER ELECTRONICS  
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### Also inside this issue

Opinion | Market News | Power Electronics Research  
APEC 2013 | PCIM 2013 | Industry News  
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**PAGE 6****Market News**

PEE looks at the latest Market News and company developments

**PAGE 10****Power Electronics Research****COVER STORY****Power Semiconductors on 300-Millimeter Wafers**

In February 2013 Infineon Technologies released the first products of the CoolMOS™ family being produced on its new 300-millimeter line at the Villach site in Austria. The production process based on the new technology has completed qualification and is now ready for delivery. This follows more than three years intensive research and development activities within Infineon and with partners all over Europe in the fields of process technologies, production technologies as well as handling and automation for advanced power technologies based on 300mm wafers. Now Infineon is the first and only company worldwide to produce power semiconductors on 300-millimeter thin wafers. Thanks to their larger diameter compared to standard 200-millimeter wafers, two-and-a-half times as many chips can be made from each wafer. With this massive invest of capital and engineering efforts Infineon Technologies will be able to sustainably support the market with significantly enhanced capacity for leading edge power semiconductor devices. Full story on page 44.

Cover supplied by Infineon Technologies AG

**PAGE 14****APEC 2013****PAGE 25****PCIM 2013****PAGE 28****Industry News**

Thermal Design: Incorporating EDA and MDA Design Flows

Integrated MOSFET Buck Regulators

Driving GaN Switches Efficiently

**PAGE 38****GaN Transistors for Efficient Power Conversion**

For over three decades, power management efficiency and cost showed steady improvement as innovations in power MOSFET structures, technology, and circuit topologies paced the growing need for electrical power in our daily lives. In the new millennium, however, the rate of improvement slowed as the silicon power MOSFET asymptotically approached its theoretical bounds. **Alex Lidow, CEO, and Johan Strydom, VP Applications Engineering, Efficient Power Conversion Corporation, El Segundo, USA**

**PAGE 41****Industrial Grade 25 A Versatile Voltage Regulator**

At APEC International Rectifier introduced the IR3847 high current Point-of-Load (POL) integrated voltage regulator that extends the current rating of IR's third generation SuplIRBuck® family up to 25 A in a compact 5x6 mm package.

**Ramesh Balasubramaniam, Cecilia Contenti, Enterprise Power Business Unit, International Rectifier, El Segundo, USA**

**PAGE 49****Website Product Locator**



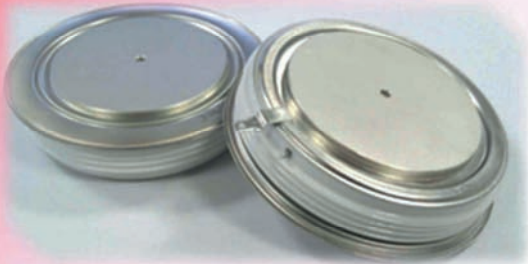
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### Phase control and Medium voltage thyristors

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### Gate turn-off (GTO) thyristors

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### Press-pack IGBT's

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IXYS UK can offer a range of isolated base diode/thyristor modules, including our new range of high power modules available with current ratings up to 1080A and voltage ratings up to 3600V

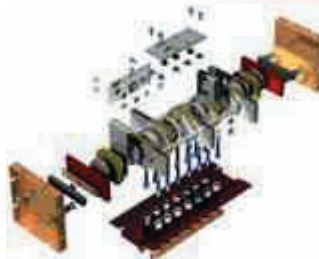


### Ancillary components

To complement our range of semiconductor devices, IXYS UK can offer a wide variety of ancillary components including, bar and box clamps, heatsinks, coolers, gate drives, leads, high speed fuses and snubber capacitors

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## The Next Power Evolution

in Room Brüssel 1. As the title indicates not only device technologies and properties will be discussed, but also the application possibilities.

Western industrialized societies rely on the use of electrical energy for providing a high quality of life for their citizens. The comforts of refrigeration, air-conditioning, and lighting are taken for granted by people. Convenient transportation and communication capabilities are no longer considered a luxury. These benefits are derived by ever increasing demands on our electrical power delivery systems which produces a detrimental environmental impact by causing a high level of carbon footprint, secondly 10 % of electrical energy is lost by conversion steps in the grid.. This can be overcome by better efficiency of the power electronic systems, illustrated by the development from early bipolar transistors to MOSFETs and IGBTs. The latest generation of promising devices are SiC and GaN, SiC has reached the point to be feasible and the next step will be GaN having a different cost structure, particularly in the combination with a Silicon substrate, so the opening statements at APEC 2013.

According to Yole Développement the SiC Devices market will surpass \$600 million by the year 2020. SiC device applications are today found in trains, wind turbines, EV/HEV, motor control and smart grids. SiC technology, compared to GaN and Silicon, provides strong added-value for high and very high-voltage applications (from 1.7 to 10 kV). Regarding Power GaN the market will evolve this year to reach \$100 million next year. Yole forecasts \$300 million already by the year 2015 to accelerate up to roughly \$2 billion in 2020. Early adopters will be in IT (power supplies), consumer and lighting, followed by automotive, motor drives (600 V) and battery chargers. IT applications are forecast to have a 50 % share in 2020 and automotive around 30 %. In general more lower power and lower voltage (up to 600 V) but high-efficiency applications such as PV inverters and (H)EV are foreseen in 2013/14/15 for GaN. Not only market researchers but also research institutes view a bright future for GaN since these devices open new future application and thus business opportunities not effectively possible with Si or SiC.

That's why at APEC 2013 a special GaN Rap Session has been organized with participation of leading vendors (see our comprehensive report). Also the upcoming PCIM in Nuremberg will focus on this subject in various sessions. But I will draw your interest to PEE's Special Session entitled "Power GaN for Highly Efficient Converters" on May 16, 2.00 pm

Though Japanese semiconductor manufacturers such as Fujitsu and Panasonic have recently announced they will enter the 600 V GaN market, the major players having devices ready come from the Americas. Thus this Special Session will feature Alex Lidow, CEO Efficient Power Conversion (EPC) El Segundo/USA; Umesh Mishra, CEO Transphorm Goleta/USA; Girvan Patterson, CEO GaN Systems Ottawa/Canada; and Michael Briere, ACOO Enterprises Scottsdale/Arizona for International Rectifier, El Segundo/USA. Efficient Power Conversion Corporation (EPC) has been in production with enhancement mode GaN-on-Silicon power transistors (eGaN FETs) for over three years. Much progress has been made improving device performance and reliability. Transphorm's Umesh Mishra investigates how GaN is making such rapid performance progress and uses test results to illustrate what is now possible using GaN compared to recent SiC transistor performance. He then predicts future improvements that will continue to make GaN a more attractive alternative to either Si or SiC for high efficiency systems. GaN Systems is investing heavily to accelerate the adoption of the new technology by designing CMOS integrated driver solutions onto which the GaN die is mounted directly in a stacked chip assembly combining the switch, its driver, sensors and customized interface circuitry. In solar and wind inverter applications the high voltage operation, embedded galvanic isolation and high speed operation of these devices offer the prospect of higher switching speeds with improved conversion efficiency, lower component count, smaller size and reduced conversion loss, as Girvan Patterson will explain. In The final presentation experimental results for the use of GaN based power devices in highly efficient high frequency power circuits such as AC/DC power supplies, DC/DC boost and DC/AC motor drive inverters are presented by Michael Briere. The current status of the development and current performance of the required 600 V rated GaN on Si based devices at International Rectifier are presented, including the development of crack free AlxGayN alloy based epitaxy on standard thickness 150 and 200 mm Si substrates. Results of long term reliability studies of more than 5000 hrs are presented, as well as results for device robustness under standard application conditions. Finally a short podium discussion between all speakers and the auditorium is planned.

PEE would be happy to welcome you at PCIM and our Special Session!

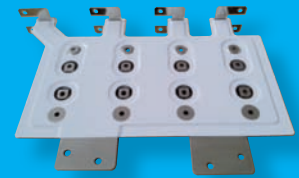
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# SiC Devices Market Exceeds \$600 Million by 2020

With its SiC technology & market analysis update arriving in May 2013, the French technology consulting company Yole Développement will announce that the SiC Devices market will surpass \$600 million by the year 2020.

"Two years ago we said the SiC industry is not a niche market anymore. We expect a SiC market with 30 % CAGR between 2015 – 2020," said analyst Philippe Roussel. SiC device makers now offer two main power electronics devices: the diode and the transistor.

Harkening back to 2011, SiC's two main players, Rohm and CREE, announced the

introduction of the first SiC MOSFET devices. The obvious question is, what's next? Per Yole Développement, SiC device applications are profligate today in a variety of fields, including trains, wind turbines, EV/HEV, motor control and smart grids... SiC technology, compared to GaN and Silicon, provides strong added-value for high and very high-voltage applications (from 1.7 to 10 kV). For applications exceeding 10 kV, only a few players are developing SiC devices, and the existing market is still very low.

For the third time, Yole Développement, the SiC Power Center and the Enterprise Europe

Network have joined forces to organize the International SiC Power Electronics Applications Workshop 2013 from June 9 to 11 in Sweden (IsiCPEAW), a unique European event dedicated solely to the Silicon Carbide industry. Key players such as CREE, Rohm, Mitsubishi and Infineon will swap SiC technology visions, exchange insights on market developments, and identify business opportunities. In 2012 the workshop welcomed 200+ attendees from around the world.

[www.yole.fr](http://www.yole.fr)

## Restructuring at Semikron

The SEMIKRON Group is being restructured to become more responsive to global developments. These developments refer to market flexibility requirements as well as to corporate organization structures.

In the course of these restructuring activities, Harald Jäger has been appointed a new member of the board. He joins the top management team consisting of the present directors of many years, Peter Frey (Sales) and Thomas Dippold (Corporate Finance). Harald Jäger has held various management positions throughout the company for almost 20 years. He will be responsible for production and engineering. Dirk Heidenreich will retire from operational management, but will continue to take on other

responsibilities for the company. He will remain the Managing Director of the SEMIKRON owner families' non-operative holding company, SEMIKRON International Dr. Fritz Martin GmbH & Co KG. "After 25 years of being responsible for operative business, the time has come for me to lay operational leadership in new hands. I will focus on the company's strategic alignment in the future, and will work as a consultant to the new management team", he commented. Thomas Stockmeier, CTO at SEMIKRON, left the company in February.

[www.semikron.com](http://www.semikron.com)



**Harald Jäger (left), Peter Frey and Thomas Dippold form Semikron's new top management**





# IGCTs making grid code issues a thing of the past?

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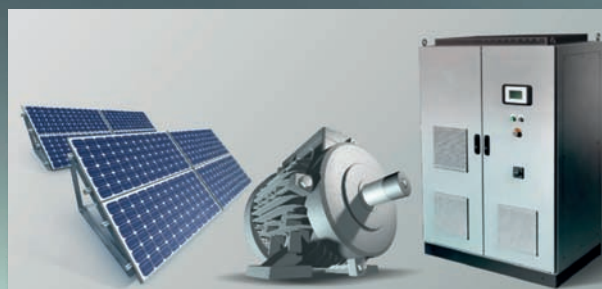
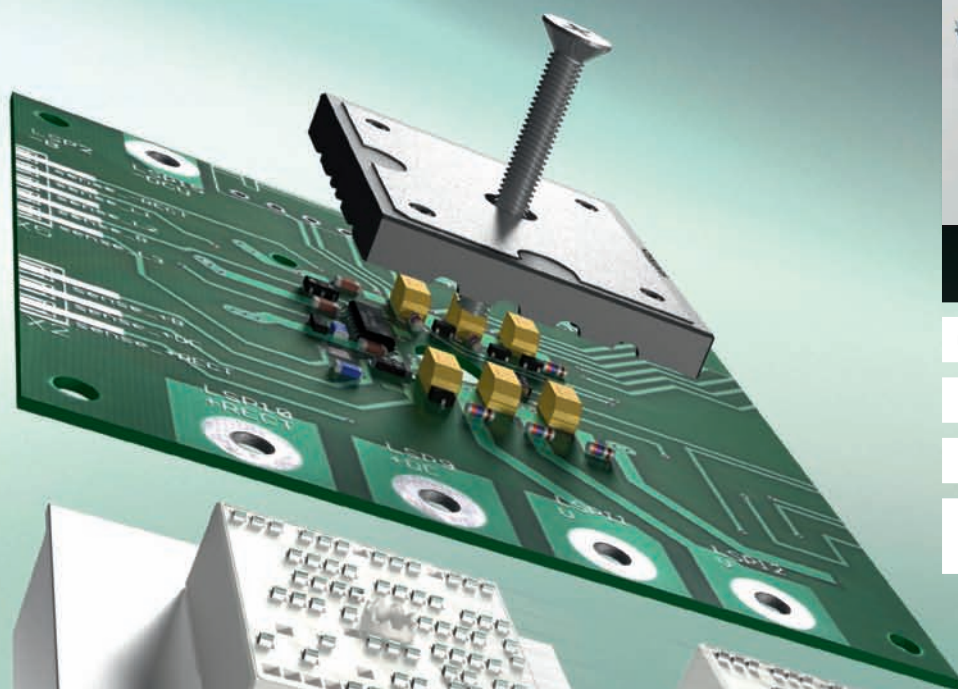


ABB's integrated gate-commutated thyristors (IGCTs) powered converters support turbine manufacturers to achieve grid code compliance. IGCT is the semiconductor of choice for demanding high power applications such as medium voltage drives, marine drives, co-generation, wind power converters, interties and STATCOMs. ABB's portfolio offers a complete range of IGCTs and diodes for all your high power switching needs. For more information please visit our website:  
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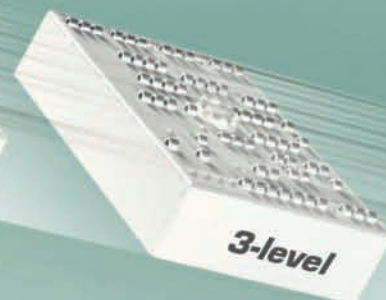
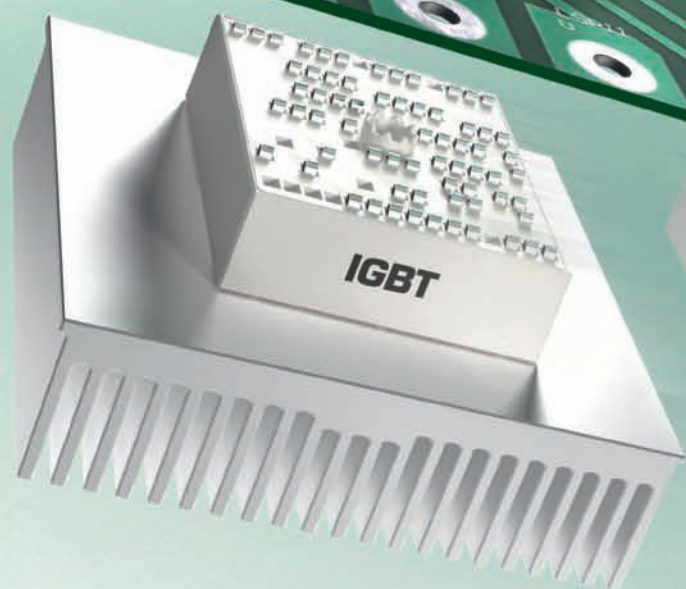
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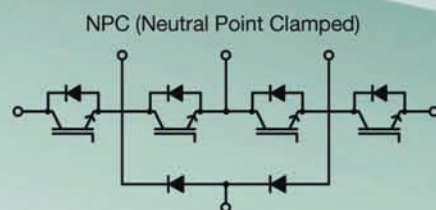
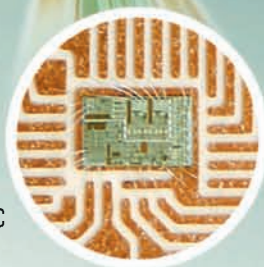
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# Drive Profit Margins Down in 2012 but Forecast to Improve

IHS forecasts that global compact AC low-voltage drive sales will grow to \$3 billion in 2016. Compact AC drives are those rated less than 25 kW, used primarily in fan and pump applications. End-users are increasingly demanding a low priced, simple product and the industry is responding by splitting compact AC motor drive product lines into a simpler lower-priced line and a more complex, higher-functioning and expensive drive.

"Compact AC drive average selling price declines accelerated in 2012, especially in EMEA and Japan where prices fell nearly 4 percent. Suppliers accepted lower overall margins on compact drives to maintain and secure customers to which they sell higher margin products," comments analyst Rolando Campos. Despite economic slowdowns in Asia and Europe in 2012, demand for low-end drives remained strong, partly due to lower prices facilitating budget approvals in a

tight-lending environment, but also as separate lines of drives increased options for customers. In 2012, compact AC drive shipments grew 2.6 percent over 2011 levels, reaching nearly 11 million unit shipments. The Chinese market for compact AC drives has grown rapidly over the past several years to \$880 million in 2012 and forecast to nearly double in 2016.

Due to intense competition and the penetration of new lower cost compact drives, profit margins declined in 2012. Reluctance to reduce compact drive prices in line with the overall industry has resulted in a loss of market share for some companies in EMEA and Japan. In response to a more competitive market, some suppliers are moving towards drive products and markets with less competition, more opportunity to add value, and higher potential margins.

[www.ihs.com](http://www.ihs.com)

## Siemens is Boosting E-Car Power Electronics

The Siemens Drive Technologies Division has signed a cooperation agreement with Semikron International in order to intensify their future collaboration in power electronics for electric vehicles. Under the agreement Siemens has taken over the fully owned Semikron subsidiary VePOINT, which has 30 highly qualified employees based in Nuremberg.

VePOINT develops innovative power electronic components and systems, based on Semikron's SKiN technology, specifically for the hybrid and electric vehicle market. SKiN does not require conventional soldered joints or wire bonds. These solutions complement the Siemens range of products by adding systems with attractive power densities and power/weight ratios for automobile applications. The cooperation agreement between Siemens and Semikron will also see a continuation of the existing close collaboration of the two companies in the field of power modules. Jörg Grotendorst, CEO of the Siemens Inside e-Car Business Unit, said, "The cooperation with Semikron and the acquisition of VePOINT are important milestones for us on our way toward achieving a high degree of integration in the entire drive train. This widens the Siemens range of motors, inverters, speed sensors and gearboxes by adding further innovative e-Car power electronics".

[www.industry.siemens.com/topics/global/en/electric-vehicle](http://www.industry.siemens.com/topics/global/en/electric-vehicle)



Siemens' E-Car inverters will incorporate Semikron's SKiN technology



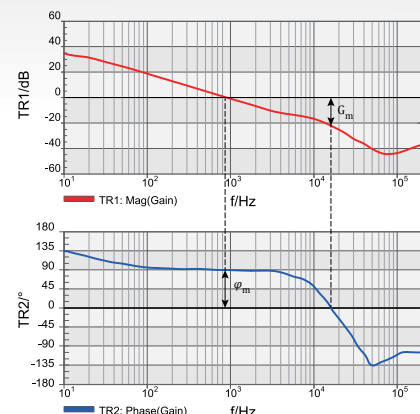
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# European Power Electronics on the Forefront

On April 17/18 the European Center for Power Electronics (ECPE) celebrated its 10th anniversary in Nuremberg as a European research network linking applied technology institutes, universities and companies in a pre-competitive environment. Representatives from research and industry gave an overview on the European and global status of the power electronics market.

Starting with eight founding members on 17 April 2003, ECPE has grown to an acknowledged European research network comprising 70 member companies and the same number of competence centers from universities and research centers.

"ECPE has significantly contributed to education and training to overcome the shortage of qualified personal in power electronics and has developed a technology platform for driving pre-competitive research projects", General Manager Thomas Harder pointed out. ECPE's annual budget is around € 800,000. "As the Industry-driven Power Electronics Research Network covering the value chain from the materials and components to the systems and applications ECPE strengthens the cooperation between Power Electronics industry and universities & research centers on a European level. Research is performed in the competence centers, where our members may contribute to projects. As a European Technology and Innovation Platform we are driving pre-competitive joint research and we set up research & technology roadmaps for a strategic research agenda with future research directions according to the demands of European power electronics industry. And with one strong voice of the power electronics community to the public and to politics we create awareness for the role and importance of power electronics regarding the megatrends in society e.g. energy efficiency, use of renewable energies, smart grids and e-Mobility", Harder said.

## From automotive power

One of the European strategic market segments for power electronics is automotive. Martin März from Fraunhofer Institute IISB outlined in his speech "System Integration in Automotive Power Electronics" some of the lighthouse projects which have influenced some industrial developments. "Our HEV demonstrator featuring an integrated motor/generator situated in the gearbox provided a platform for new designs such as a direct water cooled power module substrate. Si-Fe soft magnetic material as an other example is well suited for EMI filtering. In conjunction with a ring-shaped capacitor, designed for the HEV demonstrator, size and cost for DC link applications can be substantially reduced, and this material is patented by ECPE. Additionally an automotive 120 kW DC/DC converter has been designed switching at

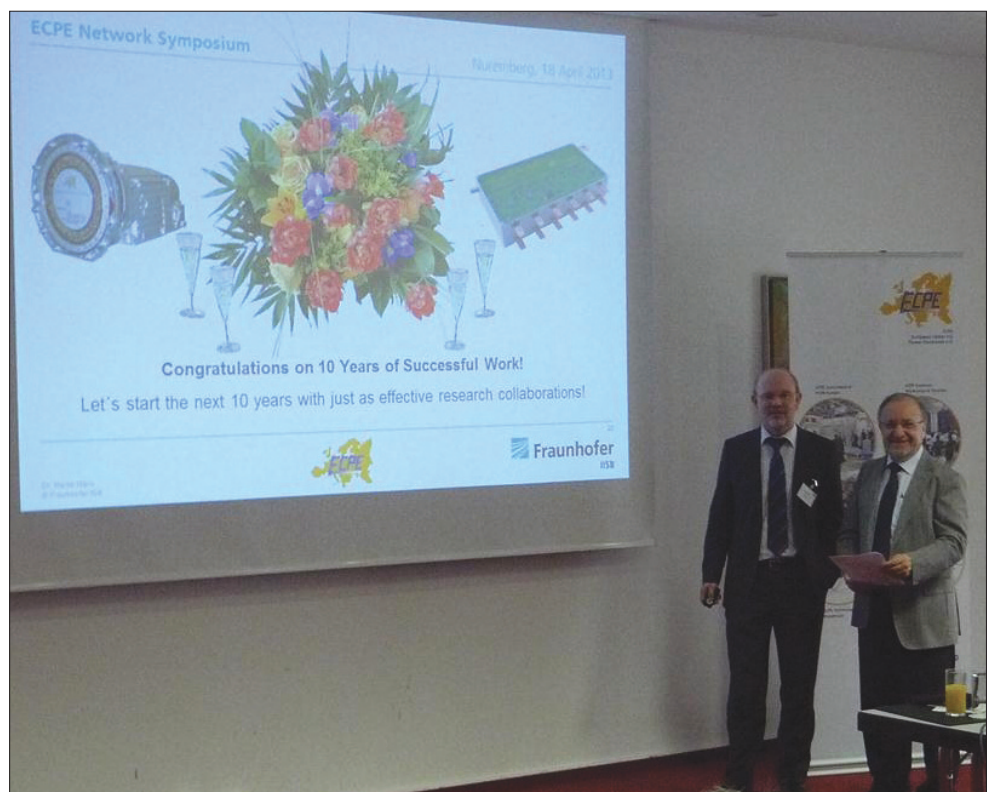
200 kHz and 98.75 percent efficiency utilizing Si switches and SiC diodes".

This was the past, but what is the future? Fraunhofer IISB is working with the latest GaN devices (Panasonic) and has realized an experimental 1.5 kW/600 V boost converter reaching 99 percent efficiency at 100 kHz switching frequency. "But with GaN power semiconductors not all failure mechanisms are well understood, in particular short circuit and avalanche behavior. Also low-inductive packages have to be developed which also have to withstand high temperatures – and the passives have to be improved to catch up with the properties of the power semiconductors. Finally, the long-term reliability issues on the system level have to be studied in more detail".

## over wide bandgap devices

Wide Bandgap Power Semiconductors were more stressed by Nindo Kaminsky from Bremen University/Germany. Due to his research SiC wafers are now micropipe-free and feature reduced dislocations ( $10^4 / \text{cm}^2$ ) with cost at € 10 /  $\text{cm}^2$ . Schottky diodes up to 1700 V are widely used. In switches JFETs and BJTs are used more or less in niche markets. MOSFETs could be the devices of the future. "SiC FETs work well under partial load, at rated load the IGBT performs better. But SiC FETs have much lower switching losses, thus higher switching frequencies are possible reducing the size of passive components",

Fraunhofer's Martin März (left) congratulated ECPE's President Leo Lorenz for ten years successful work in power electronics research





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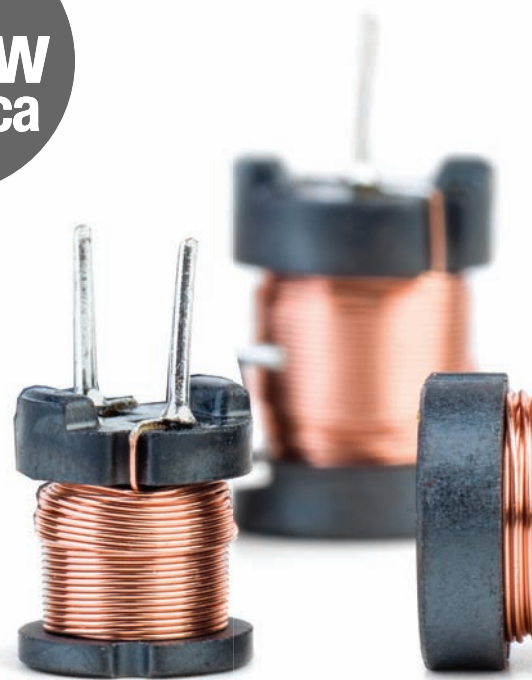
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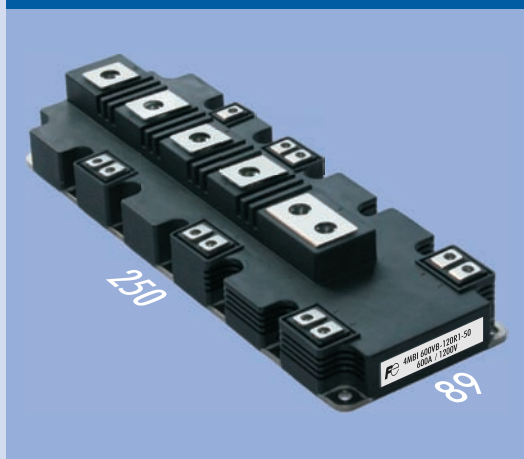
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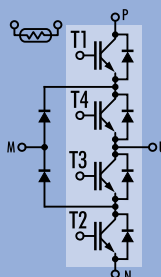
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- ▶ Low internal leakage inductances
- ▶ High performance T-type with RB-IGBT

### 1 phase IGBT modules



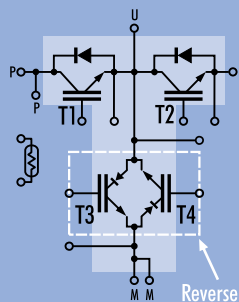
#### I-Type

$I_c$	T1, T2, T3, T4
600A	1200V



#### T-Type

with Reverse-Blocking IGBT



$I_c$	T1 & T2	T3 & T4
450A		
650A	1200V	900V
900A		
450A	1700V	1200V
600A		



## Dawn of a new intelligence for current measurement

Kaminsky said.

Regarding GaN the question of the substrate might be an important factor. Pricing of bulk GaN is € 100 / cm<sup>2</sup>, GaN on SiC € 10 / cm<sup>2</sup>, GaN on Sapphire € 1 / cm<sup>2</sup>, and GaN on Si € 0.1 / cm<sup>2</sup>. "But the latter feature a 116 percent thermal mismatch between substrate and GaN layer, which has to be overcome by a buffer layer. But with GaN on Si it could be possible to make cheaper FETs due to shrinked die size. And with GaN bidirectional switches can be implemented easily", Kaminsky pointed out.

Infineon's head of power semiconductor development Gerhard Miller compared power densities of 150 A devices with SiC JFETs or GaN on SiC being better by a factor of 4 compared to IGBT 4. GaN on Si would have same power density than IGBT 4. Infineon works on normally-off cascoded GaN switches featuring on-resistance better than a factor of 5 compared to CoolMOS C7. "GaN promise up to 650 V performance advantages. Cost can come down due to availability on 150 mm wafers and later 200 mm or even 300 mm wafers", Miller said.

Johann W. Kolar introduced some results of the research on converters at the ETH Zurich/Switzerland. "In a first step we concentrated on power density and reached 10 kW/l with CoolMOS switches and SiC diodes at 500 kHz. We experienced that power density is mainly affected by the passive components". From 2007 onwards the work was focused more on efficiency. With synchronous rectification losses can be reduced, in 2011 his team reached 99.23 % efficiency with a CoolMOS 1.3 kW/l converter. "Designing a converter is a multi-objective optimization also including the power semiconductors", Kolar stated.

Power Electronics at Aalborg University/Denmark has changed its focus towards reliability issues. Thus a Center of Reliable Power Electronics (CORPE) has been established. According to US statistics the solar inverter is by far the most vulnerable part in a solar plant. "Here a LESIT and future lifetime model of a device is of interest, not so much the FIT rate", Prof. Frede Blaabjerg underlined. Reliability could be greatly improved by new joining and interconnect technologies in power modules, i. e. XT technology.

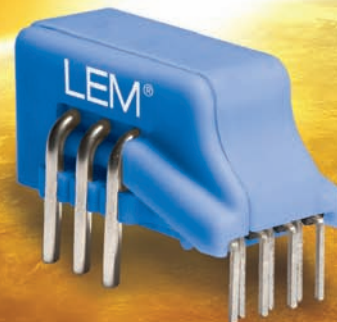
### to MW power

Prof. Rik De Doncker from RWTH Aachen/Germany outlined in his speech "MW Power in Energy Technology" the problems of the German "Energiewende" and associated power transmission. "The around 8000 km of transmission lines to be upgraded or new installed can be avoided by the efficient use of power electronics. Due to many conversion steps in AC transmission 13 % losses will occur, with DC transmission this can be reduced to 5 %. In other words, with DC transmission the transmission capacity can be doubled. Also pricing of copper will increase, but converters will become cheaper due to increased efficiency and power density", he explained. At his institute (EON) a DC/DC converter for up to 20 GW at 99.2 % efficiency for transmission applications has been designed, featuring IGBT power semiconductors. DC transmission will be also beneficial in home applications such as LED lighting, solar power generation or EV charging. "The future could feature 100 percent renewable power supply and thus more power electronics are needed", De Doncker concluded.

Michel Mermet-Guyennet from ALSTOM/France outlined in his talk "Industrial Applications driving Power Electronics" the trend towards SiC in traction drives. "Today we are working on 1700 V, in 2015 on 3300 V and beyond on 6500 V devices in drives. With SiC MOSFETs power losses have been halved and temperature goes up from 150°C to 200°C", he said. The company also realizes the 83 km long transmission line to connect off-shore wind farms with on-shore distribution in Germany for provider Tennet with 320 kV HVDC transmission. Project delivery is scheduled for 2017 at € 1 billion.

Finally an overview on power electronics research activities in Japan, the US and China has been given. As a result – Europe is in a good position.

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# Powering the Future

APEC 2013 in Long Beach/California closed on March 21 with a record of nearly 4,000 delegates (+ 27 %) and 187 exhibitors, making it one of the greatest power electronics conferences and showing the increasing interest in the role of power electronics for energy efficiency. Wide bandgap technologies such as SiC and GaN were of major interest.

The important point energy efficiency was underlined by Dr. Jayant Baliga from North Carolina State University in his Plenary Session opening speech on "The Role of Power Semiconductor Devices in Creating a Sustainable Society". "Western industrialized societies rely on the use of electrical energy for providing a high quality of life for their citizens. The comforts of refrigeration, air-conditioning, and lighting are taken for granted by people. Convenient transportation and communication capabilities are no longer considered a luxury. These benefits are derived by ever increasing demands on our electrical power delivery systems which produces a detrimental environmental impact by causing a high level of carbon footprint. This can be overcome by better efficiency of the power electronic systems, illustrated by the development from early bipolar transistors to MOSFETs and IGBTs. IGBTs in automotive ignition already save 10 % of fuel consumption. The latest generation of promising devices are SiC and GaN, I predicted already in 1980 at GE that SiC will be superior over Silicon, but it has taken a long time to become feasible. SiC has reached this point and the next step will be GaN having a different cost structure, particularly in the combination with a Silicon substrate". "There are very exiting times ahead of us", Baliga concluded.

## The next evolution

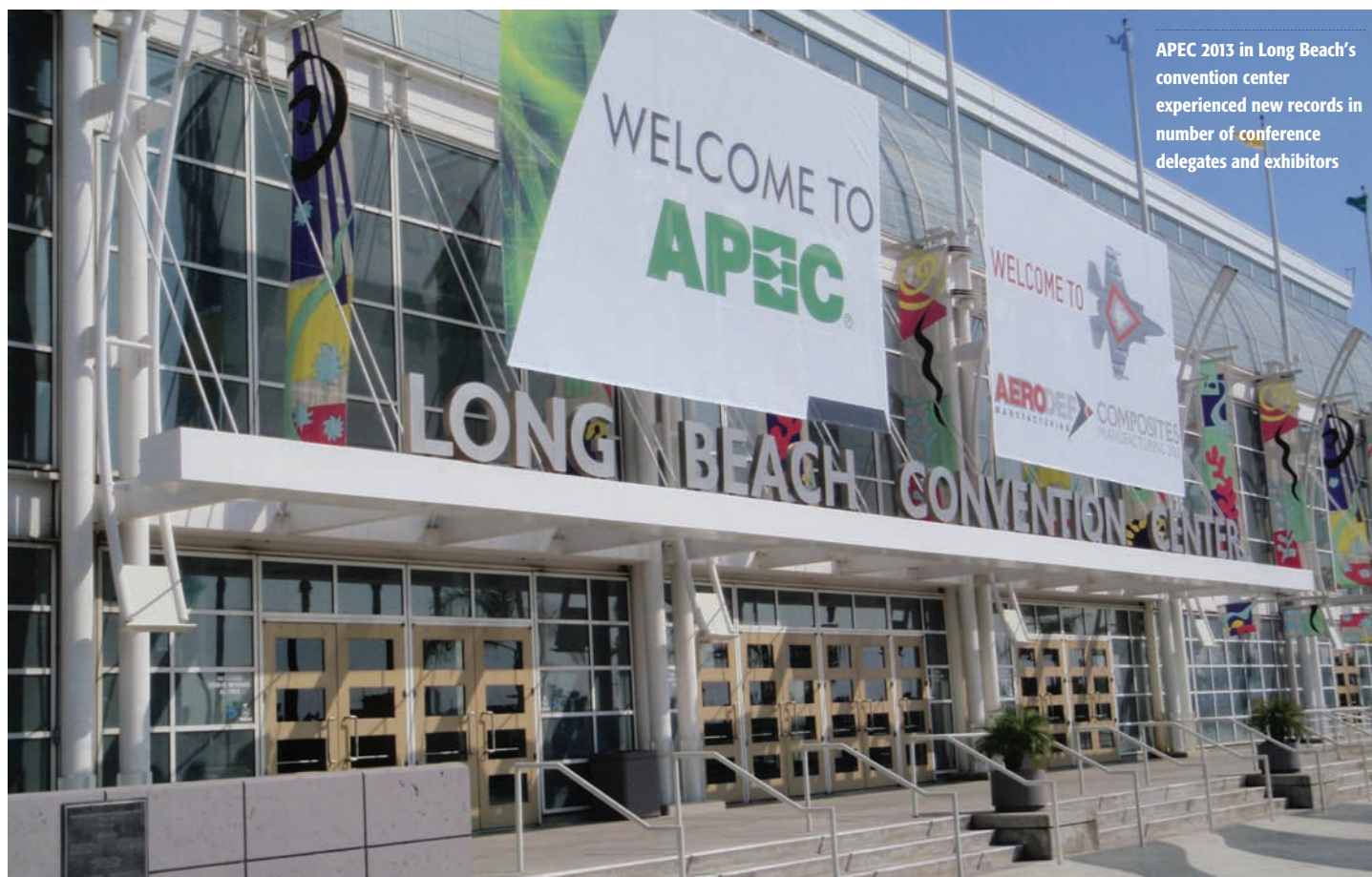
Transphorm's CEO Umesh Mishra said in his plenary talk, that 10 % of electrical energy is lost by conversion steps in the grid. "The progress we make is not by integration as it is in the IC world, but by innovations from the SCR to

the BJT, IGBT, SiC and now GaN. GaN is not competing with SiC, it is competing with Silicon since it is better over Superjunction Si MOSFETs by a factor of 5 and by a factor of 2 better than SiC! That is our Moore's law." As an example on the system advantages of GaN he showed a 3-phase module incorporating diode-free operation at 300 kHz switching frequency for inverters coming with a small integrated filter – as a result of the high switching frequency. Real examples are already on the market, i.e. a drive inverter manufactured by Japanese Yaskawa, or a 4.5 kW PV inverter prototype featuring 98 % efficiency. "High efficiency and high frequency operation shrinks the size of the system, and that is the real advantage of this new material and related devices", Mishra concludes.

Cian Ó Mathúna from Irish Tyndall National Institute also confirmed the increasing role of GaN. "GaN is an enabler for integrated power supplies, challenging is the integration of magnetics".

PSMA (Power Systems Manufacturer Association) presenter Eric Persson has noticed from recent surveys a strong interest in 650 V devices and SiC. "In isolated DC/DC converters GaN adoption is expected by the year 2015".

Vicor's CEO Dr. Patrizio Vinciarelli introduced in his talk "Power Components Come of Age" a newly developed 3D packaging technology named Converter Housing in Package (ChiP) capable of voltages up to 430 V and currents up to 180 A at 98 % efficiency. "Similar to semiconductor wafer processing thin (4.7 mm) ChiP power modules are manufactured on scalable magnetic panels from which the individual devices are sawn out. Applications include AC/DC



APEC 2013 in Long Beach's convention center experienced new records in number of conference delegates and exhibitors





**IGBTs**



**Power Diodes**



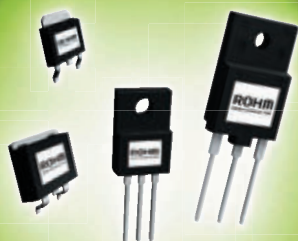
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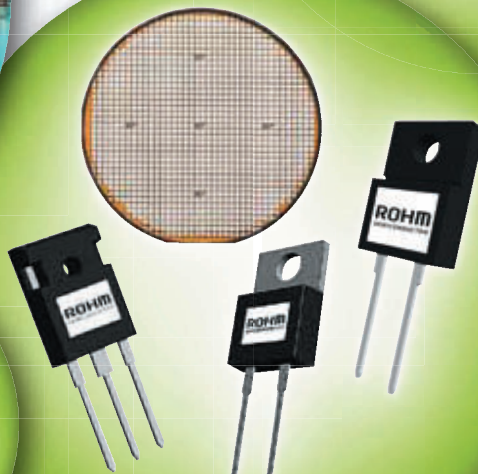
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**SiC Devices**

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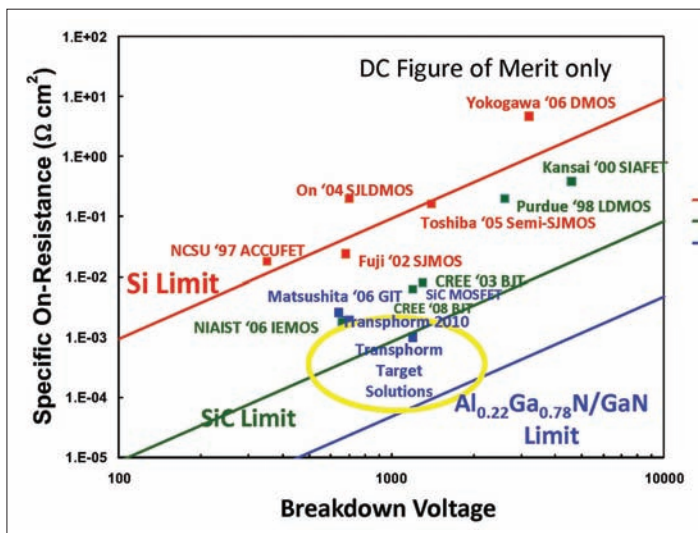
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#### GaN switches giving lowest conduction loss (Source: Transphorm)

with PFC and DC/DC converters, buck/boost regulation, and POL current multiplication. "ChiP technology enables our vision of complete power systems from the AC wall plug to the point of load", he concluded.

Dr. Terry C. Lowe from Los Alamos National Laboratory gave a talk on "Advances in Nanotechnologies for the Power Supply Industry". Nanotechnology can have a huge impact in power transmission and power semiconductors, he said. "Around six percent of power is lost in cable transmission, nanotechnology can reduce this loss significantly i. e. through nanostructured aluminum. For power transistors Graphene can be deposited on SiC featuring ultra-high mobility of carriers and temperatures up to 500°C".

#### SiC and GaN on the move

For several years now we have been hearing about how wide band gap semiconductor devices will revolutionize power electronics as we know it - "its gonna be great.... soon, just wait and see". Silicon Carbide and GaN have co-existed with Silicon as the incumbent "proven & good enough cheap" solution for some time. Silicon devices still have the majority of the market share today, yet, is this about to change? Just as digital power appeared to be a solution in search of problems to solve a few years ago - that technology has been making steady advances into the mainstream market place. Will wide band gap devices follow a similar market adoption curve? Will wide band gap devices deliver the goods and gain market share in mainstream power electronics designs or will it be a technically charming laboratory curiosity relegated to high-end exotic design applications where premium prices can be justified? Will customers be able to buy compelling products across several markets where wide band gap devices enable attractive value to utilize on a broad scale? Is silicon good enough at continuously lowering bargain basement price points to fend off any encroachment? Will Wide band gap break into new and existing applications with demonstrated value even us

"show me" power electronics designers? Will the price-performance ratio of wide band gap devices hit the required metrics, which will allow it to penetrate across multiple cost effective market applications? Will wide band gap take off and penetrate the mainstream or will it be forever relegated to rail guns and "one off" exotic high-end applications? Where is the demonstrable evidence of performance advantages to justify any premiums? Will system level cost savings allow wide utilization by creating value and end customer benefits and eliminating component count and reducing BOM costs? What's the payback period of a design with wide band gap devices? What are the sustainable competitive advantages of wide band gap devices? Will manufacturing cost differences be solved so that pricing can compete with Silicon? What will happen when- accomplished by whom?

To give some answers to this bunch of questions a special Rap Session has been organized featuring

Dr. Michael Briere, Executive Scientific Consultant, ACOO Enterprises for IR; Greg J. Miller, Sr., Vice President - Applications Engineering, Sarda Technologies; Dr. Alex Lidow, CEO, Efficient Power Conversion (EPC); Dr. Primit Parkh, President, Transphorm; Isik C. Kizilyalli, PhD, CTO, Avogy; Dr. John Palmour, CTO, CREE; and Dr. Dan Kinzer, CTO, Fairchild Semiconductor on the panel.

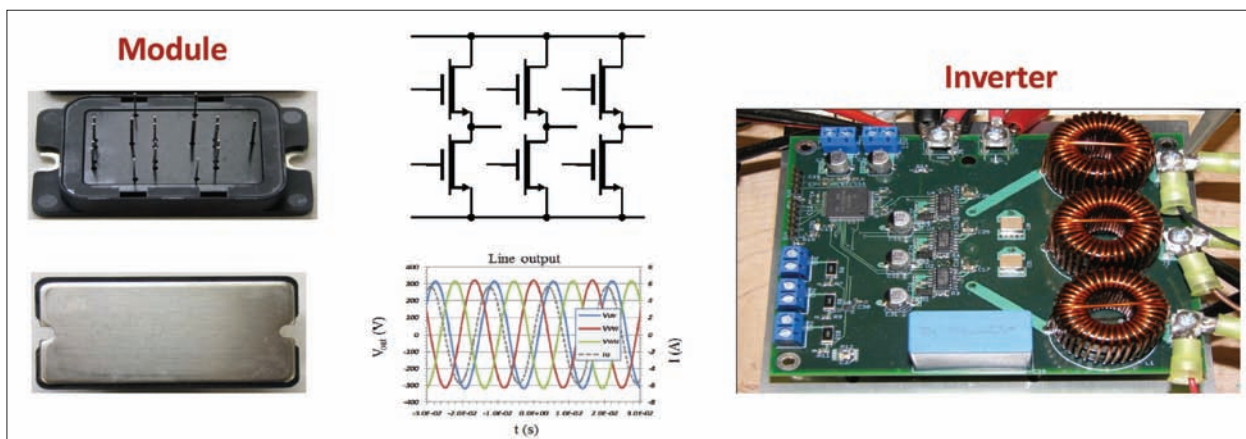
First French market researcher Yole Développement gave an overview on the power device market. "In 2012 the overall market went down to \$11 billion, we expect a recovery in the running year up to 11.5 billion and \$14 billion in 2014. By the year 2018 we expect the market to grow with slightly downs and ups to \$16 billion", said analyst Alexandre Avron.

Regarding wide bandgap power semiconductors, SiC devices are ramping up from \$50 million in 2010 to \$100 million in 2013. By the year 2020 the SiC power market is forecasted to grow gain by a factor of 6 to reach around \$600 million. While PFC has been the major application for SiC and here in particular diodes, since 2012 PV and also light rail traction are gaining more interest. In 2020 PV applications will have a share of around 40 % and traction of around 15 %. PFC will grow slowly in sales to reach \$80 million in 2020, what compares to the traction application market. "The SiC power MOSFETs will contribute significantly to this growth figures", Avron pointed out.

Regarding Power GaN the market will evolve this year to reach \$100 million next year. Yole forecasts \$300 million already by the year 2015 to accelerate up to roughly \$2 billion in 2020. Early adopters will be in IT (power supplies), consumer and lighting, followed by automotive, motor drives (600 V) and battery chargers. IT applications are forecast to have a 50 % share in 2020 and automotive around 30 %. In general more lower power and lower voltage (up to 600 V) but high-efficiency applications such as PV inverters and (H)EV are foreseen in 2013/14/15 for GaN. "We expect the over 600 V GaN market to evolve well beyond the year 2015. SiC will be positioned for middle and high-end solutions at 1200 V and above, and Silicon all the way round for low-end solutions", Avron concluded. But the problem with Silicon compared to SiC or GaN is the charge which has to be removed during switching, in other words the recovery charge which does not exist in SiC and GaN.

What are the barriers for widespread adoption of wide bandgap semiconductors? That was the first question directed to the panel.

Michael Briere on behalf of International Rectifier said "it is always the same





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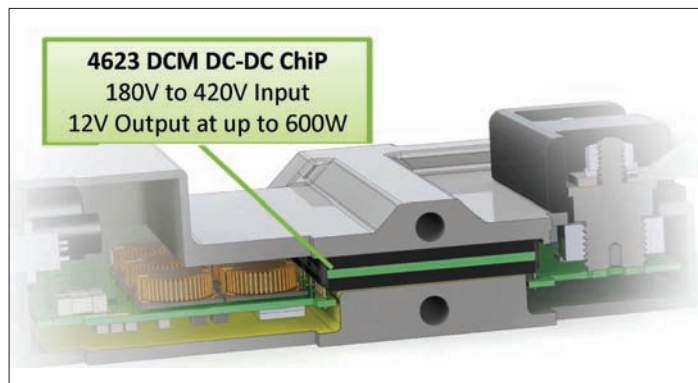
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### Presentations Summary: Components



- Si FETs continue to improve, both low and high voltage
- SiC Schottky diodes now mainstream
- Enhancement-mode GaN on Si commercialized for 3 years
- SiC MOSFETs look promising at 1,200V and up
- GaN on Si cascode FETs (600 V) entering commercialization
- 1,200 V SiC BJTs may begin to encroach on IGBT territory
- Nanocrystalline magnetic core materials better than ferrite at >100 kHz, high flux



#### Results of the PSMA Power Technology Roadmap 2013 for components (Source: PSMA)

with new technologies or in other words performance to cost. Adoption requires history and time, first you have to serve the consumer markets and then moving on to industrial and perhaps hirel". "When we converted the Bipolars to MOSFETs we found three major barriers we also face with compound semiconductors today – lower price, enough reliability, and easy to use. We have to get it cheaper than the MOSFET and that will take 2 or 3 years time", Alex Lidow commented. "GaN has to fulfill application demands which can not be fulfilled otherwise. Cost and reliability are also important, but performance and ease of use are main issues for our customers", added Primit Parkh. "We are growing GaN on a GaN substrate what differentiates us from other vendors. This so-called True-GaN approach can outperform Silicon Carbide at 600 V and higher", Isik C. Kizilyalli expressed. "With the introduction of our second generation SiC MOSFET we have halved the cost, the 1200 V /20 A part sells for \$16. We offer 4 times the power for twice the cost of GaN, so SiC is not that expensive. And the third generation processed on 6-inch wafers will be cheaper as well. But the big challenge today and in future is proper packaging to handle these high power densities at low inductance levels – and this is common to SiC and GaN", John Palmour explained. "The SiC BJT is the most efficient switch at 1200 V, that's why we acquired this technology recently from TranSiC. This vertical device has no channel resistance. Lateral devices simply does not approach the theoretical limits of vertical structures, where the currents flows through the device. Since cost is an important factor and since we rely on SiC wafer vendors these have to reduce defect density and price. System performance and cost is more important than unit cost, but with time SiC cost will decrease. And improved packaging to deal with higher frequencies and temperatures is also a major issue", Dan Kinzer confirmed.

To the question regarding GaN getting to 1200 V Primit Parkh commented that there is no physical barrier. We choose first to focus on 600 V because it was sufficiently differentiated to Silicon in performance and giving a system advantage to our customers. We definitely will commercialize 1200 V devices in the future". "The main challenge of raising the voltage are the vertical fields across the GaN epitaxial layer which means the material has to be thicker and

#### Liquid cooled automotive ChiP power module

secondly a field on the surface can reduce reliability. I do believe that 1200 V is possible but it is not trivial to achieve", Michael Briere added. "With vertical structures, GaN on GaN, the issue of dielectric fields is not a major problem. We are making 600 and 1200 V devices and 1700 V are in qualification. We are not afraid of high voltages and high electric fields", Isik C. Kizilyalli pointed out. But the disadvantage of this technology are small (2-inch wafers) at relatively high cost. "The advantage of using bulk GaN compared to SiC is by a factor of 2 and that is why we did not chose this way", John Palmour confirmed.

To the question of the pros and cons for the SiC MOSFET, JFET and BJT Cree's John Palmour said: "The SiC BJT is fast and acts more or less than a major carrier device. Though it is a current driven device in terms of switching performance it looks just like a FET. But one problem is gain degradation over time". "The SiC BJT has no internal body diode so it does not to have an external body diode and properly driven it switches faster than a FET", Fairchild's Dan Kinzer added. "But the gain degradation is due to not dislocation-free SiC wafers and here the SiC wafer vendors have to



**Panelist Micheal Briere envisions new power topologies with GaN**



**Vicor's new ChiP power components are sawn out of scalable magnetic panels**



**Panelist Alex Lidow sells GaN devices in wafer form and this cuts half the price**





**Panelist Primit Parkh sees no barriers for future 1200 V GaN devices**



**Panelist John Palmour offers 4 times the power for twice the cost of GaN**



**Panelist Dan Kinzer claims that gain degradation in SiC BJTs is due to not dislocation-free SiC wafers**

improve the starting material!"

Of course the question of appropriate packaging for SiC and GaN was issued to the podium. "Due to fast switching you have to have low inductance and in order to get the heat out double sided cooling is very important", Michael Briere pointed out. "Package and die go hand in hand together", Transphorm's Primit Parkh stated. "In order to have low EMI at fast switching we made a simple change – instead of having Gate/Drain/Source pinning we do Gate/Source/Drain what reduces EMI. Alternatively we can connect either the Source or the Drain to the Tap what we call Quiet Tap. Also low-cost low-inductance modules are needed. "Integration within the package is key, perhaps with certain passive components", Dan Kinzer added. "We are getting

rid of packaging since GaN on Si is self-isolating up to 200 V. We sell the devices in wafer form and this cuts half the price", EPC's Alex Lidow stated.

To the question of new topologies Greg J. Miller said that wide bandgap devices open the way to 50 MHz switching and in a second step to bidirectional switches. But he works with low voltage (20 V) GaAs material. "First you have to drop the new devices into existing topologies. But GaN allows the integration of devices and thus I can envision hundreds of power transistors on an IC capable of sine-wave manipulation where each of the switches work on part of the packet instead of today's square waves. Thus new power topologies will emerge because you never had power devices you are going to have", so Micheal Briere's outlook.

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# APEC's Power Products and Services

The 187 APEC exhibitors presented their latest products and services from March 18 – 20 in Long Beach. Among them were the international well known names as well as some smaller start-ups particularly in wide bandgap semiconductors reflecting the growing market opportunities in SiC and GaN.



The some 4000 APEC conference delegates showed a lot of interest on the 187 exhibitor's offerings

Alpha and Omega Semiconductor ([www.aosmd.com](http://www.aosmd.com)) introduced the AOTF11C60 and AOTF20C60, 600 V MOSFETs with AlphaMOS™ II technology. The AlphaMOS II (a patent pending proprietary structure and process) combines planar-like robustness and controlled switching characteristics with the low on-resistance performance of Superjunction type devices. The AOTF11C60 and AOTF20C60 are suited for high-voltage applications such as server, telecom and networking power supplies, UPS, solar inverters, industrial motor control systems, and LED lighting. The devices offer improvement in UIS capability over Superjunction and has been optimized for low noise operation and high efficiency by fine tuning the switching parameters. Low  $R_{DS(ON)}$  of 0.4  $\Omega$  resp. 0.25  $\Omega$  allow for designs that require high efficiency.

AVX Corporation ([www.avx.com](http://www.avx.com)) introduced a new line of polypropylene dielectric DC-link film capacitors. Designated the FB Series, the 2-leded capacitors feature a voltage rating of 550-1200 V, a capacitance range from 0.68-75  $\mu\text{F}$ , are rated for use from -40 to +100°C, and are available in 14 case sizes. Applications include DC power supplies and inverters for solar power, electric drive, and industrial power systems. The new FB Series DC link capacitors combine low loss film technology with the self-healing properties of the dielectric to ensure long lifetimes and low thermal losses in power applications.

CREE ([www.cree.com/power](http://www.cree.com/power)) announced its second generation 1200 V/50 A SiC MOSFET enabling systems to have higher efficiency and smaller size at cost parity with Silicon-based solutions. These new 1200V MOSFETs deliver leading power density and switching efficiency at half the cost per Amp of Cree's first generation MOSFETs. The product range has been extended to

include a much larger 25 m $\Omega$  die aimed at the higher power module market for power levels above 30 kW. The 80 m $\Omega$  device is intended as a lower cost, higher performance upgrade to the first generation MOSFET. Bare dies are also available intended as a 50 A building block for high power modules. "With our new MOSFET platform, we already have design wins in multiple segments," said Cengiz Balkas, vice president and general manager, Cree Power and RF.

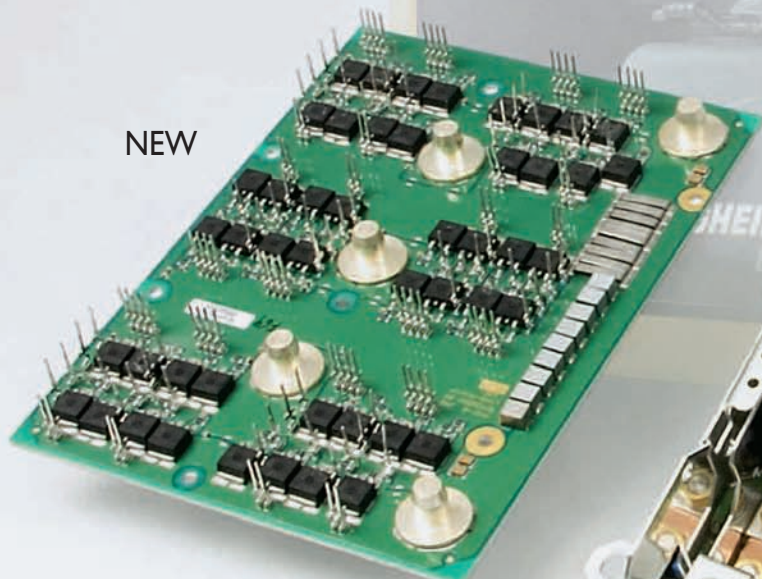


AVX's new DC-link film capacitors



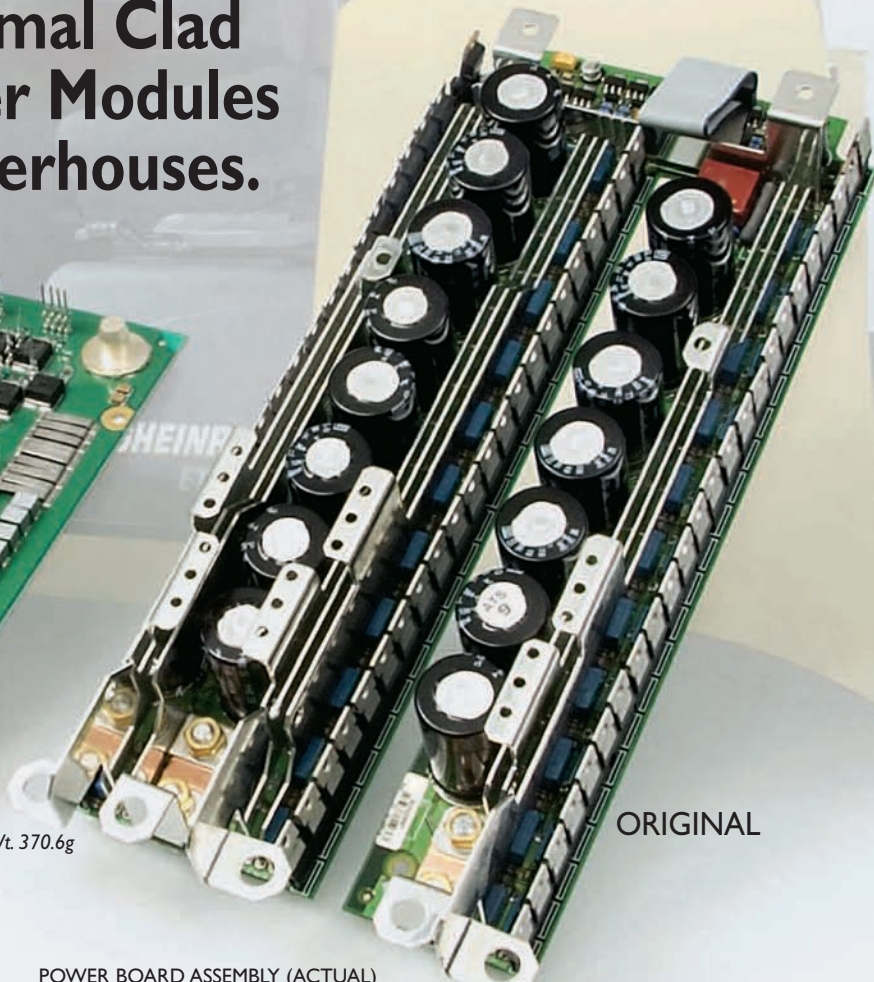
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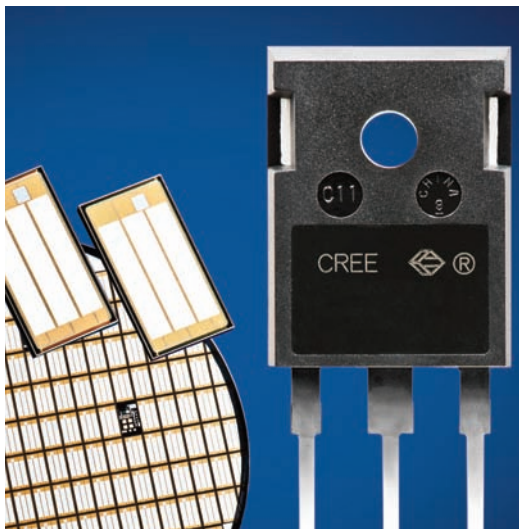
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**Cree's second generation 1200 V/50 A SiC MOSFETs**

"Due to the rapid acceptance of this second generation of SiC MOSFETs, we are shipping pre-production volumes to several customers ahead of schedule and we are ramping volume production in-line with customer demand".

GaN Systems ([www.gansystems.com](http://www.gansystems.com)) and Arkansas Power Electronics International (APEI) demonstrated a GaN power switch based DC/DC boost converter with 1 MHz switching capability and over 98.5 % efficiency at 5 kW output power. Testing demonstrated turn-on and turn-off transitions of only 8.25 ns and 3.72 ns, respectively. "The ultra-high switching frequency that Gallium Nitride enables is one key to reducing the size and weight of power



**GaN Systems' Geoff Haynes presents a first GaN-based 5 kW DC/DC boost converter with 1 MHz switching frequency**

electronic systems", said Business Development Manager Geoff Haynes. "These test results demonstrate first-hand the system-level benefits enabled by this new devices". He announced also that production of GaN on SiC devices would be carried out using RFMD's GaN on SiC foundry processes. RF Micro Devices based in Greensboro/N.C ([www.RFMD.com](http://www.RFMD.com)) is a global leader in the design and manufacture of high-performance radio frequency components and compound semiconductor technologies. Initially designed for SiC substrates the GaN process has been moved also to Silicon substrates.

Infineon ([www.infineon.com/rapiddiodes](http://www.infineon.com/rapiddiodes)) introduced the fast recovery 650V Rapid 1 and Rapid 2 Silicon diode families combining ultrathin wafer technology with unique cell design. The new Rapid diode families complement the 600 V and 650 V diode portfolio by filling the gap between SiC and emitter-controlled diodes to address the ultrafast power Silicon diode markets for switching frequencies between 18 and 100 kHz. The Rapid 1 diode family has a 1.35 V temperature-stable forward voltage to ensure low conduction losses and provide soft recovery to keep EMI emissions low. The devices are suited for PFC topologies which are switching between 18 and 40 kHz. The Rapid 2 diode family is designed for applications switching between 40 and 100 kHz for PFC stages in servers, telecom rectifiers, TV and laptop power adapters, and welding machines particularly in conjunction with

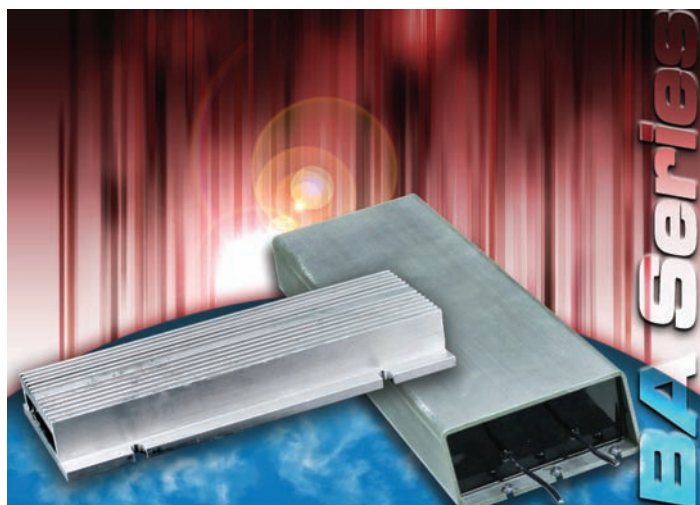


**Infineon's new fast recovery 650V Rapid 1 and Rapid 2 Silicon diode**

Infineon's CoolMOS™ MOSFETs and high-speed IGBTs.

Intersil's new ZL8101 ([www.intersil.com/products/ZL8101](http://www.intersil.com/products/ZL8101)) is an adaptive digital DC/DC PWM controller with auto compensation that provides a single phase solution with output currents up to 50 A. Designed to work with an external driver and with DrMOS solutions, it can be used in parallel for current sharing between multiple ZL8101 devices. It also can be deployed as a flexible building block for 12 V and 5 V down conversion. The ZL8101 uses a dedicated, optimized state machine for generating precise PWM pulses and a proprietary MCU for set-up and optimization. Additionally the new PowerNavigator GUI offers a single software platform for all PMBus-enabled Power Management products at Intersil, meeting user requirements with complete design editing from design start to hardware implementation. The software allows simple configuration and monitoring of multiple PMBus-based products using a PC with a USB interface. It can monitor large systems through dashboard views, allows for easy debugging during prototyping, and provides comprehensive visualizations and power-centric intelligence such as sequencing and fault management.

Ohmite Manufacturing ([www.ohmite.com](http://www.ohmite.com)) showcased its BA Series of wirewound resistors, custom thick film products, and new active cooling heatsinks. The BA Series are intended for dynamic braking, motor starting, and power control applications. Other uses include inverter and power conversion applications. The heatsinkable BA Series resistors feature power ratings of 500-1000 W and resistance values from 0.5  $\Omega$  to 18 k $\Omega$ . The company also highlighted its capabilities in designing custom thick film solutions. During the

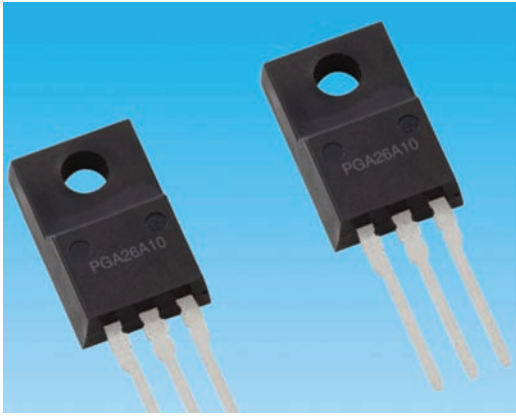


**Ohmite's high-power resistors for dynamic braking applications**

a standard, thick film product consisting of a deposited film on an alumina substrate is used. Its form, fit, and function is customized to fit a customer's specific high power or high voltage application. Also two new active cooling heat sinks were on display. Modular C Series heat sink accepts a 40 mm fan, which will make it easy to modify for any high power environment.

Panasonic's (<http://panasonic.net>) 600 V/15 A normally-off Gate Injection Transistors (GITs) are processed on 6-inch Si substrates via





**Panasonic's new  
GaN/GIT  
normally-off FETs**

proprietary technologies for the epitaxial growth of GaN by metal organic chemical vapor deposition (MOCVD). The p-type gate of the GIT greatly helps to reduce the on-state resistance taking advantages of the conductivity modulation by the hole injection from it. The GIT exhibits low  $R_{on} \times Q_g$  of 715 m $\Omega$ nC which is one thirteenth lower than that by the state-of-the-art Si MOS transistors. Panasonic also demonstrate 1 MHz operation of resonant LLC DC/DC converters at high efficiency over 96%.

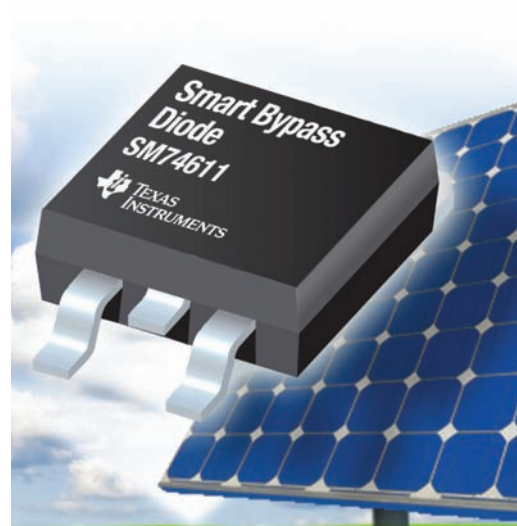
STMicroelectronics ([www.st.com/web/catalog/sense\\_power/FM100/CL824](http://www.st.com/web/catalog/sense_power/FM100/CL824)) announced special fast-acting variants of its advanced 600 V/18 A/190 m $\Omega$  Superjunction power MOSFETs with its MDmesh power MOSFETs, and now delivers even better performance with its latest MDmesh II Plus™ Low  $Q_g$  family. These devices feature a reduced internal charge for high efficiency when switching as well as when conducting, saving even more energy in resonant-type power supplies. Until now, Superjunction transistors have been used most effectively in hard-switching topologies, where the device is made to switch even while the current and voltage remain high. In a resonant power supply two inductors and a capacitor (LLC converter) ensure the transistor is switched at zero voltage to smooth the flow of energy in the system and help increase efficiency. The new device family is also highly



**ST's MDmesh II Plus 600  
V Superjunction MOSFET**

resistant to the effects of large and sudden changes in applied voltage (high dv/dt ruggedness).

Texas Instruments ([www.ti.com/solar-pr](http://www.ti.com/solar-pr)) introduced a smart bypass diode in a standard surface-mount package with 15 A current handling capability. In a typical application, each SM74611 lowers power dissipation by 80 % and reduces the operating temperature inside the junction box by 50°C when compared with a similar box using three conventional Schottky diodes. When a PV solar panel is shaded, the SM74611 provides an alternate low-resistance path for string current to prevent hot spots that can damage the panel. The SM74611 protects the panel and improves PV solar panel reliability by boosting efficiency, and the reduced thermal dissipation enables more compact junction boxes with smaller heat-sinks. The SM74611 joins TI's family of solar products that include the UCD3138 digital power controller for solar



**TI's new PV  
bypass diode  
lowers power  
dissipation by 80  
% in the junction  
box**

micro-inverters, SM72441 maximum power point tracking controller and SM72295 full bridge driver.

Toshiba ([www.toshiba-components.com](http://www.toshiba-components.com)) introduced a new line of 600 V DTMOS IV SJ MOSFETs rated at 16/31/39 A and on-resistances of 0.23/0.099/0.074  $\Omega$  respectively. The company also announced that it will manufacture Schottky Barrier Diodes (SBD) as the first of its new line-up of SiC products. The SBD is suited for applications that include power conditioners for photovoltaic power generation system. SBDs can also act as replacements for silicon diodes in switching power supplies, where they are

Wide range of power semiconductor solutions

## SiC Devices

650V SiC Schottky Diodes

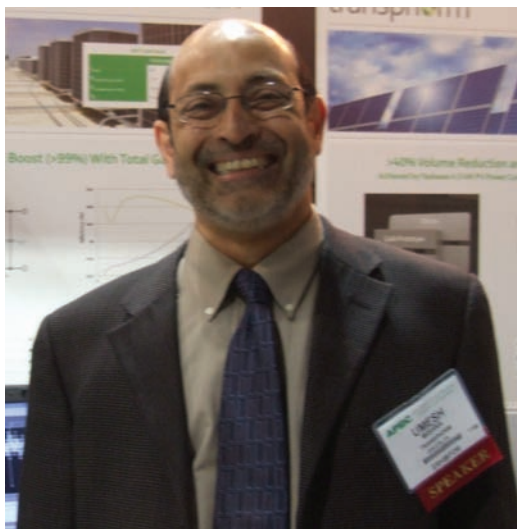
### Features

- 650V rating
  - ~ 1,200V devices are under planning
- 12A product (TRS12E65C) in production soon
- 6A and 8A products samples available
  - ~ 10A products available soon
- Improved V<sub>f</sub>-I<sub>f</sub> trade-off
- TO-220 (2 pin) package available
  - ~ Package variation will be expanded
- Suitable for PFC circuit for AC-DC converters

#### Toshiba enters the SiC market with 650 V diodes

50% more efficient. Toshiba aims to secure a 30 % SiC market share in 2020 by strengthening its product line-up, starting with the launch of the new SBD. According to Business Development Manager Norio Nakashima SiC MOSFETs are planned in the near future.

Transphorm ([www.transphormusa.com](http://www.transphormusa.com)) introduced the JEDEC-qualified 600 V Total GaN family on Silicon transistors and diodes. "This marks a significant milestone in the broad adoption of GaN-based power electronics in power supplies and adapters, PV inverters for solar panels, motor drives, as well as power conversion for electric vehicles", stated CEO Umesh Mishra. "Our GaN high electron mobility transistor combines low switching and conduction losses to reduce energy loss by 50 % compared to conventional Silicon-based power conversion designs". The TO-220-packaged TPH3006PS GaN transistor features low on-state resistance of 150 m $\Omega$ , low reverse-recovery charge of 54 nC and thus high-frequency switching capability. Also available in industry-standard TO-220 packages, the TPS3410PK and TPS3411PK GaN diodes offer 6 A and 4 A operating currents, respectively, with a forward voltage of 1.3 V. In addition, three application kits — PFC (TDP5400E1A7), Daughter Board (TDP5500E0A) and Motor Drive (TDMC4000E0I) — are available for rapidly benchmarking the in-circuit performance. The TPH3006PS HEMT device



**Transphorm's CEO Umesh Mishra introduced the JEDEC-qualified 600 V Total GaNTM family**

University and member of USCI's board. At PCIM 2013 the company will present new designs in 100 V normally-off JFETs and GTOs.

Vishay ([www.vishay.com](http://www.vishay.com)) announced various devices such as SiR872ADP, an 18 mΩ, 150 V ThunderFET® n-channel MOSFET in the PowerPAK® SO-8; and 100 V ThunderFET® devices in 2 mm by 2 mm and 1.6 mm by 1.6 mm PowerPAK packages with on-resistance under 100 mΩ and 200 mΩ, respectively. The SiR872ADP's low on-resistance enables more efficient operation in DC/DC converters while the smaller devices save space in power bricks. Also on view were 600 V and 650 V E Series Super Junction MOSFETs based on Vishay's next generation technology. The MOSFETs offer 30 % lower specific on-resistance and improved gate charge in TO-220 FullPAK, TO-247AC/AD, D2PAK, DPAK, IPAK, and PowerPAK 8x8 packages.

AS



**According to Guy Moxey United Silicon Carbide focuses on high-voltage SiC devices**

is available at \$5.89 in 1,000 quantities, the TPS3410PK and TPS3411PK diodes are priced at \$2.06 and \$1.38, respectively.

United Silicon Carbide ([www.unitedsic.com](http://www.unitedsic.com)), a spin-off of Princeton University, took the chance to present its SiC foundry service and products at APEC. Its New Jersey based manufacturing facility is fully equipped with a Class 100 clean room for design, fabrication, testing, and packaging of electronic and optoelectronic devices. "USCI possesses the necessary SiC packaging and testing expertise for delivery of our fabricated die in hermetically sealed packages to customers", Product Marketing Director Guy Moxey pointed out. The company offers SiC JFETs and BJTs, MOSFETs up to 1700 V as well as SiC GTOs up to 6.5 kV. Derek Lidow, former IR CEO and founder of iSuppli, today is Visiting Professor in Entrepreneurship at Princeton

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EUROPE



International Exhibition and Conference  
for Power Electronics, Intelligent Motion,  
Renewable Energy and Energy Management  
Nuremberg, 14 – 16 May 2013

# More Power for a Greener World

After APEC is before PCIM. From 14 - 16 May 2013 all the major companies in the field of power electronics will be presenting their latest innovations in Nuremberg. The future application markets renewable energy, smart grid, energy efficiency and consumer electronics sectors will play a major role. Power electronics are of considerable importance as they are a key technology for these and other many fields of application. PCIM 2012 closed with 263 exhibitors, 6.874 visitors and 744 conference delegates, more a expected for this year's event.

The exhibition therefore will be held in halls 7 and 9 for the first time, to take into account the growing demand for space from existing exhibitors as well as an increasing number of new ones. In the last three years alone, the exhibition area of the PCIM Europe has grown by 30 % and will reach 18,500 square meters this year. Also new is the second Forum, which will link together cross-sector topic areas and offer panel discussions, roundtables, short seminars and other highlights.

In addition, this is where vendor presentations by exhibitors will take place as in past years.

## **Comprehensive seminar and tutorial program**

Six seminars and ten tutorials will offer delegates on the two days prior to the conference the opportunity to educate themselves about particular power electronics topics. These will be led by specially invited internationally renowned industry experts who will be able to speak on the issues in their own specialist area.

Seminars on the Sunday, May 12 include subjects such as "Loop compensation of Voltage Mode and Current Mode DC/DC Converters", "Basics of Electromagnetic Compatibility (EMC) of Power Systems", "SMPS Topology Selection", "Current Mode Control", "New Developments in Power-Factor Correction", and "Wireless Power Technologies".

Tutorials on the Monday (May 13) will cover "Trends in Soft Switching Technologies",

"Controlling DC-DC Converters for Fast Dynamic Response", "Electromagnetic Design of High Frequency Converters and Drives", "High Performance Control of Three Phase Inverters", "High Frequency Magnetics Design", "Understanding batteries for optimized power electronics development - Battery designs, charging requirements, state-of-charge monitoring, lifetime", "Power Electronics for Renewable Energy Systems", "IGBT Gate Drive Technologies", "Design approaches to SMPS Control", and "Reliability of IGBT Power Modules".

## **From power devices to power systems**

Also the PCIM Conference targets the development of power electronics with regard to leading edge technologies such as solar and wind power, e-mobility and new materials. Delegates can expect a total of more than 230 presentations and poster displays in over 40 sessions, providing a comprehensive overview of the most up-to-date power electronics topics. Experts from leading



Again it's time for  
PCIM in Nuremberg  
from May 12-16

companies as well as representatives from colleges and research institutes will be revealing their latest findings. Three Young Engineer Awards and the Best Paper Award, the latter sponsored by Power Electronics Europe, will be handed over at the conference opening ceremony.

Highlights at the beginning of each conference day will be the three keynote speeches on: "HVDC – State of the art and future trends", "New Generation of Traction Drives based on SiC Power Components" and "High-density Fast-transient Voltage Regulator Module", led speakers from Siemens, ALSTOM and Virginia Polytechnic Institute and State University.

The first keynote will be given by Jörg Dorn, Siemens AG. The growing share of power generation from renewable energy sources leads to continuative challenges in the field of electric power transmission. The load centers are often far away from the location of generation and very long transmission distances have to be considered.

Requirements, such as low environmental impacts, low transmission losses and high availability have to be fulfilled. In many cases, HVDC (High Voltage Direct Current) transmission is the only technical and economical solution to cope with these challenges. Line-commuted converter technology was the unique solution for many decades and is today focusing on bulk power transmission up to 8 GW. Since the introduction IGBT based modular multilevel converters (MMC) into HVDC transmission, this VSC technology is becoming significantly important. It combines low losses, excellent controllability and failure handling with the capability to build large multi-terminal systems or even HVDC grids in the future. The presentation gives an overview of the state of the art technology and some insights of the applied power electronics. An outlook is given, which role HVDC will play in the field of renewable power generation and associated transmission networks in the future.

The second keynote by Michel Mermet-Guyennet, ALSTOM/F covers Transportation. Power component technologies evolve very fast. In 1995, ALSTOM Transport introduced the first traction drive using IGBT (Insulated Gate Power Component) power components in tramway application; since this date, all the ALSTOM traction



The conference serves as a platform for exchange of expertise and latest technology

drives use IGBT components with blocking voltage up to 6,5 kV. This is the case of the new AGV train which is the last generation of very high speed train with distributed power among all the cars and permanent magnet motors. In 2008, a new generation of power component based on SiC (Silicon Carbide) has reached industrial maturity and is available up to 1700 V blocking voltage today. These components offers much better characteristics than IGBTs. These components will revolutionize the approach of traction to take the full advantage of their characteristics, leading to a much better integration and efficiency. A prospective view will be presented. However, several aspects are still open and need in depth investigations before starting a commercial implementation.

The third keynote by Qiang Li, Virginia Polytechnic Institute, will address computing. Over a period of 15 years, the Intel processor has evolved from a relatively low voltage of 2 V and low current of 10 A to a still lower voltage of less than 1 V and an increased consumption of more than 100 A. Current generation of Intel's processor also requires a fast dynamic response in order to implement the sleep/power mode of operation. This mode is necessary to conserve energy and extend operation time for battery-powered

equipment. This has been possible because of multi-phase voltage regulator (VR) technology that powers almost every Intel processor today. At the heart of this success story, the VR technology is a specialized distributed power system that provides precisely regulated output with fast dynamic response so that energy can be transferred as fast as possible to the microprocessor. This presentation will give a general overview of multi-phase VR, and address some advanced technologies, such as integrated power device, coupled inductor, two-stage architecture and constant-on control. These technologies either have been used already or are poised to be adopted by industry to enable high-efficiency high-density fast-transient VR design. Several emerging technologies, such as Gallium Nitride (GaN) device, magnetic component integration, and high bandwidth control with auto-tuning function will also be discussed to show that the power density and transient speed of future VR could be further improved to another level.

Six special sessions will highlight what the new drivers for demanding applications are likely to be.

#### Special session on gallium nitride

In particular PEE's Special Session "Power GaN for Highly Efficient Converters" on Thursday (May 16,

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As usual the PCIM exhibition will gain a lot of interest by qualified visitors

2.00 pm) in Room Brüssel 1 will complement the third keynote and other more technological oriented sessions with device- and application-oriented details on this new power semiconductors. Market researcher Yole Développement expects turnover in excess of \$100 million in 2014 followed by an exponential growth in the years to come.

Though Japanese semiconductor manufacturers such as Fujitsu and Panasonic have recently announced they will enter the GaN market, the major players having devices ready come from the Americas. Thus this Special Session will feature Alex Lidow, CEO Efficient Power Conversion (EPC) El Segundo/USA; Umesh Mishra, CEO Transphorm Goleta/USA; Girvan Patterson, CEO GaN Systems Ottawa/Canada; and Michael Briere, ACOO Enterprises Scottsdale/Arizona for International Rectifier, El Segundo/USA.

Efficient Power Conversion Corporation (EPC) has been in production with enhancement mode GaN-on-Silicon power transistors (eGaN FETs) for over three years. Much progress has been made improving device performance and reliability. There have also been several new power management applications that have emerged. Two of these applications, RF Envelope Tracking and high frequency Wireless Power Transmission are beyond the fundamental capability for the aging power MOSFET due to the requirements of high voltage, high power, and high frequency. As a result, these are early growth markets for GaN on Silicon devices. eGaN FETs have also made

inroads in several other applications that Alex Lidow will discuss along with the latest in device technology and future direction for both discrete and integrated circuits made in GaN.

During the past decade improvements in semiconductors have lead the way to more efficient systems, but further advances in silicon devices have come close to a wall limited by inherent semiconductor properties. Luckily devices based on GaN have emerged and now matured enough to demonstrate higher efficiency in inverter circuits for both solar and motor drive systems. The presentation given by Umesh Mishra investigates how GaN is making such rapid performance progress and uses test results to illustrate what is now possible using GaN compared to recent SiC transistor performance. It then predicts future improvements that will continue to make GaN a more attractive alternative to either Si or SiC for high efficiency systems.

GaN transistor switching speeds of a few nanoseconds and two orders of magnitude improvement in specific on-resistance over Silicon devices improves volumetric and conversion efficiency in any power systems and has particular relevance to solar and wind inverters. GaN Systems novel switch topology maximizes these advantages whilst reducing cost of manufacture. To derive the maximum benefit from these devices requires new circuit design and construction techniques. GaN Systems is investing heavily to accelerate the adoption of the new technology by designing CMOS integrated driver solutions onto

which the GaN die is mounted directly in a stacked chip assembly combining the switch, its driver, sensors and customized interface circuitry. In solar and wind inverter applications the high voltage operation, embedded galvanic isolation and high speed operation of these devices offer the prospect of higher switching speeds with improved conversion efficiency, lower component count, smaller size and reduced conversion loss, as Girvan Patterson will explain.

It has been well documented that the advent of high voltage GaN based power devices provides unprecedented opportunities to reduce both conduction and switching losses in a wide variety of power conversion circuits. In The final presentation experimental results for the use of GaN based power devices in highly efficient high frequency power circuits such as AC/DC power supplies, DC/DC boost and DC/AC motor drive inverters are presented by Michael Briere. The current status of the development and current performance of the required 600 V rated GaN on Si based devices at International Rectifier are presented, including the development of crack free AlxGayN alloy based epitaxy on standard thickness 150 and 200 mm Si substrates. Results of long term reliability studies of more than 5000 hrs are presented, as well as results for device robustness under standard application conditions.

After this paper a short podium discussion between all speakers and the auditorium is planned. PEE would be happy to welcome you!

AS

# Thermal Design: Incorporating EDA and MDA Design Flows

The main source of heat in electronic equipment is their (power) semiconductor chips, and this presents a challenge in designing cooling mechanisms. Overheating causes the chips and passive devices such as electrolytic capacitors to prematurely fail. The higher the chip temperature, the earlier and more certain the failure. As functionality has increased, the associated heat dissipation has escalated to the extent that it is recognized as a potential limitation on the pace of electronics development. Appropriate cooling strategies are needed to prevent overheating and failure of critical components. General-purpose CFD software is far from ideal in satisfying these requirements, which is why special-purpose software, such as Mentor Graphics FloTHERM XT, optimized for electronics thermal applications, with industry-specific input and control, was developed.

In electronics, the complete design cycle from concept to first customer ship is much shorter than in traditional manufacturing industries - in some sectors, now as short as nine months. Cooling design and simulation applications have to be quick, reliable, and integrated into a fast-moving, complex design process. The people responsible are not experts in CFD or fluid dynamics, and they do not want to spend a lot of time learning detailed CFD concepts, or running potentially time-consuming operations such as sophisticated grid generation.

Mechanical engineers are responsible for all aspects of the physical design of the equipment, that is, everything beyond the electronics design, which typically culminates in the printed circuit board (PCB) layout. They are responsible for the enclosure, appropriate location of the PCBs and

other components, and for ensuring structural integrity as well as safe, reliable operation of the equipment. Cooling and thermal design is only one of the issues they are concerned with, although often it is a crucial issue.

Mechanical engineers have to collaborate with electronic designers using electronic design automation (EDA) software and with other mechanical designers using mechanical design automation (MDA) software. Thermal design software is expected to contribute at all stages of the design process, from concept, through design exploration and optimization, to final verification.

These diverse needs have major implications for software development, especially with regard to interface, data management, and integration.

Traditionally, CFD-based thermal design software has targeted engineering analysts with specialized knowledge of thermal design and the use of CFD techniques. These engineers still form a core group in electronics companies today; however, CFD-based thermal design has broadened to include electrical engineers, general mechanical design engineers, industrial designers, and marketing engineers. As a result, the requirements for designing a software solution have become more challenging in terms of user interface (UI) design, geometry and attribute pre-processing, interoperability with other mechanical computer-aided design (MCAD), CAE, and EDA software, obfuscation of CFD terminology and functionality, post-processing results, and meshing/solver performance.

## Geometry capture

During detailed design, the geometry comes from

both the EDA and MDA design flows. One particular challenge is that EDA systems deal with 2D representations of the electronics because both IC and PCB design are done using schematics. PCB design tools require only the component layout and often do not contain even the most basic geometric information about the components such as component height. Detailed information about the internal geometry of the chip packages is typically unavailable. FloTHERM XT does not use Spice or other models provided by some device vendors.

## Missing data

Material property data is absent from MCAD systems, so CFD simulations in general suffer from this problem. In the case of electronics cooling applications, systems are essentially constructed from many components from many different suppliers, the thermal characteristics of which are typically not well understood. These include IC packages, PCBs, heat pipes, fans, Peltier devices, etc.

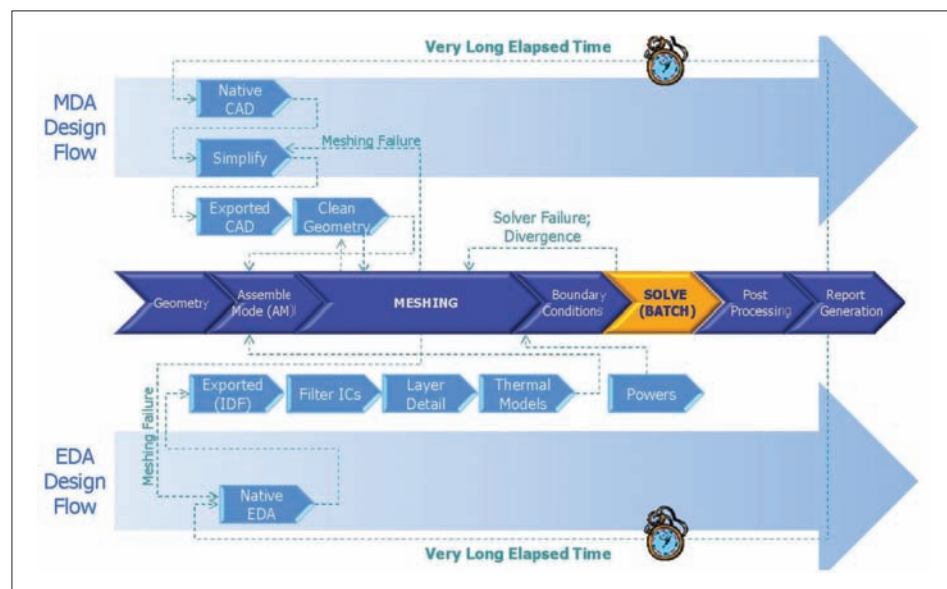
The geometry comes in part from the EDA system, which often does not include any information on the materials being used. This adds complications during electronic systems assembly where thermal interface materials (TIMs) and gap pads are used to maximize the thermal contact between different parts of the system to implement an effective cooling solution.

Also operational power information is needed for the active components to predict system temperatures under operational conditions, which vary as a function of the product's usage. Design for steady-state operation at maximum power, which leads to significant over-design, is no longer tolerable. Increasingly, transient simulations are needed to ensure reliable operation and minimize overdesign.

## Flow regime

In highly cluttered electronic systems, air is forced through channels that contain all manner of protuberances that induce low Reynolds Number transitional flow. However, this wall-induced turbulence is not self-sustaining, and the flow would be laminar if the channel were smooth. Turbulence modeling is, therefore, a particular challenge. Within a fast-paced design environment, providing a sufficiently fine mesh to perform large eddy simulation (LES) is completely impractical because of the large number of flow channels, objects, etc. combined with a large system residence time.

Until recently, the practicality of using standard two-equation Reynolds Averaged Navier-Stokes (RANS) models has been questionable. Zero-equation "effective viscosity" models have been



Traditional complex EDA/MDA integration in electronic design flow





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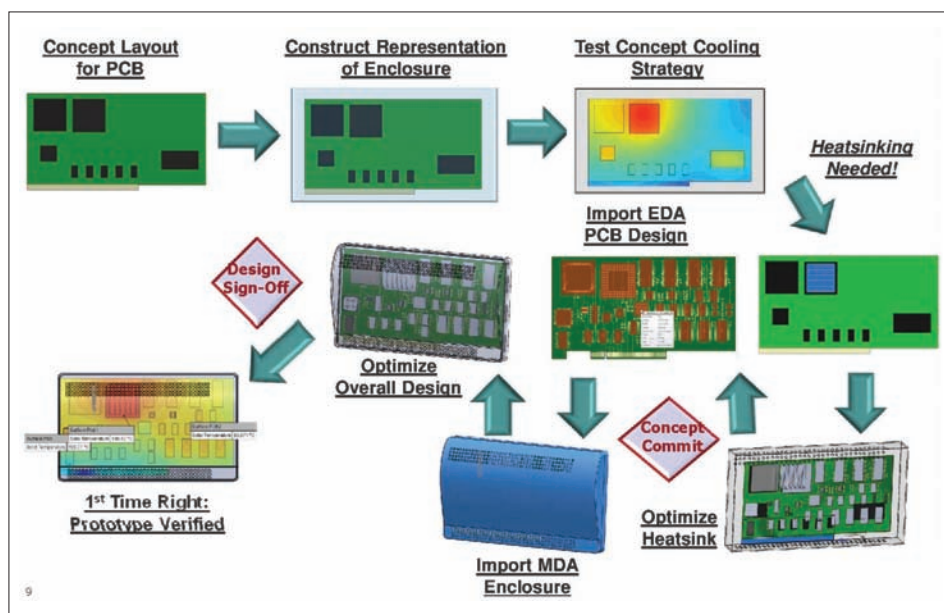
Please go to [powermodules.danfoss.com](http://powermodules.danfoss.com) for more information.

A large background image showing several white wind turbines with blue-tipped blades standing in a lush green field under a bright blue sky with scattered white clouds. A large, light-blue circular graphic is overlaid on the bottom left of the image.

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### Cooling solution with Flotherm XT

avored to impose an estimated turbulent viscosity because the low mesh densities often used would cause one and two-equations models to predict less realistic turbulent viscosity values than can be estimated based on empirical data and knowledge of the bulk flow velocity.

A key issue with one- and two-equation models is the need to refine the mesh near to the surface when used with standard, generalized, and scalable wall function treatments (log law, van Driest, 1/7th Power Law, etc.), to provide a  $y^+$  value of  $\sim 30$  for the near wall cell, with a low mesh size inflation rate out to the core flow. In electronics applications, boundary layers start at the leading edge of components, PCBs, heatsink fins, etc. resulting in a large number of very thin boundary layers to resolve within the system, so the standard advice on  $y^+$  simply cannot be followed. Consequently, LVEL remains the model of choice. However, the recent application of immersed boundary treatments to electronics cooling applications overcomes this drawback.

### Mesh generation

Although generic to CFD, mesh generation for electronics cooling applications presents a challenge because of the sheer number of solid-fluid and solid-solid surfaces that need to be captured. As a consequence of the need for fully automated optimization including geometry changes, the meshing also must be fully automated with no manual intervention beyond predefining the required mesh sizes before meshing is started.

A fortuitous outcome of using EDA systems to design components and PCBs in 2D, with no aesthetic requirements for the unpackaged electronics, is that electronics tend to contain large numbers of Cartesian-aligned objects, so Cartesian-based grid systems are the natural choice for this application. However, size

constraints are forcing electronics designers to angle components on boards, insert DIMMs at an angle, and design heatsinks with non-Cartesian profiles.

Use of simple Cartesian meshes with grid lines that "bleed" out from an object to the edges of the solution domain are inadequate because they quickly lead to unacceptable mesh counts when increasing geometric detail is added to the model. As a result, the use of locally refined Cartesian overset grids to refine the mesh within and around objects has become prevalent, allowing either porosity or voxelization treatments to approximate non-Cartesian and non-aligned Cartesian objects with acceptable accuracy in many cases.

As the amount of non-Cartesian geometry present within electronics systems has increased, so has the need for more sophisticated meshing strategies. Over recent years, Octree meshes with MCAD-embedded CFD in early product design increasingly have been used across a range of industries and applications where the product design process is built on a company's MCAD system.

In electronics, design processes vary considerably from company to company. Embedding CFD within the MCAD system may not facilitate its use because often much of the early design work will be done outside the MCAD environment, and the design process may be centered on the company's EDA flow. Thus, the simulation approach used in MCAD-embedded CFD needs to be available within a stand-alone product.

### Hardware environment

Traditionally, thermal design has been done alongside electronic design. The use of high performance computing (HPC) infrastructure for CFD has been far less than in other industry sectors; for example, in automotive, HPC has facilitated the use of LES to undertake "high

fidelity" CFD to address difficult aspects of the product design, such as aero-acoustics. But in electronics cooling applications, increased simulation precision does not translate into improved product quality. The quality of the simulation model is limited by far greater uncertainty in the input data.

To date, good scalar performance with reasonable scaling up to 8–16 cores has matched market requirements. Good scaling for a limited number of shared memory nodes is likely to remain the target for hardware performance. The hardware environment may change away from desktop to cloud-based computing, which will greatly facilitate design space exploration by the use of numerical design of experiment techniques.

As a consequence of design margins shrinking, the need for simulation accuracy is increasing. This however, does not translate directly into a need for higher fidelity CFD. Indeed, since the early 2000s power increases have occurred at higher levels of packaging, such as the PCB.

What has this to do with accuracy? The allowable temperature rise from ambient to junction is not increasing, but as power densities increase within the package, PCB, etc., the proportion of the temperature rise that occurs in the air is diminishing. Put another way, the importance of modeling the conduction within the solid structures is increasing. This explains the emphasis placed on MCAD integration (e.g., for heatsink design), and perhaps more importantly EDA integration, to accurately capture the copper content and distribution on PCBs, effects such as Joule heating in traces, and power and ground planes, and to accurately measure the thermal conductivity of TIM materials, particularly the softer Type I and Type II materials that are not well-suited to being measured in ASTM D5470-based equipment.

### Solving the thermal design challenges

FloTHERM XT provides easier modeling of more complex devices and enclosures, connected with SmartPart technology where required, particularly for LED lighting, consumer electronics, aerospace/defense, and automotive designs.

Meshing can take up a significant amount of time and energy in some general-purpose CFD codes and can be a cause of frustration when it goes wrong. Most general mechanical engineers would like to simply have the software do the job for them wherever possible, but with the ability to switch to more manual definition should the need arise, and this has reinforced the need for more sophisticated meshing strategies. The advanced code in FloTHERM XT provides semi-automatic, object-based algorithms, with options to adjust the mesh manually where necessary or to allow the freedom and control that is required by the more experienced, and CFD-aware, thermal engineers.

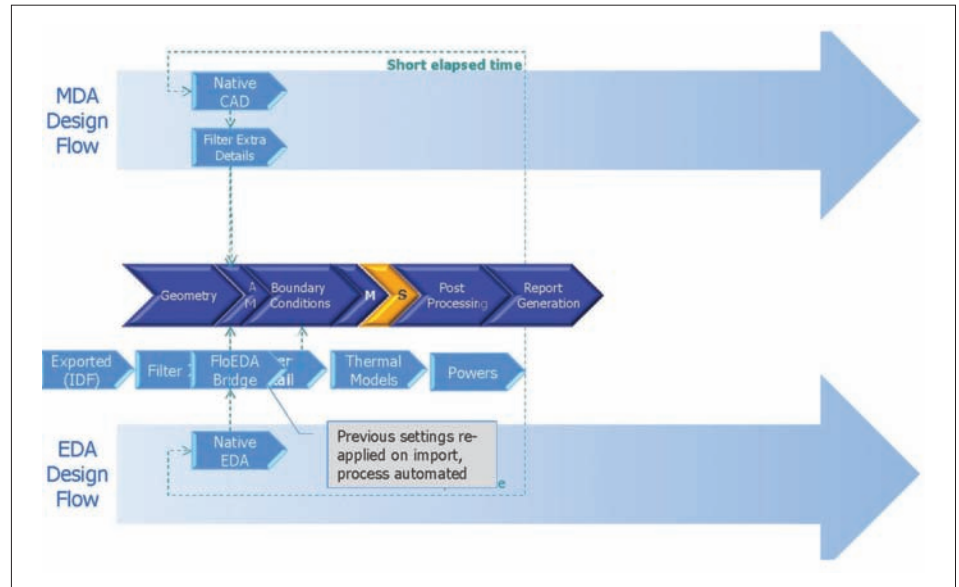
FloTHERM XT uses highly stable numerical schemes and solution controls that operate semi-automatically to control the convergence of the solution with only the minimum of intervention



ever being required. For electronics cooling applications, issues relating to turbulence modeling are rarely, if ever, the largest source of error in the results. It is more likely to be uncertainties in power dissipation, materials, flow rates, or interface resistances. However, turbulence can be a source of concern for some more specialized designs. The software provides options for laminar, transitional, and turbulent flows, but limits the turbulence models that are available to avoid confusion. FloTHERM XT makes use of a general two-equation model combined with a proprietary immersed boundary treatment for near-wall effects that smoothly transitions between the different flow regimes.

### Summary

Since the launch of FloTHERM, the challenges facing thermal designers have changed. Power dissipations increased, and products have become smaller and more tightly packed than ever before. Design complexity is driving the EDA and MDA design flows closer together, with pressure on thermal designers to use native geometry from these systems without simplification to keep the simulation model up to date, minimize the time taken to analyze design variants, and increase accuracy of results. These changes have affected the demographics and skill sets of engineers, which has implications for software usability, geometry



**Optimized MDA/EDA integration in electronic design flow**

handling, and the underlying CFD technology. FloTHERM XT has been written to support different types of design engineers and levels of expertise, to be as usable in early design as it is in late design verification, with the ability to evolve the model as the design is elaborated and provide an environment that delivers the best possible collaboration between the main

mechanical and electrical design flows.

### Literature

Efficient Thermal Design for Power LEDs and Semiconductors, Power Electronics Europe 1-2012, Pages 17-21

[www.mentor.com/flotherm-xt](http://www.mentor.com/flotherm-xt)

# Integrated MOSFET Buck Regulators

At APEC 2013 Micrel rolled out its latest family of integrated MOSFET buck regulators optimized for 12 V rails, with 6/9/12 A output current. The new MIC2405x family is comprised of six common-footprint, DC/DC buck regulators that leverage proprietary so-called HyperSpeed Control™ and HyperLight Load® architectures. The devices provide flexible solutions for distributed power systems, communications networking, infrastructure, and

industrial applications.

The common footprint shared by all devices in this family enables current scalability which in turn provides design flexibility for the power supply designer. This family of regulators has been tailored to be stable independent of the output capacitance's Equivalent Series Resistance (ESR), thus solving the perpetual problem of stability when dealing with distributed output

capacitance. Moreover, these buck regulators provide more than 95 % peak efficiency and operate at 600<kHz switching frequency with  $\pm 1$  % of output voltage accuracy (with output adjustable down to 0.8 V).

### Continuous mode operation

The MIC24055 is an adaptive ON-time synchronous step-down DC/DC regulator with an internal 5V linear regulator and a power good (PG) output. It is designed to operate over a wide input voltage range from 4.5V to 19V and provides a regulated output voltage at up to 12 A of output current. An adaptive ON-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented without an external sense resistor. The device includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output

**Schematic and applications of Micrel's new Integrated MOSFET Buck Regulators**

Part Numbers	I <sub>OUT</sub> (A)	Packages
MIC24051/2	6	MLF - 28L
MIC24053/4	9	MLF - 28L
MIC24055/6	12	MLF - 28L

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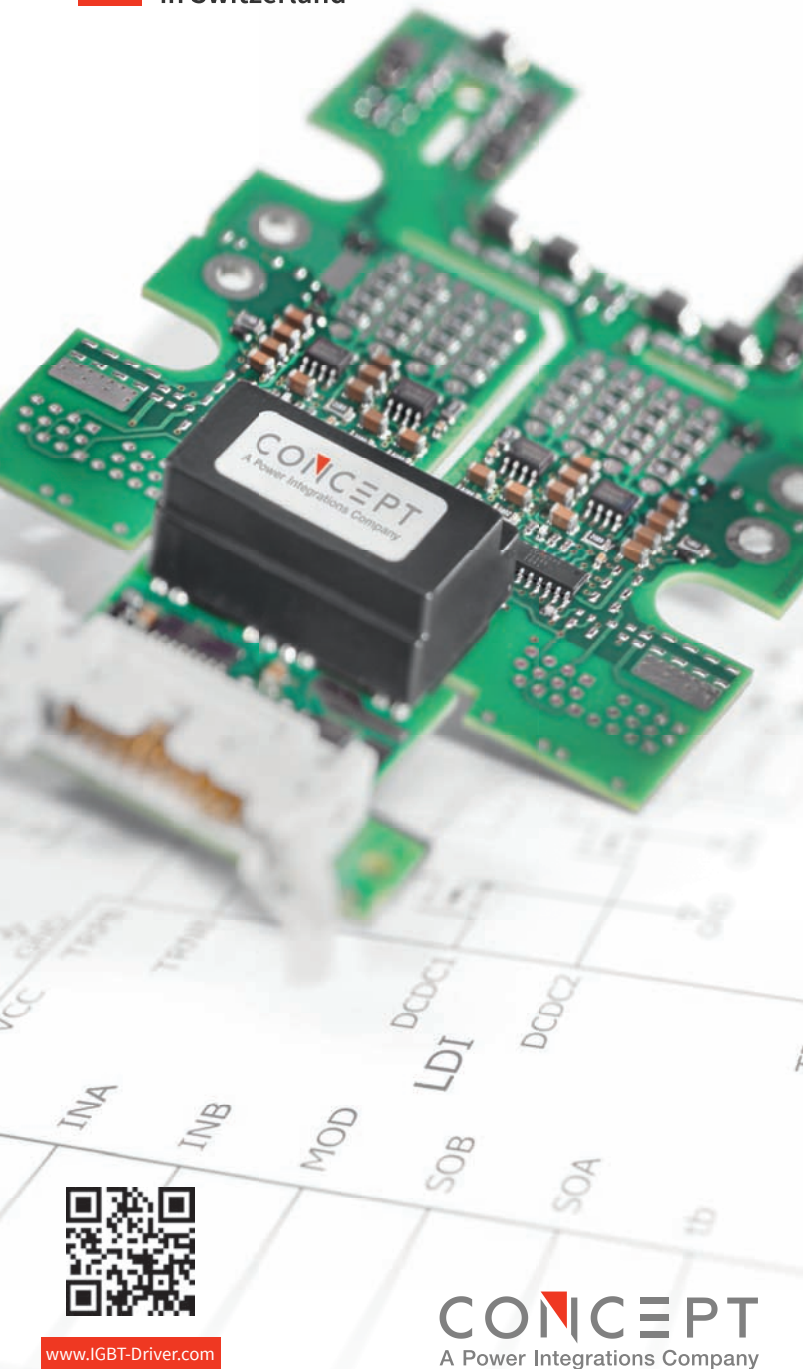
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voltage rise time. The MIC24055 operates in a continuous mode as shown in the block diagram.

In continuous mode, the output voltage is sensed by the feedback (FB) pin via the voltage divider R1 and R2, and compared to a 0.8 V reference voltage  $V_{REF}$  at the error comparator through a low gain transconductance (gm) amplifier. If the feedback voltage decreases and the output of the gm amplifier is below 0.8 V, then the error comparator will trigger the control logic and generate an ON-time period.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the gm amplifier is below 0.8 V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time  $t_{OFF(min)}$ , which is about 300 ns, the control logic will apply the  $t_{OFF(min)}$  instead, since  $t_{OFF(min)}$  is required to maintain enough energy in the boost capacitor ( $C_{BST}$ ) to drive the high-side MOSFET.

It is not recommended to use an OFF-time close to  $t_{OFF(min)}$  during steady-state operation. Also, as  $V_{OUT}$  increases, the internal ripple injection will increase and reduce the live regulation performance. Therefore, the maximum output voltage should be limited to 5.5 V and the maximum external ripple injection should be limited to 200 mV.

The actual ON-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the  $V_{DD}$  voltage. Also, the minimum  $t_{ON}$  results in a lower switching frequency in high  $V_{IN}$  to  $V_{OUT}$  applications, such as 18 V to 1.0 V. The minimum  $t_{ON}$  measured on the evaluation board is about 100 ns. During load transients, the switching frequency is changed due to the varying OFF-time.

During steady-state, the gm amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the  $t_{ON}$  estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when  $V_{FB}$  falls below  $V_{REF}$ , the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

During a load transient the output voltage drops due to the sudden load increase, which causes the  $V_{FB}$  to be less than  $V_{REF}$ . This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time  $t_{OFF(min)}$  is generated to charge  $C_{BST}$  since the feedback voltage is still below  $V_{REF}$ . Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC24055 converter.

Unlike true current-mode control, the device uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The control loop has the advantage of eliminating the need for slope compensation.

In order to meet the stability requirements, the feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the gm amplifier and the error comparator. The recommended feedback voltage ripple is 20 – 100 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the gm amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation.

#### Soft-start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower





### Inductor selection

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC24055 requires the

### Output capacitor selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view.

The MIC24055 requires at least 20 mV peak-to-peak ripple at the FB pin to make the gm amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor's ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20 % greater for aluminum electrolytic or OS-CON.

The input capacitor for the power stage input  $V_{IN}$  should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple will primarily depend on the input capacitor's ESR.

More detailed guidelines and application informations can be found in the MIC24055 datasheet available on Micrel's website.

The MIC24055 implements an internal digital soft-start by making the 0.8 V reference voltage  $V_{REF}$  ramp from 0 to 100 % in about 3 ms with 9.7 mV steps. Therefore, the output voltage is controlled to increase slowly by a staircase VFB ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. Pin VDD must be powered up at the same time or after pin VIN to make the soft-start function correctly.

### Current limit

In each switching cycle of the converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. If the peak inductor current is greater than 21 A, then the MIC24055 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode is called "hiccup mode" and its purpose is to protect the downstream load in case of a hard short.

The power good (PG) pin is an open drain output which indicates logic high when the output is nominally 92 % of its steady state voltage. A pull-up resistor of more than 10 k $\Omega$  should be connected from PG to VDD.

## MOSFET gate drive

The block diagram shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and CBST. This circuit supplies energy to the high-side drive circuit. Capacitor CBST is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0 V. When the high-side MOSFET driver is turned on, energy from C<sub>BST</sub> is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V<sub>IN</sub>. Diode D1 is reverse biased and C<sub>BST</sub> floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10 mA so a 0.1 pF to 1 pF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle.

When the low-side MOSFET is turned back on, CBST is recharged through D1. A small resistor  $R_G$ , which is in series with CBST, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the VDD supply voltage. The nominal low-side gate drive voltage is VDD and the nominal high-side gate drive voltage is approximately  $V_{DD} - V_{DIODE}$ , where  $V_{DIODE}$  is the voltage drop across D1. An

# Driving GaN Switches Efficiently

Gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design. Emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability.

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. With advent of digital power, this situation will be often encountered since the PWM signal from the digital controller is often a 3.3 V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the 3.3 V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses.

Traditional buffer drive circuits based on NPN and PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power since they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-

frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

## Optimized for GaN FETs

TI's UCC27611 is a single-channel, high-speed, gate driver optimized for 5-V drive, specifically addressing enhancement mode GaN FETs (see block diagram). The drive voltage  $V_{REF}$  is precisely controlled by internal linear regulator to 5 V. The UCC27611 offers asymmetrical rail-to-rail peak current drive capability with 4 A source and 6 A sink. Split output configuration allows individual turn-on and off time optimization depending on FET. Package and pinout with minimum parasitic inductances reduce the rise and fall time and limit the ringing. Additionally, the short propagation delay with minimized tolerances and variations allows efficient operation at high frequencies. The 2  $\Omega$  and 0.3  $\Omega$  pull-up and pull-down resistance boosts immunity to hard switching with high slew rate dV and dt.

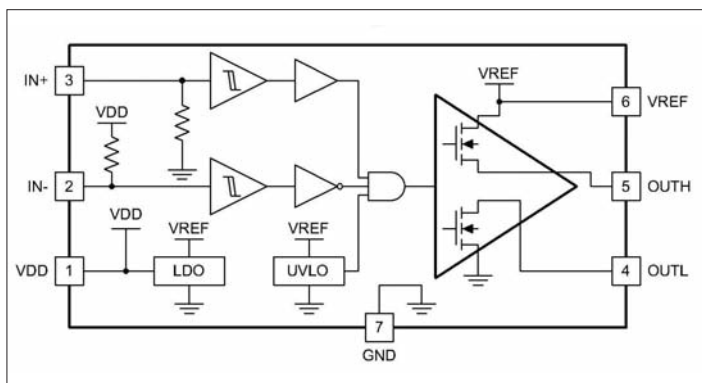
The independence from VDD input signal thresholds ensure TTL and CMOS low-voltage logic compatibility. For safety reason when the input pins are in a floating condition, the internal input pull-up and down resistors hold the output LOW. Internal circuitry on  $V_{REF}$  pin provides an under voltage lockout function that holds output LOW until  $V_{REF}$  supply voltage is within operating range.

The UCC27611 is offered in a small 2 mm x 2 mm WSON-6 package (DRV) with exposed thermal and ground pad which improves the package power handling capability. It operates over wide temperature range from -40°C to 140°C.

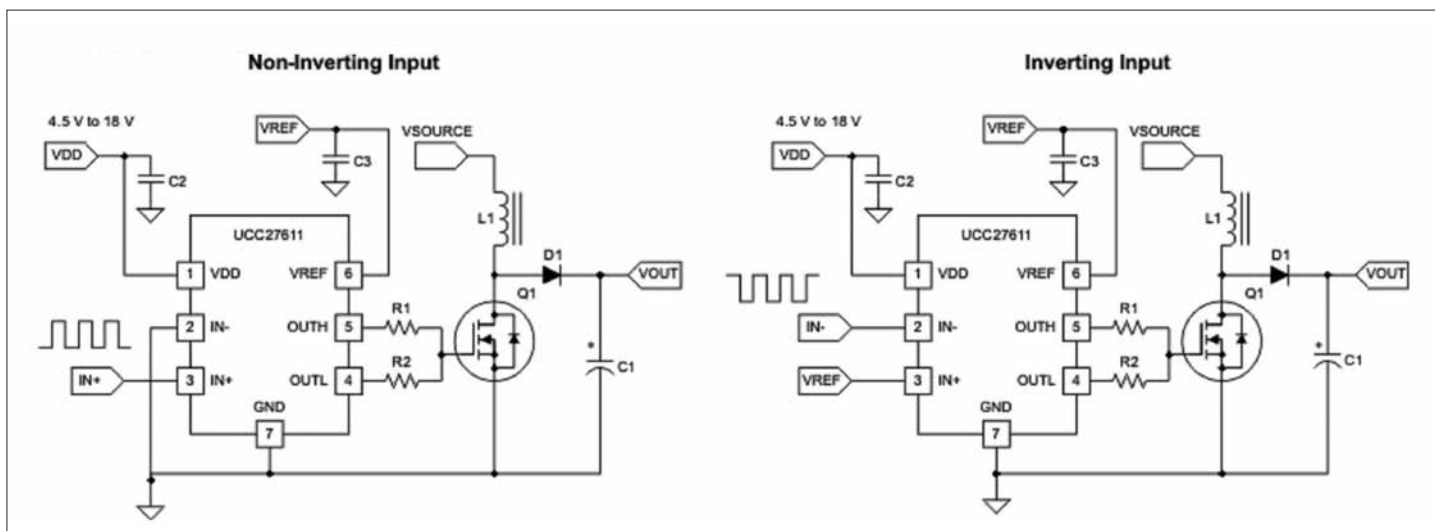
## Powering up

The UCC27611 devices have internal Under Voltage LockOut (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (i.e. when VDD voltage less than  $V_{ON}$  during power up and when VDD voltage is less than  $V_{OFF}$  during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 3.8 V with 250 mV typical hysteresis. This hysteresis helps prevent chatter when low  $V_{DD}$  supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in  $I_{DD}$ .

The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide bandgap power semiconductor devices.



UCC27611 block diagram



UCC27611 functional diagram (non-inverting and inverting)





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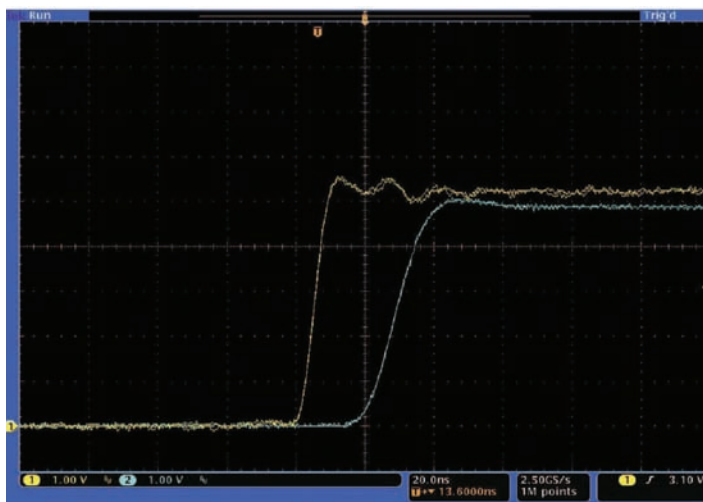
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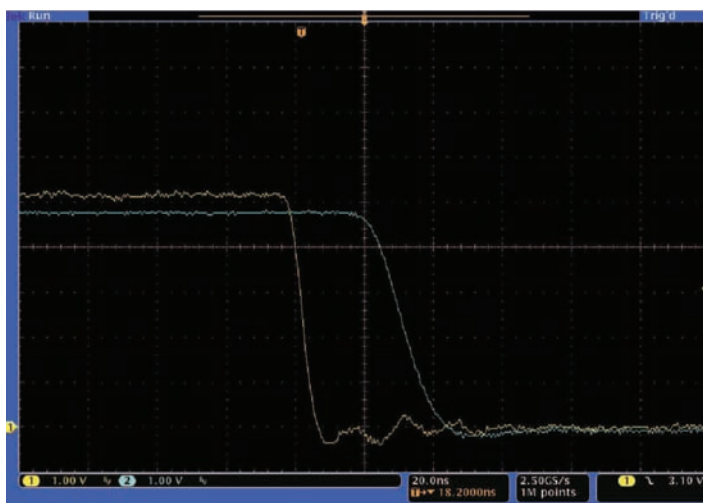
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Output rising waveform (Ch 1 = IN+, Ch 2 = OUTPUT)



Output falling waveform (Ch 1 = IN+, Ch 2 = OUTPUT)

For example, at power up, the UCC27611 driver output remains LOW until the  $V_{DD}$  voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with  $V_{DD}$  until steady-state  $V_{DD}$  is reached. In the non-inverting operation (PWM signal applied to IN+ pin), the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN- pin) the output remains LOW until the UVLO threshold is reached, and then the output is out-of-phase with the

input. In both cases, the unused input pin must be properly biased to enable the output. It is worth noting that in these devices the output turns to high state only if IN+ pin is high and IN- pin is low after the UVLO threshold is reached.

Since the driver draws current from the  $V_{DD}$  pin to bias all internal circuits, for the best high-speed circuit performance, two  $V_{DD}$  bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1  $\mu\text{F}$  ceramic capacitor should be located as close as possible to the  $V_{DD}$  to GND pins of the gate driver. In addition, a larger capacitor (such as 1  $\mu\text{F}$ ) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

### Operating supply current

The UCC27611 feature very low quiescent  $I_{DD}$  current. The total supply current is the sum of the quiescent  $I_{DD}$  current, the average  $I_{OUT}$  current due to switching and finally any current related to pull-up resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from  $V_{DD}$  supply through the pull-up resistors. Knowing the operating frequency ( $f_{sw}$ ) and the MOSFET gate ( $Q_G$ ) charge at the drive voltage being used, the average  $I_{OUT}$  current can be calculated as product of  $Q_G$  and  $f_{sw}$ .

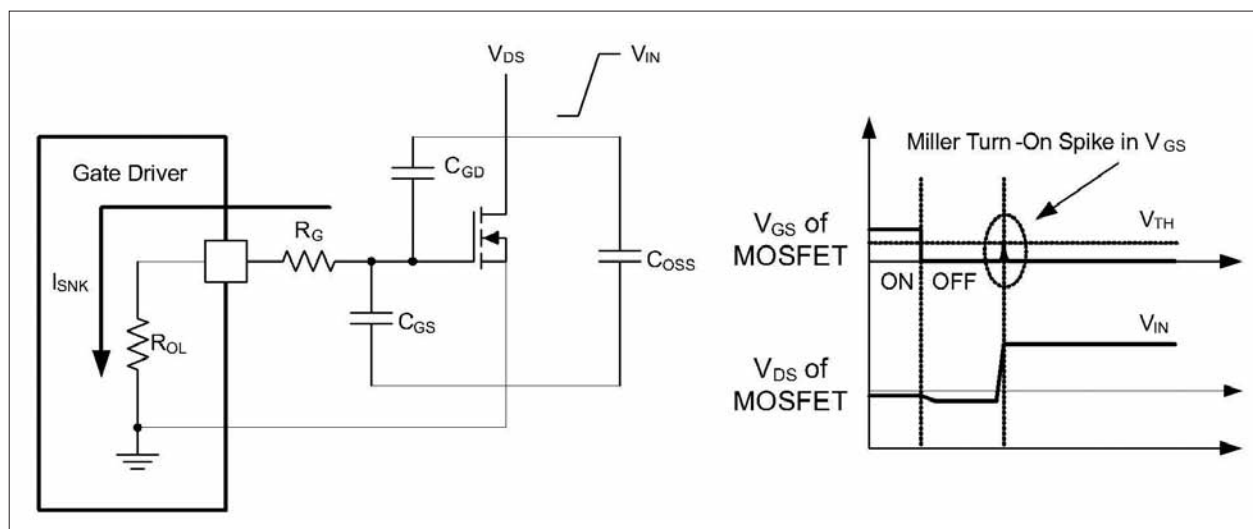
### Input stage

The input pins of the UCC27611 is based on a TTL and CMOS compatible input threshold logic that is independent of the  $V_{DD}$  supply voltage. With typical high threshold of 1.95 V and typical low threshold of 1.3 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3 V and 5 V digital power controllers. Wider hysteresis (typ. 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

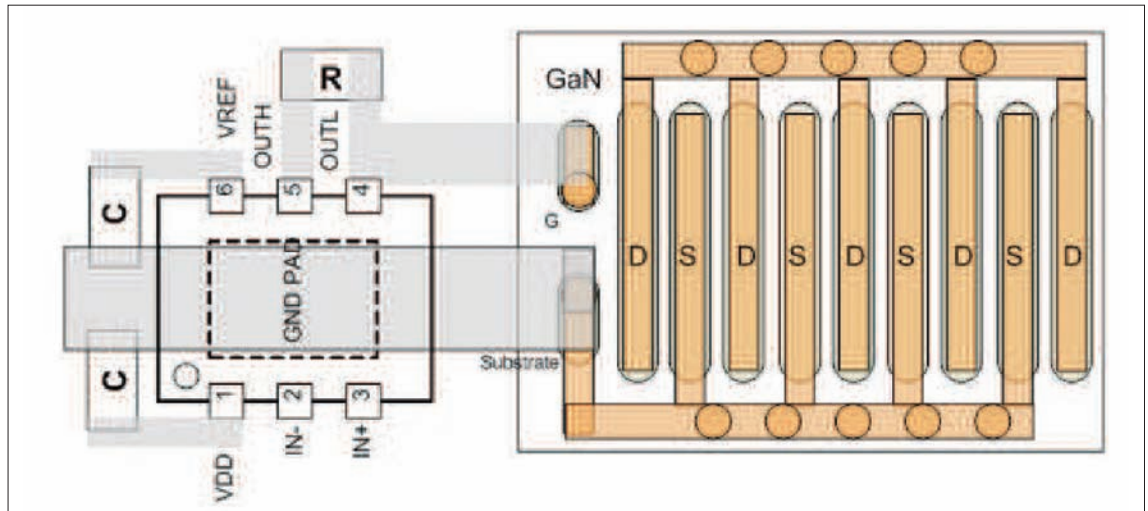
The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using  $V_{DD}$  pull-up resistors on all the inverting inputs (IN- pin) or GND pull-down resistors on all the non-inverting input pins (IN+ pin). The device also features a dual input configuration with two input pins available to control the state of the output.

The user has the flexibility to drive the device using either a non-inverting input pin (IN+) or an inverting input pin (IN-). The state of the output pin is dependent on the bias on both the IN+ and IN- pins. Once an input pin has been chosen for PWM drive, the other input pin (the unused input pin) must

Low pull-down impedance 4 A and 6 A asymmetrical drive (output stage mitigates Miller turn-on effect)





**PCB layout recommendation**

be properly biased in order to enable the output. The unused input pin cannot remain in a floating condition because whenever any input pin is left in a floating condition the output is disabled for safety purposes. Alternatively, the unused input pin can effectively be used to implement an enable and disable function.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout is not optimal.

High  $dI$  and  $dt$  current from the driver output coupled with board layout parasitic can cause ground bounce. Since the device features just one GND pin which may be referenced to the power ground, this may modify the differential voltage between input pins and GND and trigger an unintended change of output state. Because of fast 13-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.

1 V input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

In the worst case, when a slow input signal is used and PCB layout is not optimal, it may be necessary to add a small capacitor (1 nF) between input pin and ground very close to the driver device. This helps to convert the differential mode noise with respect to the input logic circuitry into common mode noise and avoid unintended change of output state.

**Output stage**

The UCC27611 device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain and collector voltage experiences  $dV$  and  $dt$ ).

The device output stage features a hybrid pull-up structure using a parallel arrangement of N-channel and P-channel MOSFET devices. By turning on the N-channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turn on.

An example of a situation where Miller turn on is a concern is synchronous rectification (SR). In SR application, the  $dV$  and  $dt$  occurs on MOSFET drain when the MOSFET is already held in off state by the gate driver. The current discharging the CGD Miller capacitance during this  $dV$  and  $dt$  is shunted by the pull-down stage of the driver. If the pull-down impedance is not low enough then a voltage spike can result in the VGS of the MOSFET, which can result in spurious turn on. UCC27611 offers a  $0.35\ \Omega$  (typ) pull-down impedance boosting immunity against Miller turn on.

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500 mA reverse current

without either damage to the device or logic malfunction.

**PCB layout recommendations**

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness.

The UCC27611 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher  $V_{DD}$  voltages, the peak-current capability is even higher (4 A and 6 A peak current at  $V_{DD}$  12 V). Very high  $dI$  and  $dt$  can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD and VREF bypass capacitors between VDD, VREF and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turn on of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD, VREF bypass capacitors) should be minimized as much as possible in order to keep the stray inductance to a minimum. High  $dI$  and  $dt$  is established in these loops at two instances – during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
- In noisy environments, it may be necessary to tie the unused Input pin of UCC27611 to VDD or VREF (in case of IN+) or GND (in case of IN-) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output.

<http://www.ti.com/product/ucc27611>

# GaN Transistors for Efficient Power Conversion

For over three decades, power management efficiency and cost showed steady improvement as innovations in power MOSFET structures, technology, and circuit topologies paced the growing need for electrical power in our daily lives. In the new millennium, however, the rate of improvement slowed as the silicon power MOSFET asymptotically approached its theoretical bounds. **Alex Lidow, CEO, and Johan Strydom, VP Applications Engineering, Efficient Power Conversion Corporation, El Segundo, USA**

Power MOSFETs first started appearing in 1976 as alternatives to bipolar transistors. These majority carrier devices were faster, more rugged, and had higher current gain than their minority-carrier counterparts. As a result, switching power conversion became a commercial reality. AC/DC switching power supplies for early desktop computers were among the earliest volume consumers of power MOSFETs, followed by variable speed motor drives, fluorescent lights, DC/DC converters, and thousands of other applications that populate our daily lives.

Many generations of power MOSFETs have been developed by several manufacturers over the years. Benchmarks were set, and fell, every year or so for 30 plus years. There are still improvements to be made. For example, Superjunction devices and IGBTs have achieved conductivity improvements beyond the theoretical limits of a simple vertical majority carrier MOSFET. These innovations may still continue for quite some time and will certainly be able to leverage the low cost structure of the power MOSFET and the well-educated base of designers who, after many years, have learned to squeeze every ounce of performance out of their power conversions circuits and systems.

## The GaN journey begins

HEMT (High Electron Mobility Transistor) Gallium Nitride (GaN) transistors on Silicon Carbide (SiC) substrates first started appearing in about 2004 with depletion-mode RF transistors made by Eudyna Corporation in Japan. GaN RF transistors have continued to make inroads in such applications as several other companies have entered in the market. Acceptance outside this market, however, has been limited by device cost as well as the inconvenience of depletion mode operation.

In June 2009 Efficient Power Conversion Corporation (EPC) introduced

Properties*	GaN	Si	SiC
$E_g$ (eV)	3.4	1.12	3.2
$E_{BR}$ (MV/cm)	3.3	0.3	3.5
$V_s$ ( $\times 10^7$ cm/s)	2.5	1.0	2.0
$\mu$ ( $\text{cm}^2/\text{Vs}$ )	990 - 2000	1500	650

Table 1: Material properties of GaN, SiC, and Silicon at 300 K

the first enhancement-mode GaN on silicon (eGaN®) FETs designed specifically as power MOSFET replacements to be produced on standard Silicon manufacturing technology and facilities.

Table 1 shows four key electrical properties of three semiconductor materials (GaN, Si, SiC) contending for the power management market. One way of translating these basic crystal parameters into a comparison of device performance in a power transistor is to calculate the best theoretical performance that could be achieved in each of the three candidates.

For power devices there are many characteristics that matter in the variety of power conversion systems available today. Five of the most important are conduction efficiency, breakdown voltage, switching efficiency, size and cost.

Using the data from table 1 (and adjusting for the enhanced mobility of the GaN 2D Electron Gas), we can calculate the theoretical minimum device on-resistance (the inverse of conductivity) as a function of breakdown voltage and as a function of material.

As shown in Figure 1, SiC and GaN both

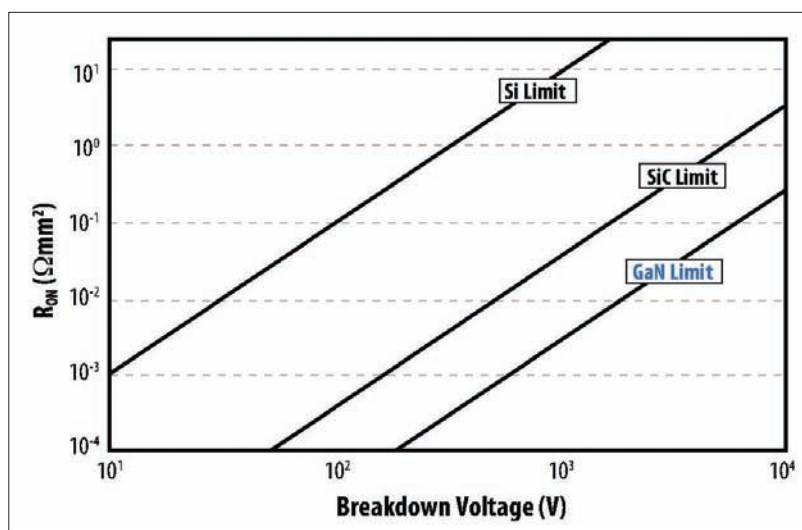
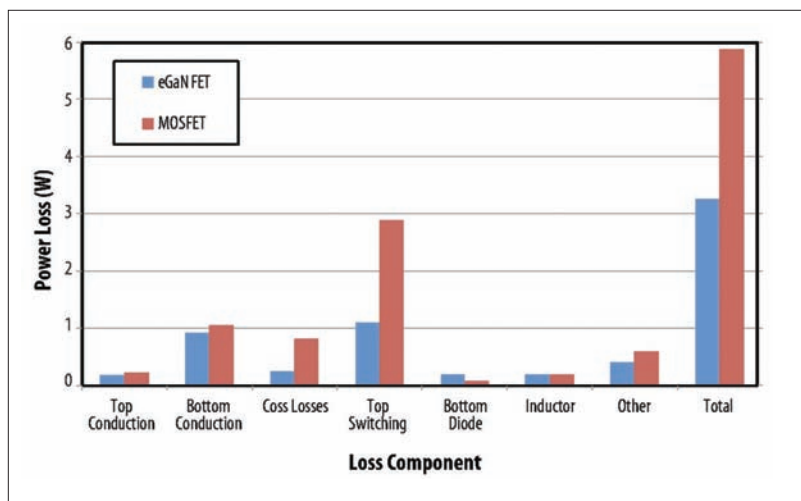


Figure 1: Theoretical on-resistance vs blocking voltage capability for Silicon, Silicon Carbide, and Gallium Nitride





**Figure 2: Comparison of switching losses of eGaN FETs vs Silicon MOSFETs in a 12 V/1.2 V Buck Converter operating at 1 MHz. For each socket both devices have similar on-resistance**

have a superior relationship between on-resistance and breakdown voltage due to their higher critical electric field strength. This allows devices to be smaller and the electrical terminals closer together for a given breakdown voltage requirement. GaN has an extra advantage compared with SiC as a result of the enhanced mobility of electrons in the 2DEG. This translates into a GaN device with a smaller size for a given on-resistance and breakdown voltage.

In Figure 2 is a comparison between Silicon MOSFET and eGaN FET power losses for a common Buck Converter circuit. The on-resistances of the transistors are equal, so the difference in total power losses can be attributed to the superior switching capability of the eGaN FETs. The eGaN device's lateral structure also lends itself to flip-chip packaging, which is a very high performance packaging solution due to the minimal increase in on-resistance and terminal inductance. Add to this a distinct die area advantage over Silicon and the resultant solution is a superior power device in a high performance package that is significantly smaller than anything available today.

EPC's normally-off eGaN FETs (Figure 3) stem from a relatively new technology and,

as such, remain somewhat more expensive to produce than their Silicon counterparts. This, however, is a temporary situation. There are no insurmountable barriers to achieving an even lower cost for an equivalent performance eGaN FET compared with a power MOSFET or IGBT.

#### Enhancement mode FET structure

EPC's enhancement mode process begins with Silicon wafers. A thin layer of Aluminum Nitride (AlN) is grown on the Silicon to provide a seed layer for the subsequent growth of a Gallium Nitride heterostructure. A heterostructure of Aluminum Gallium Nitride (AlGaIn) and then GaN is grown on the AlN. This layer provides a foundation on which to build the eGaN FET. A very thin AlGaIn layer is then grown on top of the highly resistive GaN. It is this thin layer that creates

a strained interface between the GaN and AlGaIn crystals layers. This interface, combined with the intrinsic piezoelectric nature of GaN, creates a two dimensional electron gas (2DEG) which is filled with highly mobile and abundant electrons.

Further processing of a gate electrode forms a depletion region under the gate. To enhance the FET, a positive voltage is applied to the gate in the same manner as

turning on an n-channel, enhancement mode power MOSFET. A cross section of this structure is depicted in Figure 3. Additional layers of metal are added to route the electrons to gate, drain, and source terminals. This structure is repeated many times to form a power device as shown in Figure 4. Conveniently, eGaN FETs behave similarly to Silicon MOSFETs with some exceptions that will be explained below.

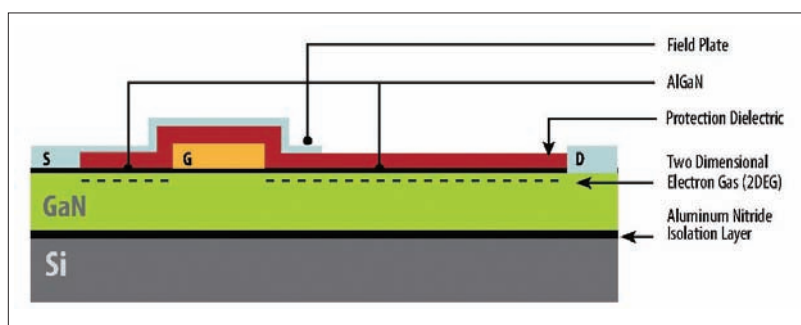
$R_{DS(ON)}$  versus  $V_{GS}$  curves are similar to MOSFETs. EPC first generation GaN transistors are designed to operate with 4 - 5 V gate drive. The temperature coefficient of  $R_{DS(ON)}$  of the eGaN FET is also similar to the Silicon MOSFET as it is positive, but the magnitude is slightly less. The 125°C point is 1.6 times the 25°C point for the EPC1001 compared to 1.7 for Silicon.

The threshold of Gallium Nitride transistors is lower than that of Silicon MOSFETs. This is made possible by the almost flat relationship between threshold and temperature along with the very low  $C_{GD}$ . Since the device starts to conduct significant current at 1.6 V, care must be taken to ensure a low impedance path from gate to source when the device needs to be held off during  $dv/dt$  in a rectifier function.

In addition to the low  $R_{DS(ON)}$ , the lateral structure of the eGaN FET makes it a very low charge device as well. It has the capability of switching hundreds of volts in nanoseconds, giving it multiple megahertz capability. This capability will lead to smaller power converters, and higher fidelity class D audio amplifiers. Most important in switching is  $C_{GD}$ . With the lateral structure,  $C_{GD}$  comes only from a small corner of the gate. An extremely low  $C_{GD}$  leads to the very rapid voltage switching capability of GaN transistors.

$C_{GS}$  consists of the junction from the gate to the channel, and the capacitance of the dielectric between the gate and the field plate.  $C_{GS}$  is large when compared with  $C_{GD}$ , giving eGaN FETs good  $dv/dt$  immunity, but still small when compared with Silicon MOSFETs giving them very short delay times, and good controllability in low duty cycle applications. A 48 V to 1 V buck regulator has been demonstrated at 1 MHz using 100 V eGaN FETs from EPC.  $C_{GS}$  is also small, being limited to the capacitance across the dielectric from the field plate to the drain. Capacitance versus voltage curves for eGaN FETs are similar to those for Silicon except that, for a similar resistance, its capacitance is significantly lower.

The last part of the performance picture is that of the so-called "body diode". EPC's GaN transistor structure is a purely lateral device, absent of the parasitic bipolar



**Figure 3: eGaN® FET structure**

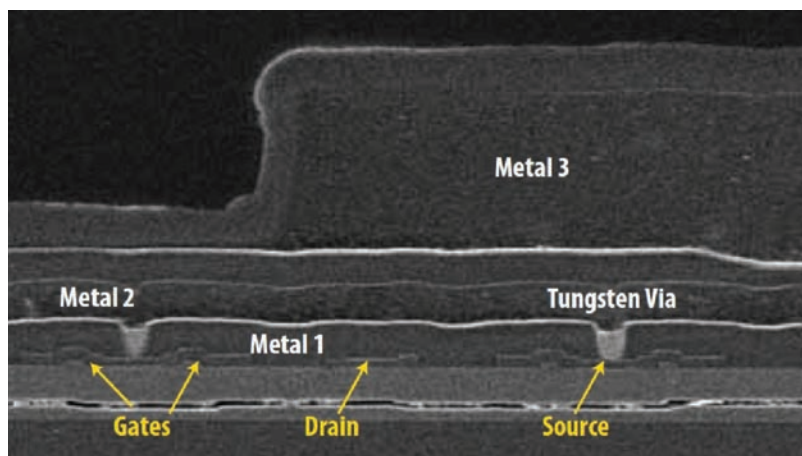


Figure 4: SEM micrograph of an eGaN FET

junction common to Silicon-based MOSFETs. As such, reverse bias or "diode" operation has a different mechanism but similar function. With zero bias gate to source, there is an absence of electrons under the gate region. As the drain voltage is decreased, a positive bias on the gate is created relative to the drift region, injecting electrons under the gate. Once the gate threshold is reached, there will be sufficient electrons under the gate to form a conductive channel. The benefit to this mechanism is that there are no minority carriers involved in conduction, and therefore no reverse recovery losses. While

$Q_{RR}$  is zero, output capacitance ( $C_{OSS}$ ) has to be charged and discharged with every switching cycle. For devices of similar  $R_{DS(ON)}$ , eGaN FETs have significantly lower  $C_{OSS}$  than Silicon MOSFETs. As it takes threshold voltage to turn on the eGaN FET in the reverse direction, the forward voltage of the "diode" is higher than Silicon transistors. As with Silicon MOSFETs, care should be taken to minimize diode conduction.

#### Conclusion

Enhancement mode transistors using Gallium Nitride grown on top of Silicon

have characteristics very similar to the power MOSFET, but with improved high speed switching, lower on-resistance, and a smaller size than their Silicon predecessors. eGaN FETs provide superior performance when compared to MOSFETs. For 200 V devices, the lead is about 10x. As the specific  $R_{DS(ON)}$  for eGaN decreases, its lead in RxQ figure of merit will increase. As voltage increases with planned new releases up to 600 V, the comparisons will become even more favorable towards eGaN FETs. Due to their increased switching frequency, they can increase the performance of applications currently using standard MOSFETs and enable applications beyond the range of Silicon and open applications that were not achievable with Silicon-based FET technology.

#### Literature

White Paper "Gallium Nitride (GaN) Technology Overview", EPC 2012

Product Brief "eGaN® FETs: Ultra High Efficiency Power Switch", EPC 2013

APEC 2013, Professional Education Seminar 7, "GaN Transistors for Efficient Power Conversion"

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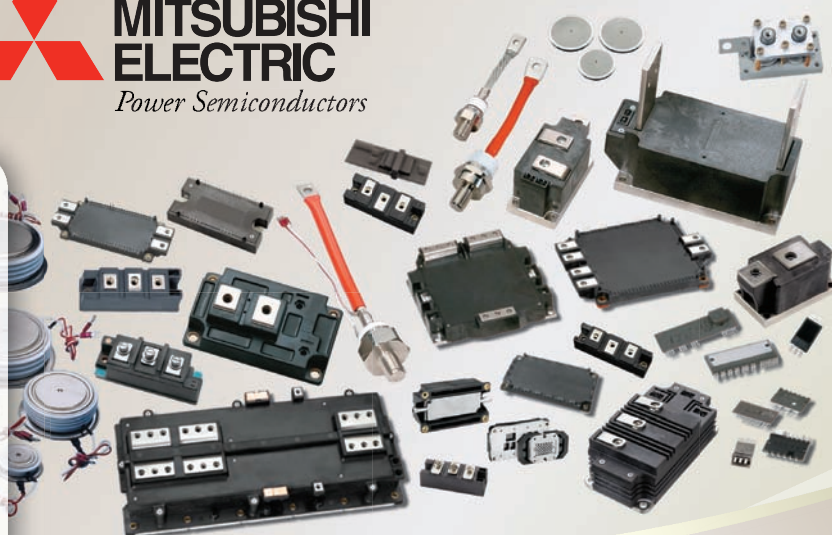
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# Industrial Grade 25 A Versatile Voltage Regulator

At APEC International Rectifier introduced the IR3847 high current Point-of-Load (POL) integrated voltage regulator that extends the current rating of IR's third generation SupIRBuck® family up to 25 A in a compact 5x6 mm package. **Ramesh Balasubramaniam, Cecilia Contenti, Enterprise Power Business Unit, International Rectifier, El Segundo, USA**

As a result of a new thermally enhanced package using copper clip and several proprietary innovations in the controller, the IR3847 can operate without heatsink, and reduces PCB size by 20 % compared to alternative integrated solutions and 70 % compared to discrete solutions using a controller and power MOSFETs. A complete 25 A power supply solution can be implemented in as little as 168 mm<sup>2</sup>. Peak efficiency is greater than 96 % and temperature rise at 25 A is as low as 50 K (see Figure 1).

## Theory of operation

The IR3847 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types. The switching frequency is programmable from 300 kHz to 1.5 MHz by connecting an external resistor from Rt pin to LGnd. The output voltage is precisely regulated and can be programmed via two external resistors from 0.6V to 0.86 \* PVin.

The IR3847 operates with an internal bias supply (LDO) which is connected to the VCC pin. This allows operation with single supply. The bias voltage is variable according to load condition. If the output load current is less than half of the peak-

to-peak inductor current, a lower bias voltage, 4.4 V, is used as the internal gate drive voltage; otherwise, a higher voltage, 6.8 V, is used. This feature helps the converter to reduce power losses. The device can also be operated with an external supply from 4.5 to 7.5 V, allowing an extended operating input voltage (PVin) range from 1.0 to 21 V. For using the internal LDO supply, the Vin pin should be connected to PVin pin. If an external supply is used, it should be connected to VCC pin and the Vin pin should be shorted to VCC pin.

## Under-voltage lockout and POR

The under-voltage lockout circuit monitors the voltage of VCC pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drops below the set thresholds. Normal operation resumes once VCC and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram in Figure 2). When the POR is asserted the soft start sequence starts.

## Enable

The Enable features another level of flexibility for startup. The Enable has

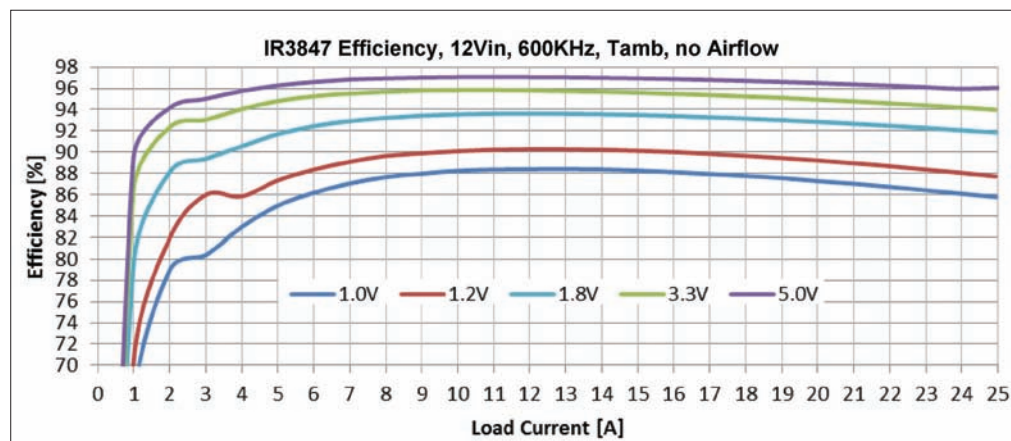
precise threshold which is internally monitored by the Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3847 will turn on only when the voltage at the Enable pin exceeds this threshold, typically 1.2 V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3847 does not turn on until the bus voltage reaches the desired level (see Figure 3). Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold, IR3847 will be enabled. Therefore, in addition to being a logic input pin to enable the IR3847, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the IR3847 to be disabled at least until PVIN exceeds the desired output voltage level. A resistor divider is used at EN pin from PVin to turn on the device at 10.2 V.

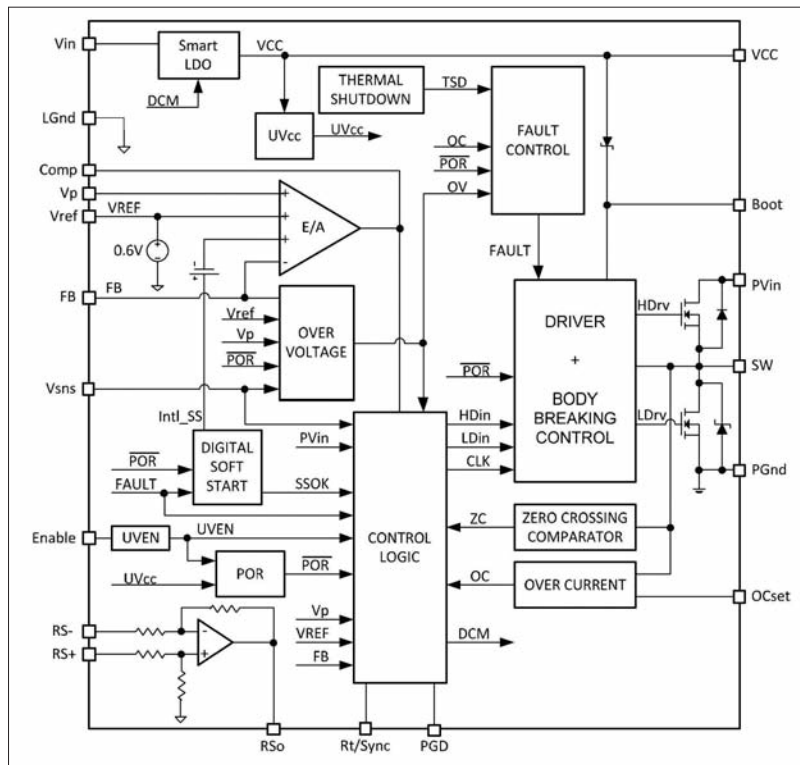
## Pre-bias startup

The device is able to start up into a pre-charged output which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous



**Figure 1:** New POL integrated voltage regulator featuring peak efficiency greater than 96 %



the current surge at start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and  $V_{cc}$  rise above their UVLO thresholds and generate the POR signal. The internal soft-start (Intl\_SS) signal linearly rises with the rate of  $0.4\text{mV}/\mu\text{s}$  from 0 to 1.5 V. Figure 4 shows the waveforms during soft start. During the soft start the over-current protection (OCP) and over-voltage protection (OVP) is enabled to protect the device for any short circuit or over voltage condition.

### Over current protection

The Over Current (OC) protection is performed by sensing the inductor current through the on-resistance of the synchronous MOSFET. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any layout related noise issues. The Over Current (OC) limit can be set to one of three possible settings by floating the OCset pin, by pulling up the OCset pin to  $V_{cc}$ , or pulling down the OCset pin to PGnd. The current limit scheme in the

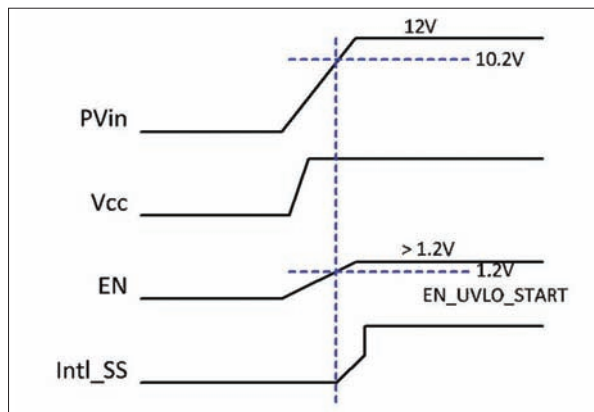
IR3847 uses an internal temperature compensated current source to achieve an almost constant OC limit over temperature.

Over Current Protection circuit senses the inductor current flowing through the synchronous MOSFET. To help minimize false tripping due to noise and transients, inductor current is sampled for about 30 ns on the downward inductor current slope approximately 12.5 % of the switching period before the inductor current valley. However, if the synchronous MOSFET is on for less than 12.5 % of the switching period, the current is sampled approximately 40 ns after the start of the downward slope of the inductor current. When the sampled current is higher than the OC limit, an OC event is detected.

When an Over Current event is detected, the converter enters hiccup mode. Hiccup mode is performed by latching the OC signal and pulling the Intl\_SS signal to ground for 20.48 ms (typ.). OC signal clears after the completion of hiccup mode and the converter attempts to return to the nominal output voltage using a soft start sequence. The converter will repeat hiccup mode and attempt to recover until the overload or short circuit condition is removed.

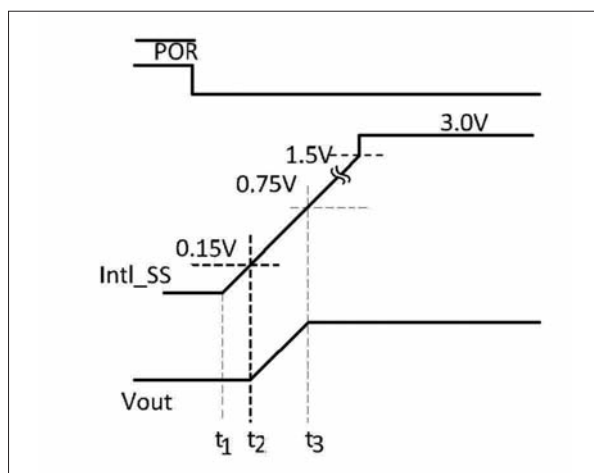
### Over-voltage protection

Over-voltage protection (OVP) is achieved by comparing sense pin voltage  $V_{sns}$  to a preset threshold. In non-tracking mode, OVP threshold can be set at  $1.2 \cdot V_{ref}$ ; in



**ABOVE Figure 2:**  
IR3847 functional block diagram

**LEFT Figure 3:**  
Normal Start up, device turns on when the bus voltage reaches 10.2 V



**LEFT Figure 4:**  
Theoretical operation waveforms during soft-start (non tracking / non sequencing)

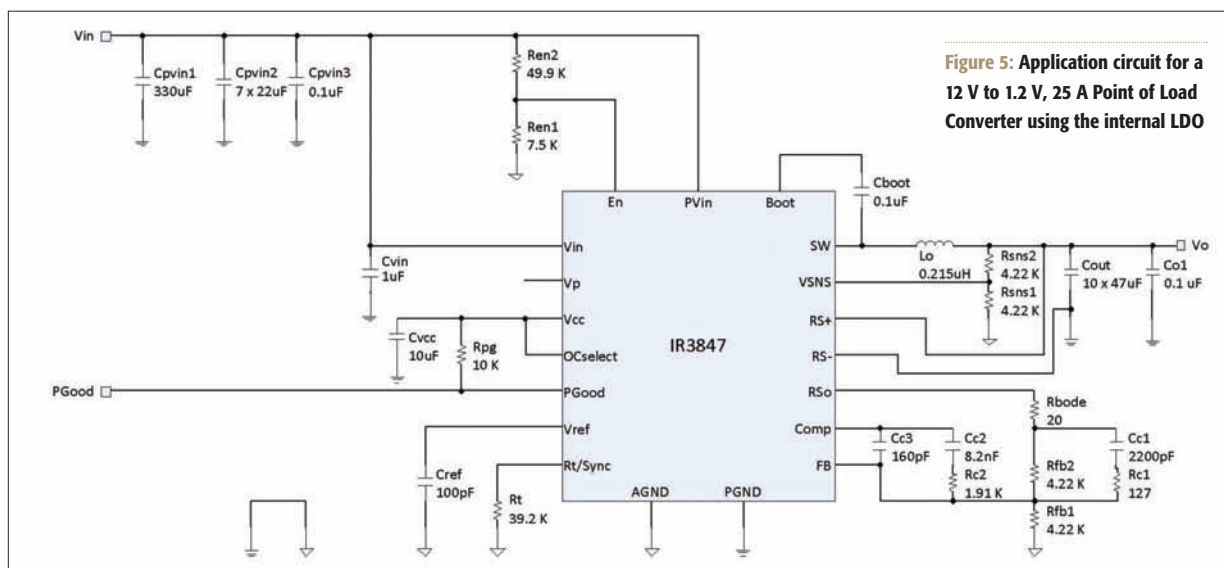
fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. The sync FET always starts with a narrow pulse width (12.5 % of a switching period) and gradually increases its duty cycle with a step of 12.5 % until it

reaches the steady state value. The number of these startup pulses for each step is 16 and it is internally programmed.

### Soft-start

IR3847 has an internal digital soft-start to control the output voltage rise and to limit





**Figure 5: Application circuit for a 12 V to 1.2 V, 25 A Point of Load Converter using the internal LDO**

tracking mode, it can be at  $1.2 \times V_p$ . When  $V_{sns}$  exceeds the over voltage threshold, an over-voltage trip signal asserts after 2.5  $\mu s$  (typ.) delay. The high side drive signal  $HDrv$  is latched off immediately and  $PGood$  flags are set low. The low side drive signal is kept on until the  $V_{sns}$  voltage drops below the threshold.  $HDrv$  remains latched off until a reset is performed by cycling either  $V_{CC}$ . OVP is active when enable is high or low.  $V_{sns}$  voltage is set by

the voltage divider connected to the output and it can be programmed externally.

#### Design example

The design example is a typical application for the IR3847 (see Figure 5) with 12 V input voltage, switching frequency 600 kHz, 1.2 V output voltage, 25 A output current, and  $\pm 1\%$  ripple voltage.

A free user friendly, interactive, web-

based design tool is available at <http://mypower.irf.com/SuplIRBuck> to simplify design and calculate Bill of Materials, schematics, Bode diagram, simulation waveforms and thermal analysis for selected design inputs. The IRDC3847 reference design is also available.


#### Literature

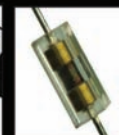
*Preliminary IR3847 datasheet, International Rectifier, March 2013*



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# Power Semiconductors on 300-Millimeter Wafers

In February 2013 Infineon Technologies released the first products of the CoolMOS™ family being produced on its new 300-millimeter line at the Villach site in Austria. The production process based on the new technology has completed qualification and is now ready for delivery. This follows more than three years of intensive research and development activities within Infineon and with partners all over Europe in the fields of process technologies, production technologies as well as handling and automation for advanced power technologies. **Dr. Gerald Deboy, Dr. Kurt Aigner Infineon Technologies, Villach, Austria**

**Due to their larger diameter compared** to standard 200-millimeter wafers, two-and-a-half times as many chips can be made from each wafer. With this massive invest of capital and engineering efforts Infineon Technologies will be able to sustainably support the market with significantly enhanced capacity for leading edge power semiconductor devices.

## The need for efficient power electronics

Power electronics play a major role in harvesting the huge potentials towards a more efficient usage of energy around the globe as outlined in the OECD scenarios in Figure 1. Being more efficient along the generation and conversion chain will be the key enabler to reduce the emission of greenhouse gases.

With an ever increasing contribution of electricity to the global energy mix the importance of power electronics will further grow. Most importantly, power electronics are mandatory to dramatically reduce the huge energy losses that occur between the primary energy source and the energy end use(r). Today, even losses of up to 90 % are seen in the market, with

50 % loss being the norm rather than the exception. Figure 2 depicts the losses from the first conversion into electricity, along the distribution to the final delivery of power to the load in the end user equipment. Modern power semiconductor devices play a vital role to drive power electronics to better performance and lower system costs, thus supporting further proliferation of power electronics into more and more aspects of power conversion and control.

If we take a closer look into the saving potential of various power applications the biggest impact can be reached in motor control applications, where up to 40 % of the electricity is being consumed. The key topic here is to move from on/off control to variable speed drives, which besides the enormous energy saving foster less noise generation and more comfort in e.g. air conditioning applications. A further important focus area are lighting applications with a roughly 15 % contribution to the energy consumption. In lighting mainly the transition from incandescent bulbs and magnetic ballasts, now being widely banned from EU countries to LED lighting and more

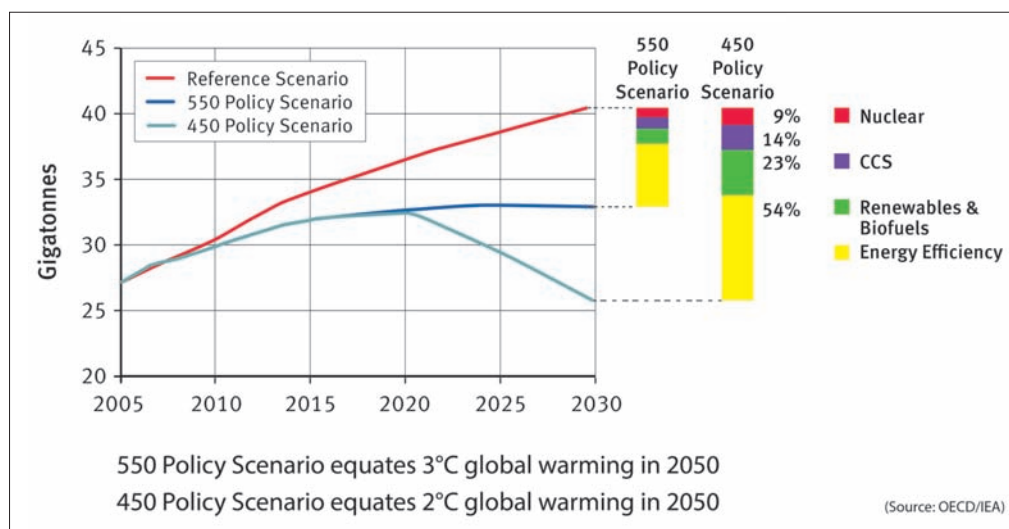
sophisticated electric ballasts drives the saving of energy. Power electronics support these transitions with fitting high voltage MOSFETs, drivers and controllers.

Last but not least power supplies fuelling datacenters and RF telecommunication base stations are indispensable for modern life style with ubiquitous internet access and exchange of data at high speed. Industry has undertaken major steps under the Computing Climate Initiative to set out more and more challenging efficiency targets now culminating in the titanium standard, which will be rolled out with ever increasing share in new IT equipment in the coming years. Key technologies here are mainly high voltage and low voltage MOSFETs ranging from 600 V devices in the AC front end to 25 V in the point-of-load converter.

Strongly growing applications such as photovoltaics (forecasted to 60 GW fresh installations in 2016) and electro mobility will further drive global demand for power semiconductor devices.

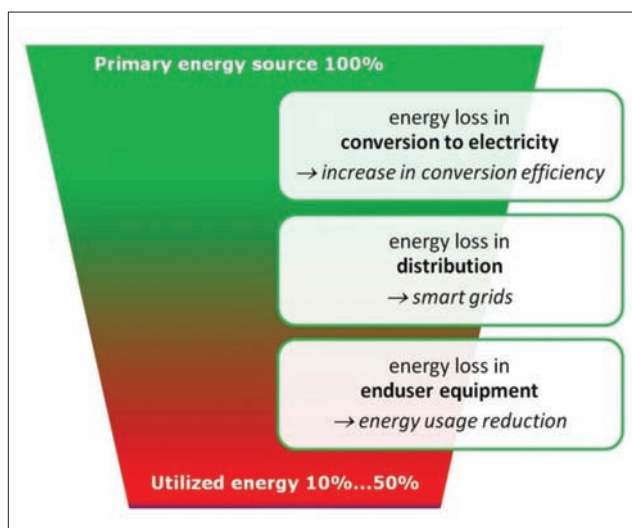
## Power technologies on 300 mm

Infineon Technologies hence undertook as



**Figure 1: CO<sub>2</sub> reduction in different scenarios. The highest CO<sub>2</sub> savings can be gained from increasing energy efficiency**





**Figure 2: Energy losses from the source to the sink are dramatic**

the first power semiconductor company the challenging task to manufacture leading edge power devices on 300 mm wafers. This massive investment of capital and engineering efforts will put Infineon Technologies into a prime position for sustainably delivering production capacity into a power sustainably growing market. Bundling the results of more than three years intensive research with the manufacturing expertise in factories such as Villach and Dresden, Infineon achieved the first customer releases for proprietary CoolMOS™ technology fabricated on 300mm by February 2013.

Infineon Technologies is partner in the EPT300 project [1] – “Enabling Power Technologies on 300 mm wafers” – an ENIAC Joint Undertaking. With the help of EPT300, a consortium of 23 Partners from the European semiconductor manufacturing and the European equipment & materials industries are the first worldwide with a 300 mm power semiconductor processing line dedicated to power device production, realizing leading edge manufacturing capabilities in Europe.

It is important to clearly distinguish power electronics fabrication from conventional CMOS manufacturing technology. Having very different product characteristics, power electronics require different materials and processes, which had not been realized on 300 mm wafers before. The current state-of-the-art in manufacturing power semiconductors (MOSFETs, IGBTs and power IC technologies) today relies worldwide on 150 mm and 200 mm wafer technology. Consequently, today's manufacturing equipment for such applications is specifically designed to these wafer diameters. Technologies dedicated to manufacturing power semiconductors on 300mm wafers require capabilities that in the recent past posed unresolved

manufacturing challenges.

To overcome this limitation, the EPT300 project aimed to provide solutions to the following targets:

- Provide first MOSFET-products fabricated on 300 mm wafers in lead-fab environment in a 1:1 transfer approach to fully prove compliance with application requirements on new substrate material.
- Provide enhanced equipment and new process technologies.
- Prove manufacturability of these products in a high volume production environment with stable and acceptable yield figures.
- Set the technology base for future enhancements in power semiconductor technologies.

The production of power semiconductors is highly complex, involving many production steps requiring in-depth material knowledge and know-how. The first precondition is the availability of proper raw materials and production equipment. Given these, the first manufacturing steps deal with a series of steps in which the active area of the device is built up. Consequent steps are dedicated to semiconductor back-end production, which includes thin-layer metallization and a set of wafer backside process steps that are essential in manufacturing power semiconductors. One key process out of these is wafer thinning, since the thickness of a power device has significant influence on its performance. Infineon Technologies has been pioneering the field of thin wafer manufacturing mainly for its portfolio of IGBTs enabling e.g. the performance of its TRENCHSTOP IGBTs. However, wafer thinning will also be a performance boost for Low voltage MOSFETs and is being used in our CoolMOS technology.

Specific challenges on the way to

300mm manufacturing

In the first step to enable power technologies on 300mm wafers, existing 200mm technologies have to be “transferred”. Nevertheless it is much more than a transfer, because no power base materials were available for 300 mm at project start. Also some equipment for power technologies was not available for 300 mm. In reality it was and still is a challenging R&D project and not a “transfer”.

Therefore it is necessary to prove the 1:1 capabilities of transferred products which are already available on 200 mm. Identical or improved performance of the devices has to be proved.

Out of this, three major challenges are pointed out as a key for the development and production of power on 300mm wafer diameter:

1. Availability of power substrate on 300 mm at a cost efficient level (e.g. Infineon modification of p-type standard substrate, development of 300 mm power substrate by substrate suppliers)
2. Adaptation of 300mm CMOS equipment for power processes (e.g. front side- and back side processing and processing, thick layer processing, high temperature processing and of course thin wafer processing, processing on bridge tools)
3. Thin wafer technology for 300 mm power technologies (adaptations of Infineon's 200 mm thin wafer technology for 300 mm down to 40 µm, enabling 20 µm silicon thickness).

### 300 mm power substrate material challenges

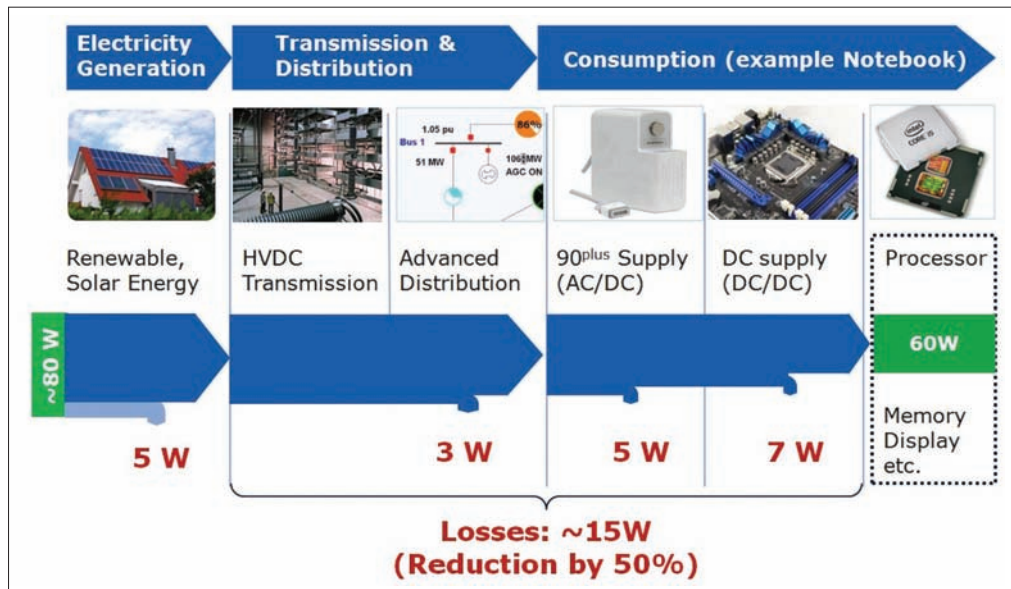
Today, CMOS devices are routinely manufactured on 300 mm substrates, enabling better chip performance at lower costs. While the performance is driven by smaller feature size (<45 nm), the cost per device depends on chip size and wafer

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**Figure 3: Power Semiconductors significantly reduce energy losses**

diameter as well. Still, given the demand volume, the available substrate materials are optimized to the requirements of these CMOS technologies, and do not necessarily allow for the specific requirements of power technologies on the substrate material.

For CMOS-technologies, p-type substrates (mostly Boron) are in use, while power technologies require n-type (typically Phosphor-doping) substrates. Furthermore, the needed doping levels and device thicknesses depend strongly on the desired break down voltage, which created another technological gap that could be solved within the project.

In CMOS technologies, the only active electrical area is located on the surface, whereas in most power technologies the entire silicon volume is used as electric currents flow from top to bottom of the

device. Contaminations and impurities in the substrate thus affect the properties of the devices in a much stronger way than CMOS structures.

Even now, dedicated raw materials for 200mm power technologies are far more expensive than standard materials for advanced CMOS processes. It is essential to find a cost efficient solution for the substrate to maintain the expected cost benefits out of the 300mm wafer diameter.

#### Equipment challenges

The bigger part of the semiconductor market is 300 mm CMOS technology down to 28 nm feature size for mass products like DRAMs, Flash memories or CPUs for PCs, notebooks and smart phones. At the same time, the rapidly growing potential of power technologies

generates a demand that calls for the adoption of 300mm technology also for these devices. However, even though all mainstream equipment for the semiconductor production is now commercially available for 300 mm wafers, there are big differences between mainstream CMOS tools and the special equipment required in power technologies manufacturing.

Compared to CMOS processing the processing of energy efficient power semiconductor requires "3 dimensional processing" (front side processing, back side processing and processing vertically (trenches) in the silicon), thick layer processing, high temperature processing and of course thin wafer technology.

Infineon's high voltage MOSFETs are based on the so-called Superjunction principle, a technology which allows to



**Figure 4: Flexible use of equipment processing 200 mm and 300 mm is crucial**



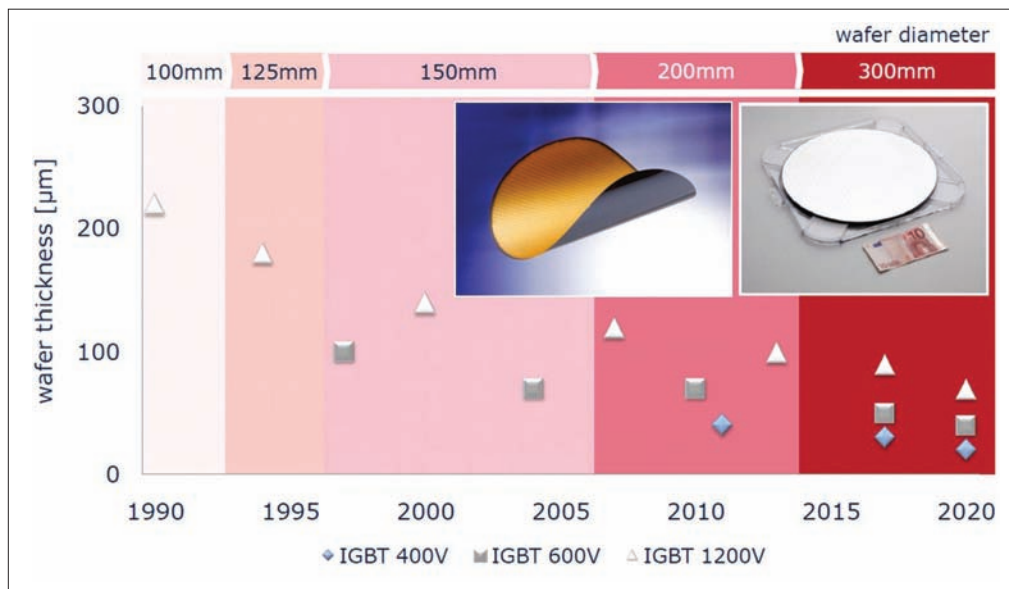


Figure 5: Target wafer thicknesses for IGBTs

drastically reduce the on-state resistance per chip area and to overcome the famous limit line of Silicon. While the on-state performance benefits from an ever higher doping level of the drift region the blocking voltage demands a perfect compensation of three-dimensionally structured p- and n-doped regions across each device, across the entire wafer, from wafer to wafer and from lot to lot. Significant effort is spent on in-line control methods and sophisticated equipment operation and maintenance respectively to successfully transfer the CoolMOS technologies to 300 mm.

Other challenges for power technologies are the high-temperature furnace processes. Standard equipment for 300 mm technologies is capable of processing at a maximum temperature of ~1000°C. Power technologies require temperatures up to ~1200°C. This leads to major research on the hardware of furnaces in order to comply with these challenging requirements. This includes the heating system and sophisticated temperature controllers as well as special, adapted quartz ware technologies.

The flexible use of equipment being capable to process 200 mm and 300 mm wafers (bridge tool) is a key to enable highly flexible and cost competitive manufacturing on European manufacturing sites. Another important aspect of these

bridge tools is the possibility to have an identical 200 mm reference on the same equipment.

#### Thin wafer manufacturing challenges

As outlined above, power devices show vertical current flow, the load current flows from the front to the backside of the device. To optimize the performance the final thickness of a power device is essential. Infineon's IGBT technology relies on extremely shallow p-doped backside implants to control accurately its emitter efficiency. In combination with a less shallow n-doped field-stop layer and the top side trench structure both the distribution of the electric field (and hence the blocking capability) as well as the carrier profile are precisely engineered. Any excess in device thickness would result both in an increase of the forward saturation voltage as well as the turn-off losses. Hence both key performance indicators of an IGBT would be compromised. Figure 5 shows the target wafer thicknesses for the coming years for the respective IGBT voltage classes.

State of the art wafer thickness for 150mm and 200mm wafers for power technologies is today 70 µm. This already implies a huge challenge in the handling of such thin wafers because of their fragility.

Using 300 mm wafers will further increase this challenge, with the trend pointing towards further reductions in the thickness of the wafers. Ultimate wafer thicknesses may be as thin as 20 µm. Other technologies such as Infineon Low Voltage MOSFETs will benefit from the achievements in thin wafer handling to reduce both electrical on-state resistance and thermal resistivity of the remaining substrate thickness.

#### Conclusion

Infineon has shown the successful implementation of power MOSFET technologies on 300 mm wafer manufacturing. The challenges regarding availability of raw material as well as thin wafer manufacturing have been solved. Specific topics such as those posed for Superjunction devices and low voltage MOSFETs have been successfully demonstrated. These achievements will put Infineon Technologies into a pole position to sustainably deliver capacity into a market with ever increasing demand for power semiconductor devices.

[1] A part of the work has been performed in the project EPT300, co-funded by grants from Austria, Germany, The Netherlands, Italy and the ENIAC Joint Undertaking.



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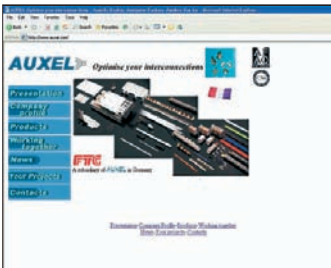
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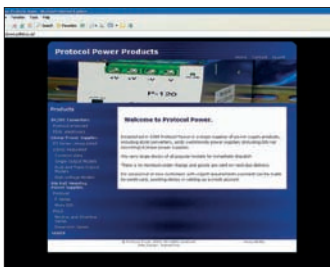
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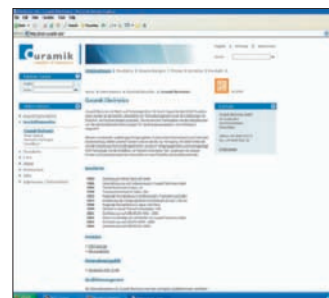
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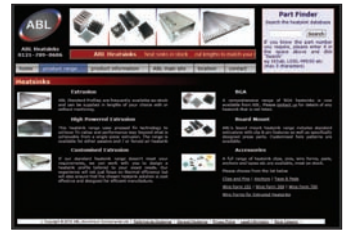
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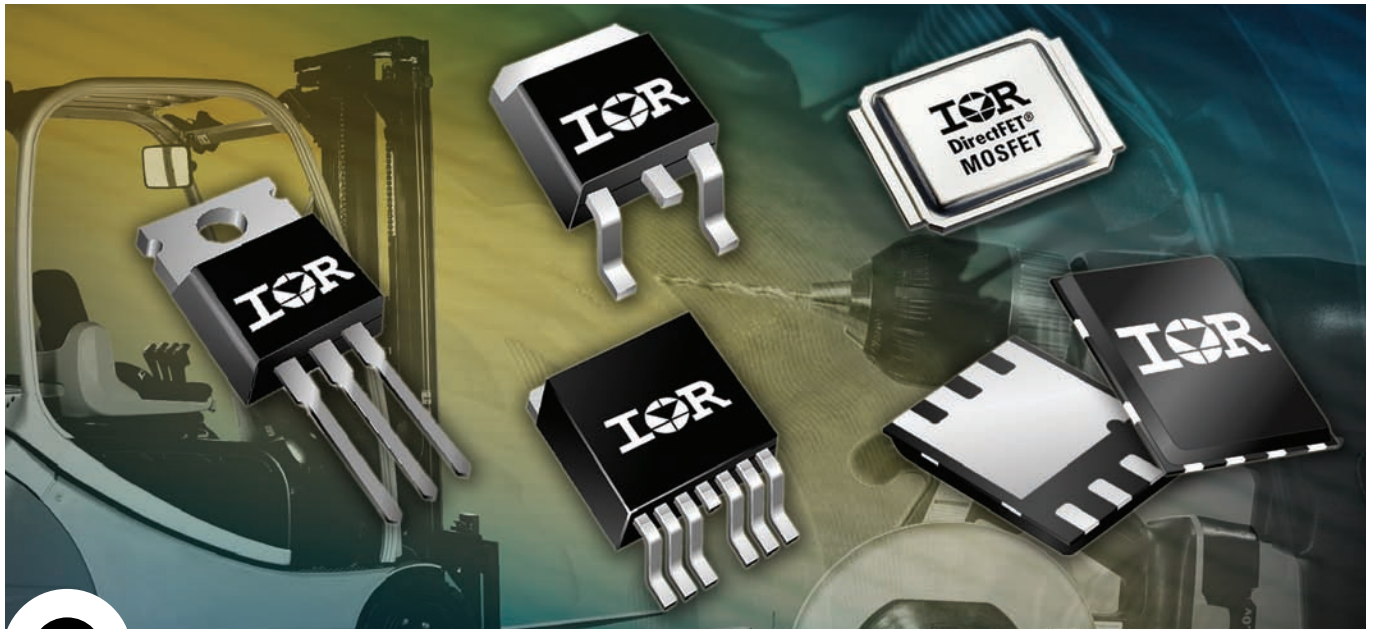
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