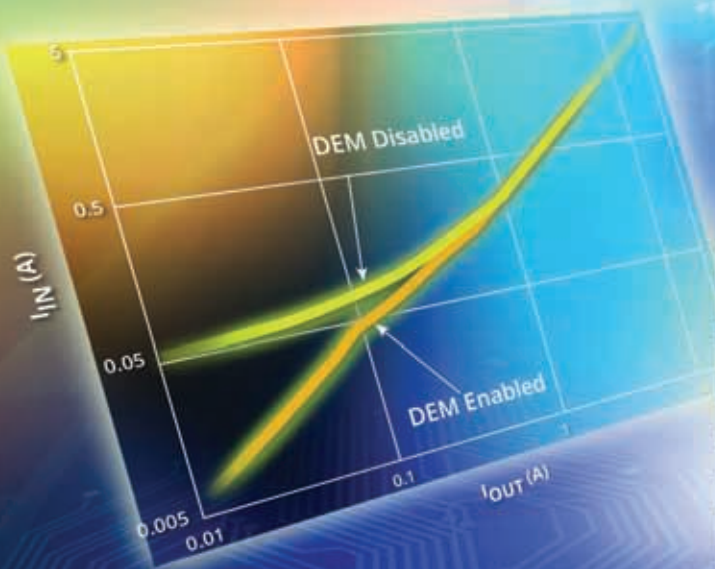


# POWER ELECTRONICS EUROPE

ISSUE 5 – September 2015 [www.power-mag.com](http://www.power-mag.com)

## POWER SUPPLY DESIGN

Improving Buck  
Converter Light-Load  
Efficiency



DIODE EMULATION MODE

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FOR POWER ELECTRONICS  
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Opinion | Market News | Research | Industry News  
SiC Power Led Drivers | Power Supply Design | Digital Power  
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 www.power-mag.com

Circulation and subscription: **Power Electronics Europe** is available for the following subscription charges. **Power Electronics Europe:** annual charge UK/NI £60, overseas \$130, EUR 120; single copies UK/NI £10, overseas US\$32, EUR 25. Contact: DFA Media, 192 The High Street, Tonbridge, Kent TN9 1BE Great Britain. Tel: +44 (0)1732 370340. Fax: +44 (0)1732 360034. Refunds on cancelled subscriptions will only be provided at the Publisher's discretion, unless specifically guaranteed within the terms of subscription offer.

Editorial information should be sent to The Editor, **Power Electronics Europe**, PO Box 340131, 80098 Munich, Germany.

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Printed by: Garnett Dickinson.

ISSN 1748-3530



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## Market News

PEE looks at the latest Market News and company developments

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## Research

### COVER STORY



## Improving Buck Converter Light-Load Efficiency

Intersil introduced its first 60V synchronous buck controller able to bypass the intermediate step-down conversion stage traditionally employed in industrial applications. The ISL8117 synchronous step-down PWM controller's low duty cycle (40 ns minimum on time) and adjustable frequency up to 2 MHz enables the direct step-down conversion from 48 V to a 1V point-of-load. In such applications where a lower output voltage is required, designers have traditionally relied on modules that increase system cost, or two stage DC/DC solutions that decrease efficiency. The controller employs valley current mode control with low side MOSFETs on-resistance, valley current sense and adaptive slope compensation. Its ramp signal adapts to the applied input voltage to improve the line regulation. A unique implementation of valley current mode and the optimized slope compensation resolves the shortcomings of traditional valley current mode controllers. Its control technique allows it to support a very wide range of input and output voltages. In essence, it is a hybrid between voltage and current mode control, displaying advantages of both modulation architectures. If your new buck regulator design requires excellent light-load efficiency, you'll want to consider the selection of a controller or regulator that offers diode emulation mode (DEM). Avoiding DCM conduction loss and reducing unnecessary gate-driver switching losses will help your next power supply design meet its performance specification targets. Full story on page 17.

Cover supplied by Intersil Corp., USA

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## Industry News

PAGE 20

## Next-Gen LED Lighting Designs Driven by SiC Devices

As LED lighting designs move into higher power applications, power electronics engineers can achieve simplified architectures, higher reliability, and lower cost through the benefits of Silicon Carbide power devices. **Marcelo Schupbach, PhD., Technical Marketing Manager, Edgar Ayerbe, Product Marketing Engineer, Wolfspeed (formerly Cree Power & RF), Durham, USA**

PAGE 23

## Zero Voltage Switching Revolutionizes Buck Regulator Performance

Typical point-of-load (POL) applications step down from an intermediate bus voltage, 12 V or lower, to a regulated voltage of a few volts, or increasingly less than a volt. System architects would like to derive stable, regulated power rails for high-current consuming devices (processors and FPGAs) directly from distribution voltages, typically 48 V. Conventional converter limitations preclude doing so because the higher step-down ratio sharply increases power losses; a 2-stage (or more) voltage conversion chain has been the default solution. A significant improvement in efficiency can be delivered by power components that are based upon the ZVS topology. **Robert Gendron, Vice President, Semiconductor Power Solutions, Vicor, Andover, USA**

PAGE 26

## Next Generation in Digital Power Supply Control

The continued adoption of digital control in power conversion and distribution is accredited to the flexibility and increased efficiency it delivers. However, these gains do not come free; they are the result of complex and sophisticated algorithms working at increasingly higher processing speeds in order to optimize the efficiencies of switching power supplies. **Tom Spohrer, Product Marketing Manager MCU16 Division, Microchip Technology, Phoenix, USA**

PAGE 28

## Advantages of Digital Power and PMBus

Power-supply concepts have been well established for many years in the consumer segment, including laptop and desktop PCs, are now increasingly adopted in more industrial applications. The following article gives a detailed description of the advantages provided by digital power supplies, with a special emphasis on the possibilities offered by the PMBus interface. **Hans-Günter Kremser, Principal Field Application Engineer, Texas Instruments, Munich, Germany**

PAGE 30

## Products

Product update.

PAGE 33

## Website Product Locator

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## The Promise of SiC and GaN

Power Electronics Europe reports since its inauguration about new power semiconductor technologies and here in particular Silicon Carbide (SiC) and more recently Gallium Nitride (GaN). After several years of delays and questionings' phase, SiC technology confirms today its added-value, compared to existing Silicon (Si) technologies. Yole Développement (Yole) announces in its latest report GaN and SiC devices for Power Electronics Applications (July 2015 edition) the penetration of SiC, from low to high voltage (600 to 3300 V), in the market segments Power Factor Correction (PFC), photovoltaics, diodes with electric and hybrid electric vehicles (EV/HEV), wind, Uninterruptible Power Supplies (UPS) and motor drives. Under this new technology and market analysis, Yole's analysts point out the emergence of SiC dynamic, especially within the EV/HEV market SiC technology becomes a reality.

In 2014, the SiC chip business was worth more than \$ 133 million. As in previous years, power factor correction (PFC) and photovoltaics (PV) are still the leading applications. Today SiC diodes represent more than 80 % of the global market. Including the growth in both diodes and transistors (MOSFETs), Yole expects the total SiC market to more than treble by 2020.

SiC market leader Cree for instance announced the willingness to spin out its power and RF activities (now named Wolfspeed) and acquired in July the US-based company APEI to strengthen its position in SiC based power modules. This acquisition strengthens Cree's market-leading position for SiC power electronics, infusing the Power and RF business with additional intellectual property and applications expertise at the systems level. The recent acquisition of APEI by Cree will likewise accelerate the development of SiC module packaging. The next event on SiC and GaN is EPE ECCE 2015 in Geneva and ECCE 2015 in Canada. Here 10–25kV SiC Power Modules for Medium Voltage Applications will be

introduced by Dr. Brandon Passmore, development electronics packaging engineering manager at Wolfspeed.

Integrating these fast switching, high operating temperature devices remains one of the major challenges. WBG suppliers and end users need to reconsider many factors, including device packaging, module packaging, gate driver integration and topology design. Packaging is becoming a particular bottleneck, but the good news is that companies are moving in the right direction.

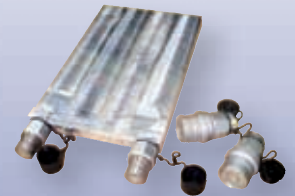
GaN is expected to explode, according to Yole - if challenges are to overcome such as high cost at the device level, reliability, multi-sourcing, and integration. Packaging is becoming a particular bottleneck, but the good news is that companies are moving in the right direction. The project "PowerBase" will improve the ability of the European industry to develop more efficient and more compact applications for energy generation, transformation and usage based on wide bandgap materials. The research and pilot line project "PowerBase" will follow a vertical approach from material research across the entire value chain to "Smart Energy" applications. In this project more than 30 partners from 7 European countries will work together to push Europe into a leading position to manufacture and to apply wide bandgap technologies such as GaN, compact assembly and 3D packaging. GaN device makers EPC and GaN Systems have both adopted advanced packaging, which seems to be more suitable than traditional power device packages. Exagan has raised \$ 6.5 million in first-round financing, to produce high-speed power switching devices on 200 mm wafers, based on GaN technologies. And Transphorm with its \$ 70 million investment round led by global investment firm KKR. WBG companies are so moving in the right direction to overcome the remaining technical challenges and confirm their confidence in these new solutions. These investments reflect the confidence in the GaN device market and investors' willingness to provide funds to accelerate production capabilities.

Numerous companies have now developed SiC MOSFETs, including Cree, Rohm, ST Microelectronics, Mitsubishi and GE. Thus end users are better able to multi-source these devices. By contrast, there's a limited number of suppliers in the GaN market. In coming years, new entrants like Exagan and TSMC will provide extra sourcing options. Infineon and Panasonic also announced in 2015 that they would establish a dual-sourcing relationship for normally-off 600V GaN power devices. And in research, GaN is approaching the kilovolt range – good prospects for the future.

Enjoy reading this issue!

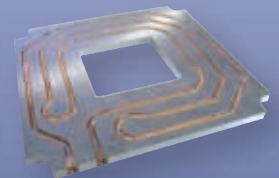
**Achim Scharf**  
PEE Editor

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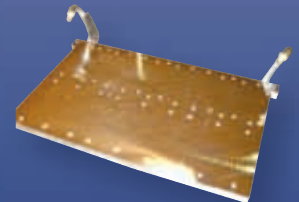
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# The Confidence of the WBG Industry

According to market researcher Yole the SiC market is expected to treble and GaN is expected to explode - if challenges are overcome. Recent financial moves indicate market confidence in WBG devices.

WBG companies are slowly but surely reshaping the industry and accelerate the market adoption with

numerous strategic mergers and acquisitions and the development of disruptive solutions. Infineon Technologies ensures the development of its WBG activities with the introduction of a new Gallium Nitride (GaN) segment - the company acquired International Rectifier in January 2015. Few

months later, Cree announced the willingness to spin out its power and RF activities (under the name of Wolfspeed since September 1) and acquired the US-based company APEI to strengthen its position in SiC based power electronics. Yole also lists huge investments that have been done by the WBG companies.

Latest examples are: Exagan, that raised \$ 6.5 million in first-round financing, to produce high-speed power switching devices on 200 mm wafers, based on GaN technologies. And Transphorm with its \$ 70 million investment round led by global investment firm KKR. WBG companies are so moving in the right direction to overcome the remaining technical challenges and confirm their confidence in these new solutions. These investments reflect the confidence in the GaN device market and investors' willingness to provide funds to accelerate production capabilities.

So far, the WBG market has not grown as fast as people in the business have hoped. The four barriers to WBG device adoption remain: high cost at the device level, reliability, multi-sourcing, and integration. Many R&D programs have been launched in recent years and some prototypes have demonstrated that the cost of the Bill Of Materials (BOM) can be lower at the system level when using WBG devices.

To overcome reliability challenges, ROHM and Cree have announced new SiC device generations or platforms with enhanced, more stable, specifications. SiC and GaN devices are also going through reliability tests to lower their adoption risk. "Numerous companies have now developed SiC MOSFETs, including Cree, Rohm, ST Microelectronics, Mitsubishi and GE" comments Dr. Hong Lin, Technology & Market Analyst at Yole. "This means end users are better able to multi-source these devices. By contrast, there's a limited number of suppliers in the GaN market. In coming years, new entrants like Exagan and TSMC will provide extra sourcing options. Infineon and Panasonic also announced in 2015 that they would establish a dual-sourcing relationship for normally-off 600V GaN power devices."

Integrating these fast switching, high operating temperature devices remains one of the major challenges. WBG suppliers and end users need to reconsider many factors, including device packaging, module packaging, gate driver integration and topology design. Packaging is becoming a particular bottleneck, but the good

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news is that companies are moving in the right direction. GaN device makers EPC and GaN Systems have both adopted advanced packaging, which seems to be more suitable than traditional power device packages. The recent acquisition of APEI by Cree will likewise accelerate the development of SiC module packaging.

The next event on SiC and GaN is EPE ECCE 2015 in Geneva and ECCE 2015 in Montreal from September 20 – 24 (see [www.power-mag.com](http://www.power-mag.com) button events). This seventh Annual IEEE Energy Conversion Congress & Exposition technical will feature breakout sessions, tutorials, keynote speeches, industry expositions and student activities, as well as industry-driven products & services sessions and application-oriented special technical sessions. This will be the first time that ECCE will be held outside of USA.

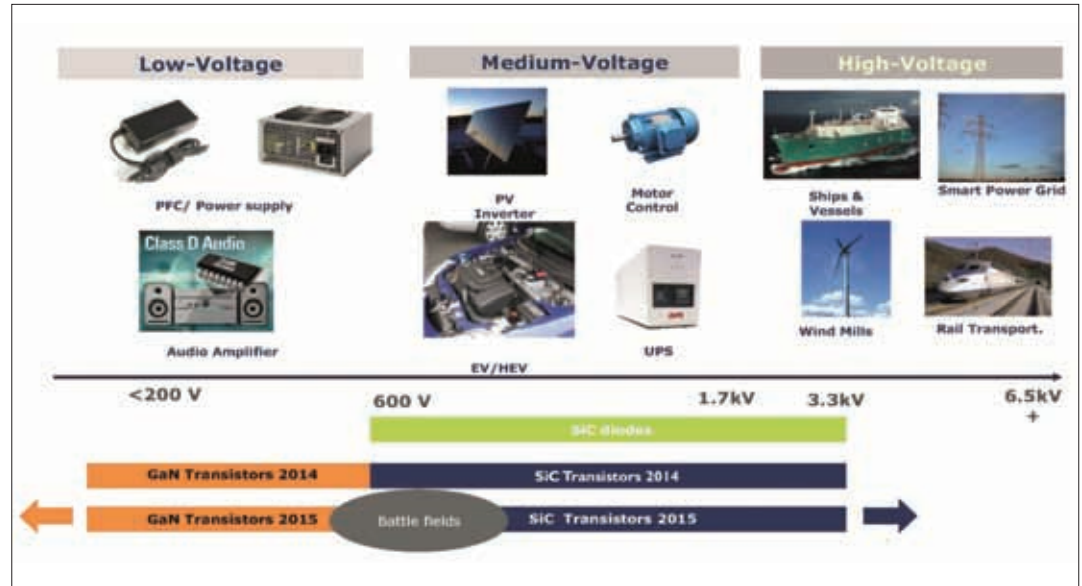
On Monday, September 21, Cree co-founder and CTO of the Power and RF business unit (now Wolfspeed), Dr. John Palmour, will present “SiC Power Devices:

Changing the Dynamics of Power Circuits from 1 to 30kV” during the plenary session. In this talk, Palmour will provide an overview of SiC semiconductors across a wide voltage range, discuss the advantages they provide over Silicon technologies, and refute the

industry’s common cost rebuttal by recontextualizing the price vs. performance data for SiC and Silicon in a system-to-system rather than a component-to-component comparison. Palmour will also briefly discuss a few of the high voltage devices (up to 27 kV) that Cree is

currently developing. Also, 10–25kV SiC Power Modules for Medium Voltage Applications will be introduced by Dr. Brandon Passmore, development electronics packaging engineering manager at Cree.

[www.yole.fr](http://www.yole.fr),



GaN vs SiC as a function of voltage range

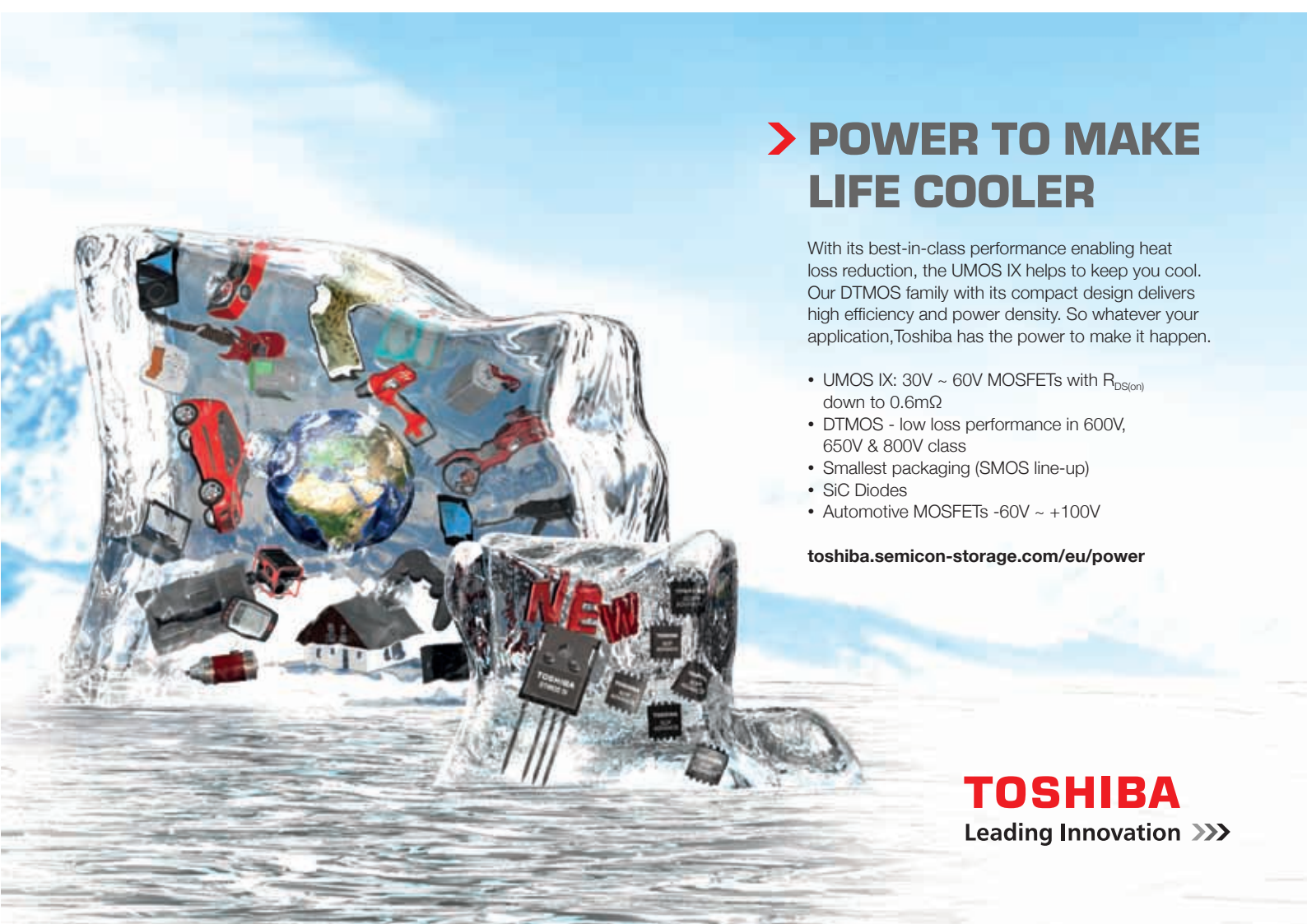
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# Data Center Power Distribution Research Corroborates 400 VAC Adoption

New data reveals that 8.0 % of three-phase, transformer-based power distribution units (PDU) sold into the Americas in 2014 had a distribution voltage of 400 VAC, accounting for \$13.9 million of the \$155.1 million American PDU market.

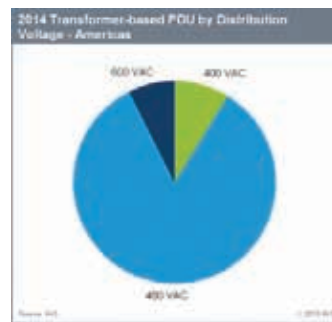
The recently published IHS study, Data Center Power Distribution Report – 2015, quantifies the market for transformer-based PDU, remote power panels (RPP), static transfer switches, branch circuit monitoring, and overhead busway. In this edition, the PDU and RPP categories are segmented by distribution voltage in order to enable IHS to track the trend of 400 VAC power architectures in American data centers.

Although the majority of PDUs sold into the Americas are still 480 VAC, accounting for \$129.8 million in 2014, the adoption of 400 VAC is growing. This new data on transformer-based PDU distribution voltage further supports data from the Rack Power Distribution Units Report – 2015, published earlier this year. In that report, IHS found that 400 VAC rack PDUs accounted for roughly 6 % of the \$418.0 million market. Insights from suppliers of data center power distribution equipment reveal that this shift is currently occurring in new data center builds in North America.

Typically, the power architecture used in a data center depends on the standard voltage of the country in which the data center resides. In North America, parts of Central and South America, Japan, and Saudi Arabia, transformer-based PDUs are typically 480 VAC. The transformer steps down the voltage, and power is delivered to the IT racks at 208/120 VAC. In contrast, much of the rest of the world distributes power through the data center at 400/230 VAC or 415/240 VAC. Data centers in North America have

begun adopting 400 VAC architectures because it requires reduced electrical drops, can lead to electrical and infrastructure savings, and contributes to overall increases in efficiency. This shift in power trends has significant implications for the data center power distribution hardware market and transformer-based PDUs in particular. Depending on the power path in the data center, using a 400VAC architecture could result in either a PDU with a smaller transformer, or the removal of the PDU altogether if the power is to be transformed elsewhere in the power path, like an upstream transformer or at the UPS. Thus, further adoption of 400 VAC could dampen PDU revenue growth, unit growth, or both. However, it could bolster sales of RPPs, which serve the same purpose of distributing power but lack the transformer.

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# Cree Power Goes IPO as Wolfspeed

In May Cree announced that they would be separating the Power and RF business into a standalone company, now this business unit has been named "Wolfspeed".

"Our new name brings together important elements of our culture and expertise. Our new name acknowledges our inception at North Carolina State University and our Cree founders as part of the Wolfpack. The wolf symbolizes intelligence, teamwork, endurance, and the relentless pursuit of innovation we put to work for you every day. Speed is an enabler of our innovation and yours. It's also our promise to you. We are nimble, responsive and hard-charging. We'll make Wolfspeed a new standard for the industry, one by which everyone will be measured", says Jim Gentile, Vice-President, Global Sales. "The new primary color, purple, a combination of red and blue, is representing the strength of our roots (Wolfpack Red and Cree Blue), to create something new and powerful on our strong foundation. But as Wolfspeed, we will remain A Cree Company."

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# Chinese Automotive Semiconductor Revenues to Hit \$6.2 Billion in 2015

The growth rate for vehicle shipments in China is slowing, but more and better performing semiconductors will still be required in automotive applications in the coming years.

Total automotive semiconductor revenue in China reached \$5.6 billion in 2014, and revenues are expected to grow nearly 11 percent year over year in 2015 to reach \$6.2 billion. Semiconductors used in automotive powertrains, infotainment and body-convenience electronic systems are the primary drivers of revenue growth, according to IHS. "There is increasing auto industry focus on power efficiency and green energy, as well as the pursuit of greater safety and a better overall driving experience," said Alex Liu, semiconductors and components analyst for IHS. "For that reason, more and higher performance semiconductors will be required in automotive applications, like direct injection systems in power engines, advanced driver assistance systems and safety applications." According to the latest IHS Automotive Semiconductor Report – China, the leading automotive semiconductor company in 2014 was Freescale, based on bill-to China sales, with 15.5 percent of the market. Freescale is strong in the microcontroller and processor

market, with products that are widely used in automotive powertrains, automotive bodies, and safety and infotainment systems. Freescale was followed by STMicroelectronics, with 14 percent of the 2014 market in China, and NXP Semiconductors, with 12 percent of the market.

Local automotive design market revenue in China was estimated to reach \$1.5 billion in 2014, led by the automotive infotainment category, which includes car radios and navigation systems. IHS expects that the total local design market in China will grow at a 13 percent compound rate from 2014 to 2019. "Local Chinese companies are strong in the automotive aftermarket, because they have a price advantage, require less time to market and have more flexible design processes than their non-local competitors," Liu said. "With the accumulation of technical knowledge, and close ties to original equipment manufacturers, some local players have also gradually entered the applications market. They provide semiconductors for low-end auto-body electronic applications where quality and reliability are less critical, such as parking assistance in advanced driver assistance systems and automotive infotainment."

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# GaN Nanoelectronics Transistor Exceeds 1 kV Blocking Voltage

Low resistance resulting in reduced power consumption and heating have attracted researchers to study GaN systems for nanoelectronics. Previous work has focused on laterally oriented GaN and AlGaN transistors, which readily provide a high mobility and low resistance. However these structures are limited in terms of the break-down and threshold voltage that can be achieved without compromising device size, which may make them unsuitable for automobile applications. Now Tohru Oka and colleagues at the Research and Development Headquarters for TOYODA GOSEI Co., Ltd in Japan show how they can overcome these limitations.

Oka and his team adopted the vertical orientation. Previous work has already shown that in this orientation the breakdown voltage can be increased by increasing the drift region thickness without compromising the device size. However, so far these structures have still been limited in the blocking voltage that the device can withstand while maintaining a low on-resistance.

"We redesigned the thicknesses and doping concentrations of channel and drift layers to reduce the resistances of the epitaxial layers while maintaining a blocking voltage of over 1.2 kV," explain Oka and colleagues in the report of their work. They also use hexagonally shaped trench gates to increase the gate width per unit area thereby reducing the specific on-resistance. "These led to the excellent performance of 1.2-kV-class vertical GaN MOSFETs with a specific on-resistance of less than 2 mΩ cm<sup>2</sup>," they state.

## Technological details

A schematic cross section and a micrograph of the fabricated trench MOSFET with a hexagonal cell structure is shown in the first figure. A n<sup>+</sup>-GaN substrate with a doping concentration of  $1 \times 10^{19}$  cm<sup>-3</sup> and a dislocation density of  $10^6$  cm<sup>-2</sup>. The epitaxial layers were grown on the n<sup>+</sup>-GaN substrate by metal-organic chemical vapor deposition. The layers consist of 0.2 μm n<sup>-</sup>-GaN, 0.7 μm p-GaN, and 13 μm n<sup>-</sup>-GaN. The Si doping concentrations of n<sup>-</sup>-GaN and n<sup>-</sup>-GaN were  $6 \times 10^{18}$  and  $9 \times 10^{15}$  cm<sup>-3</sup>, respectively. The Mg doping concentration of p-GaN was  $2 \times 10^{18}$  cm<sup>-3</sup>.

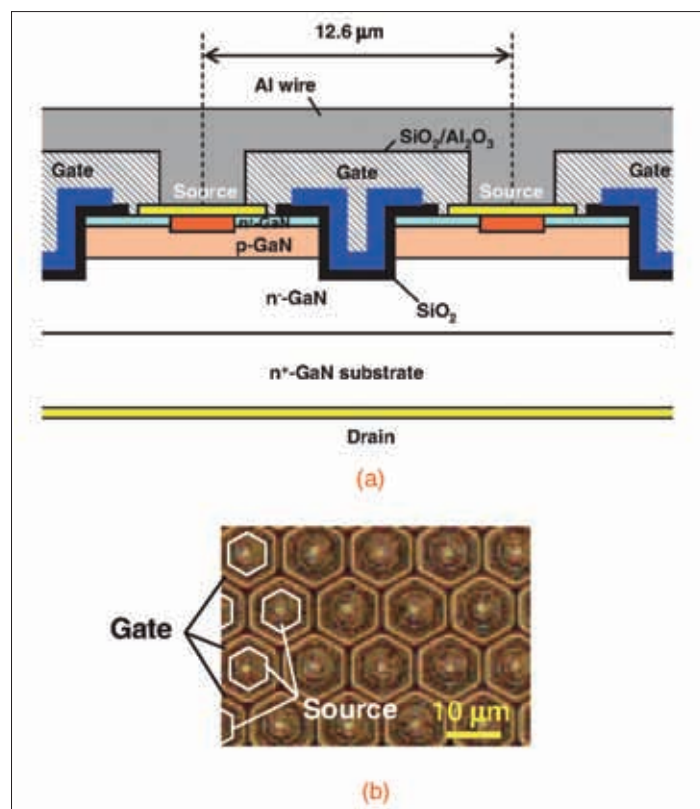
An 80 nm thick SiO<sub>2</sub> film as the gate dielectric was deposited by atomic layer deposition (ALD). The p-body electrode is Pd, and the source and drain electrodes are composed of Ti=Al. The source electrode was stacked on the p-body electrode to miniaturize the cell pitch (distance between the centers of the source electrodes). Annealing was carried out at 550°C for 5 min in N<sub>2</sub> ambient to obtain ohmic contacts. The gate and wiring electrodes consist of Al-based metals. A 100 nm Al<sub>2</sub>O<sub>3</sub> layer formed by ALD and an 800 nm thick SiO<sub>2</sub> formed by plasma-enhanced chemical vapor deposition were used as interlayer dielectrics. Field-plate edge termination around the isolation mesa of the transistor was employed to reduce the potential crowding at the edge of the p-n junction around the isolation mesa periphery.

Regular hexagonal trench gate layout devices, as shown in the lower part of

the illustration. Have been fabricated. Polygonal cells have a definite advantage over stripe cells in the sense that channel density, i.e., the ratio of gate width to unit cell area ( $W_g/S$ ), can be increased, leading to an increase in current density and, thus, a reduction in specific on-resistance. The cell pitch is 12.6 μm.

Normally-off operation with a threshold voltage of 3.5 V was also exhibited. The results demonstrated that the performance of vertical GaN MOSFETs is approaching the best performance of SiC MOSFETs. "Since the cell pitch of the fabricated device is not sufficiently narrow, we consider that further miniaturization of the vertical GaN MOSFETs to as small as the reported SiC MOSFETs will enable us to achieve a specific on-resistance of less than 1 mΩ·cm<sup>2</sup> for 1.2-kV-class devices", Oka concludes.

<http://dx.doi.org/10.7567/APEX.8.054101>



Schematic cross section (a) and micrograph of the fabricated 1.2-kV GaN trench MOSFET (b)

## Infineon Leads European GaN Project

The project "PowerBase" will improve the ability of the European industry to develop more efficient and more compact applications for energy generation, transformation and usage based on wide bandgap materials. The research and pilot line project "PowerBase" will follow a vertical approach from material research across the entire value chain to "Smart Energy" applications represented by PV-inverters, LED lighting systems and energy efficient end-use equipment. In this project more than 30 partners from 7 European countries will work together to push Europe into a leading position to manufacture and to apply wide bandgap technologies such as GaN, compact assembly and 3D packaging.

"Smart Energy" is a key application for industry to address societal

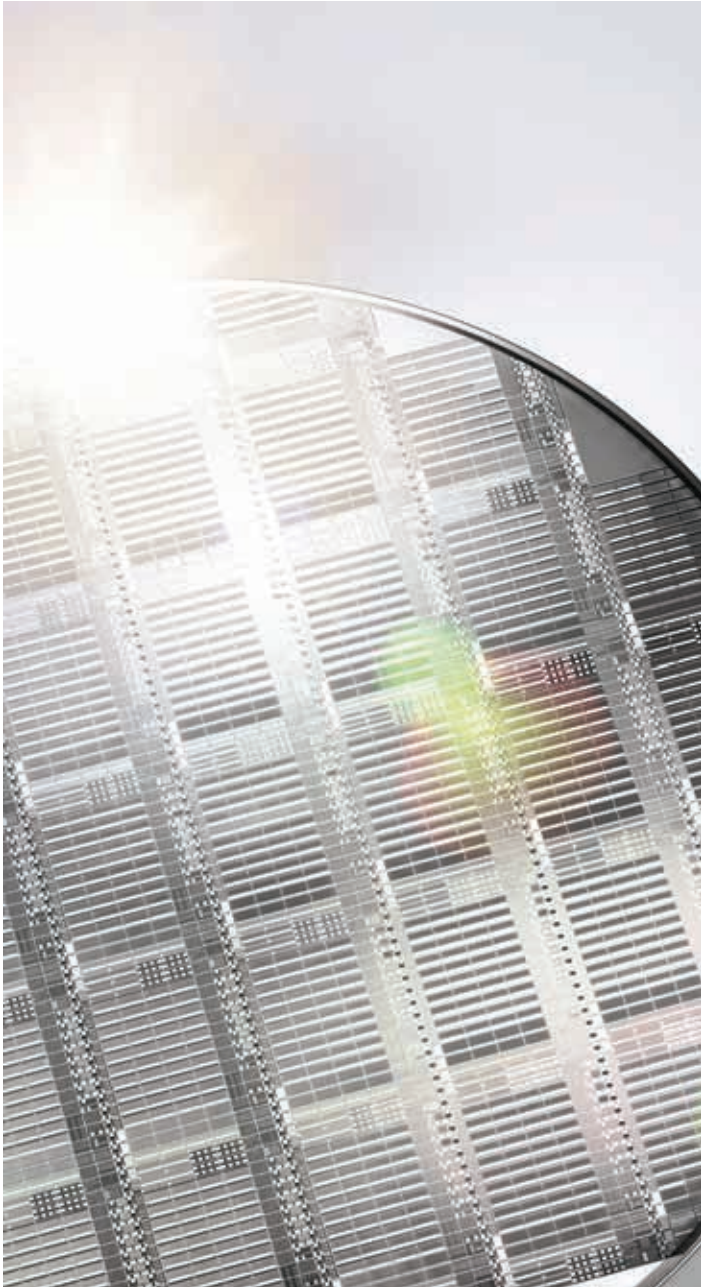
challenges. Wide bandgap based semiconductors are promising candidates enabling higher frequencies and higher efficiencies whenever Silicon based semiconductors reach their limits. In addition compact assembly and packaging including 3D technologies are a prerequisite for "Smart Energy" applications.

The Pilotline "GaN on Si incl. Epi" activities is based on research work on existing base materials. The pilot line concept will be integrated in a high volume Silicon fab to assure a good price performance ratio by better utilization of the standard equipment and significantly lower overhead cost. To reach the next level of GaN devices in terms of crystal defect density (thus enabling higher yields and better reliability) research on novel concepts for

base materials is mandatory and will be performed in parallel. This includes among others novel engineered substrates and buffer layers. Assembly and packaging of GaN is a major roadblock for the success of using GaN for power devices. The properties of GaN can only be properly used when assembly packaging with short interconnects and optimum heat dissipation is applied. This requires completely new approaches: Innovative chip embedding technologies will be investigated for their use in the first two years of the project and then applied to build up the best choice to a pilot line for GaN assembly and packaging in the last year of the project.

The project includes large industry, several SME and world-class research centers that guarantee not only the technical success but also the exploitation of the project results. At least three pilot lines, one for semiconductor front-end technology (GaN/Si technology at Infineon Villach), one pilot line for 3D integrated light sensors (ams AG), and one for GaN assembly and packaging (Infineon Regensburg) shall bring Europe into a leading position. In addition innovations from the equipment and material suppliers as well as from application partners of the project are expected.

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# Reliable and Extremely Long-Lasting High-Voltage Power Modules

How is it possible to increase the dielectric strength and reliability of power modules for medium- and high-voltage applications? Within the APEX research project the Fraunhofer Institute for Integrated Systems and Device Technology IISB in Erlangen/Germany and Rogers Germany (formerly Curamik) developed new construction and testing techniques for high-voltage modules. The project was supported by the German Federal Ministry for Education and Research (BMBF) for over two and a half years with approx. 1.3 million Euros and was coordinated by the Fraunhofer IISB.

Power electronic systems are the key components for an efficient transmission and distribution of electrical power and for ensuring grid stability. The continued decentralization of the energy supply in the medium- and high-voltage sector suggests an increasing demand for breaker cells with an extremely long lifetime of 40 or more years in continuous operation as well as with high dielectric strength. Last but not least, this makes the availability of such components strategically important for the energy industry.

Power modules with voltage classes up to 6.5 kV have become established in industrial drive technology and in rail technology. However, the new applications in energy technology make considerably higher demands of the dielectric strength and reliability of these modules. The main ceramic insulator, the DBC insulating substrate (Direct Bonded Copper) can be regarded as the central component of the power modules. The DBC substrate serves as a circuit carrier and accommodates the electronic power devices. The electrical contacting of the devices and the actual wiring of the circuit take place via a copper layer on the substrate surface that is formed by etching.

## Construction and testing technology for extremely durable high-voltage modules

In the project "Construction and Testing Technology for Extremely Durable High-Voltage Modules" (APEX), it was possible to increase the dielectric strength of currently available DBC insulation ceramics using an optimized module design. In addition to specific material characteristics, the electrical field distribution in and around the insulator is a significant influencing factor, among others. Increases in the electrical field strength especially occur at the edge structures of the etched copper layer. The field increases cause local insulation currents, so-called partial discharges, in the

surrounding insulating material, which can considerably reduce the lifetime of the power modules. The amount of the field increases depends on the applied voltage on the one hand as well as strongly on the geometric form of the edge structure on the other. For this reason, it can be influenced in a relatively cost-neutral way.

To optimize the edge structures, the maximum field strengths that occur on different designs had to be simulated and associated with partial discharge measurements. A comprehensive, simulation-based preliminary investigation of the field strength distribution on the edge structures of the DBCs identified the principal geometric and material-specific influencing factors and allowed a basic theoretical understanding of the interactions. This also required a review of the simulation tools as well as the models used, especially to circumvent so-called unavoidable singularities. In numerical simulation, the modeling of ideal edges can produce excessive values for the field strengths that occur. With the FEM simulation (Finite Element Method) used for this, it is therefore essential to have the right lattice parameters and select suitable measuring points to be able to exclude gross distortions of the calculated field strength distributions.

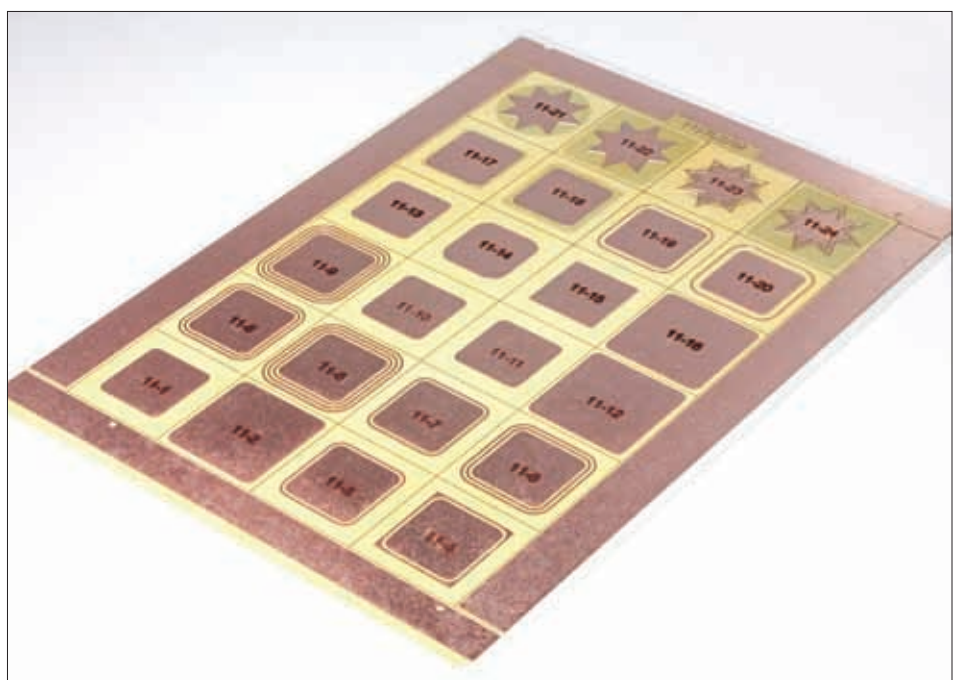
The findings obtained from the simulations

and the newly developed ideas were confirmed by partial discharge measurements on corresponding test designs with adapted edge structures. Thanks to the support of the BMBF, it is now also possible – in addition to purely indirect measurement – to detect the precise point or origin of partial discharges visually using a UV camera system at Fraunhofer IISB.

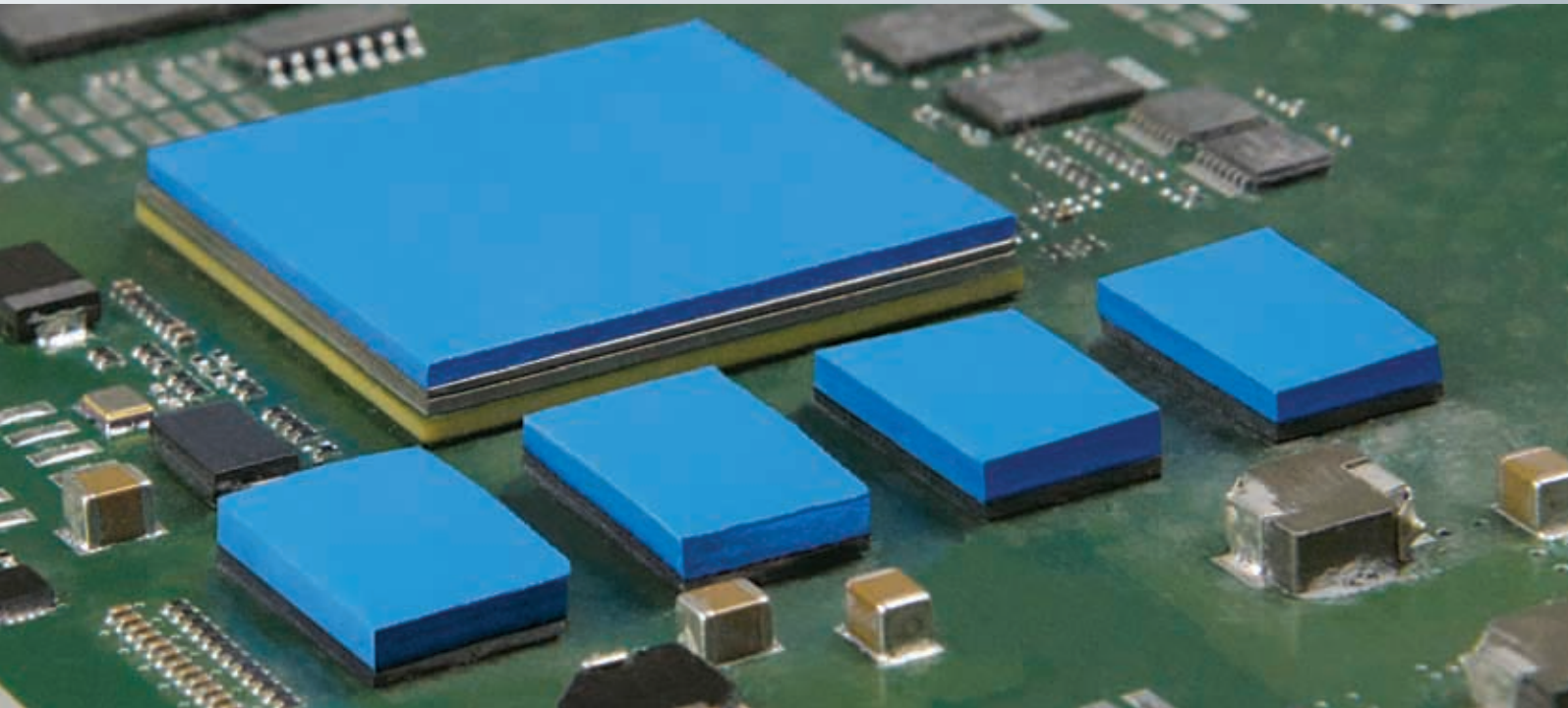
To increase the reliability and lifetime of power modules, tests were also carried out on coating systems in the framework of APEX. Filling microcracks and insulating gaps with suitable inorganic and organic materials considerably increased the mechanical resistance. Accelerated aging tests on module-oriented set-ups in temperature shock cabinets demonstrated the improved thermal fatigue resistance or storage stability of the DBC modules coated in this way.

On the basis of the modifications for DBC power modules studied in APEX, initial prototypes were produced at Rogers Germany. The optimization of the edge structures as well as the coating technology can be used individually or in combination to improve the product characteristics. The methods can be used on existing DBC layouts as well as on standardized power module dimensions.

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# New LED Drivers Bring New Possibilities

LED lighting is a near-mainstream technology. LED lamps that are available in retrofit form factors enable facility managers and building owners to enjoy the benefits of longer operational life and energy savings immediately in buildings using legacy power infrastructures. In those environments where a local area network (LAN) is installed, Power-over-Ethernet (PoE) technology gives an unprecedented ability to dynamically monitor and control each individual LED lamp and smart LED lighting/sensor hub.

Light emitting diodes (LEDs) are semiconductor devices that emit light when an electrical current passes through them. The benefits of using LEDs continue to evolve and mature, making them an increasingly viable choice for legacy and new lighting applications. The benefits of LEDs include a longer operational life, higher energy efficiency (lumens per watt), and tiny size for small form factors. For example, an LED bulb's operational life of 50,000 hours surpasses to far the 2,000 hours for typical incandescent lamps hours and up to 10,000 hours for compact fluorescent lamps.

Consequently, LEDs lights are well suited for many commercial and industrial applications where energy savings are desired, and where access/safety risks and high labor costs inhibit replacing a lamp. The brightness of the light emitted by a 10W LED bulb is roughly equivalent to a 60 W incandescent bulb, making LEDs much lower cost to operate and maintain. LEDs can be used in legacy form factors like MR16; they are ideal replacements for those sockets and provide longer lasting and more energy-efficient lighting. The wavelength, or color, of light that an LED emits depends on the materials used in the construction of the LED.

## LED drivers

With an appropriate driver, LEDs offer more design flexibility for dimming and changing the color of their emitted light. When combined with an appropriate controller and sensor, they can adjust the amount and color of emitted light based on changing conditions within the environment. This capability makes them ideal for applications like indoor lighting, and dimmable street and outdoor lighting that change their brightness as the

ambient lighting changes. Dimming LEDs saves energy at roughly a 1:1 ratio, so dimming an LED to 50 % will save about 50 % of the energy usage.

LED drivers are low-voltage components that convert input-voltage power, such as 120 V, 220 V, or 277 V, to the low voltage that LEDs need. These drivers can also interpret control signals to dim, brighten, and change the color of the emitted light. LED drivers are available in either constant-current (e.g., 350 mA, 700 mA, or 1050 mA) or constant-voltage (usually 12 V or 24 V) implementations. These two types of drivers are not interchangeable. The fixture manufacturer chooses the driver type and configuration to match the electrical requirements of the LED module used in the fixture.

Constant-current drivers support both pulse-width modulation (PWM) and constant-current reduction (CCR) methods for adjusting the output current when dimming the LED. LED applications require a constant current to ensure that the LED light output stays the same even if the input voltage fluctuates. The LED driver not only drives the range of the high- and low-end light level, but also whether the dimming is continuous or stepped. Designers match the driver and LED based on the intersection of a number of application requirements, including the number of LEDs to drive, the type of power supplied, and the functional characteristics of the LED. A poorly matched or implemented LED driver can actually shorten the operational life of the bulb and cause undesirable lighting behavior such as flickering.

Flickering occurs when the amplitude and/or frequency of the light emitted from the LED bulb periodically modulates or fluctuates (undesirably) so that it is visible to the human eye. LEDs are susceptible to flicker when there is a fast change in their light output caused by rapid changes in the input current. Flickering is caused by many sources, including line noise, control noise, component tolerance, and poor LED driver circuit design.

Fitting an LED into an existing form factor, such as the MR16, limits not only the size of the driver board, but also drives the thermal considerations of the design itself.

Because LEDs emit only visible light, they

dissipate more heat through thermal conduction than incandescent or halogen lamps. Thermal dissipation is also one of the limiting factors for the amount of light that a lamp can produce. Today's LED technology in retrofit lamps can barely achieve a level of brightness that is acceptable for the mainstream market. Pushing the limits of brightness and, consequently, thermal design is essential for designing a commercially successful product. A corollary issue to thermal dissipation is the lifetime of the driver board. To emit more light, the lamp must work at a fairly high temperature (+80°C to +100°C). At these temperatures, a poorly implemented driver board that is susceptible to high temperatures can limit the operational lifetime of the whole LED lamp.

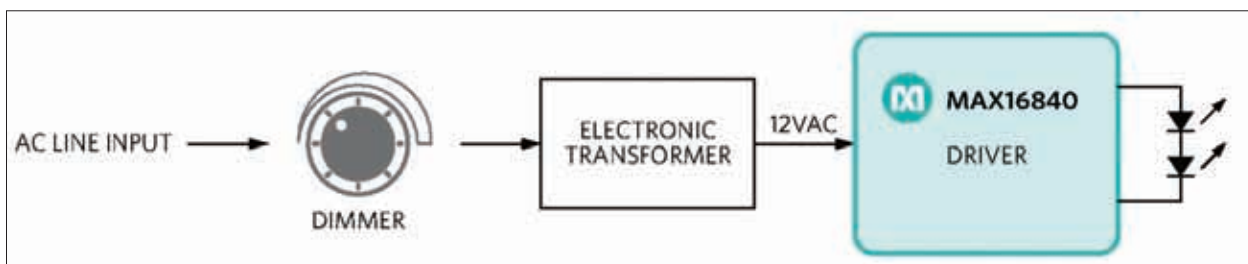
To work electrical correctly within existing form factor, the retrofit lamps must work correctly in LED infrastructures that include cut-angle (triac/leading or trailing edge) dimmers and transformers. Dimmers work well with halogen lamps because the current draw is high enough to ensure that the dimmer stays on. However, an LED retrofit lamp does not allow the triac dimmer to work properly because it provides neither the required start current nor the hold current. As a result, the dimmer does not start properly or turns off while operating, and then the LED lamp flickers.

Electronic transformers have their own design considerations. They require resistive loads, but LED

MR16 bulbs are not resistive loads. Therefore, the loading behavior needs to be modified to keep the electronic transformer from shutting off. One of the biggest obstacles in LED MR16 bulb design is producing bulbs that are dimmable with no flicker and are compatible with electronic transformers. Electronic transformers, while much smaller than traditional magnetic transformers, present a formidable design problem when supplying the lower current required by LED bulbs.

This lower LED current prevents most LED bulbs from operating with electronic transformers. A dimmer adds to this challenge by reducing the current further.

Maxim's MAX16840 LED driver uses a proprietary constant-frequency average current-mode control scheme to solve this problem. It is



The LED driver converts the input voltage to the level that the LED needs

**Connected LEDs integrated with sensors become smart networked hubs**

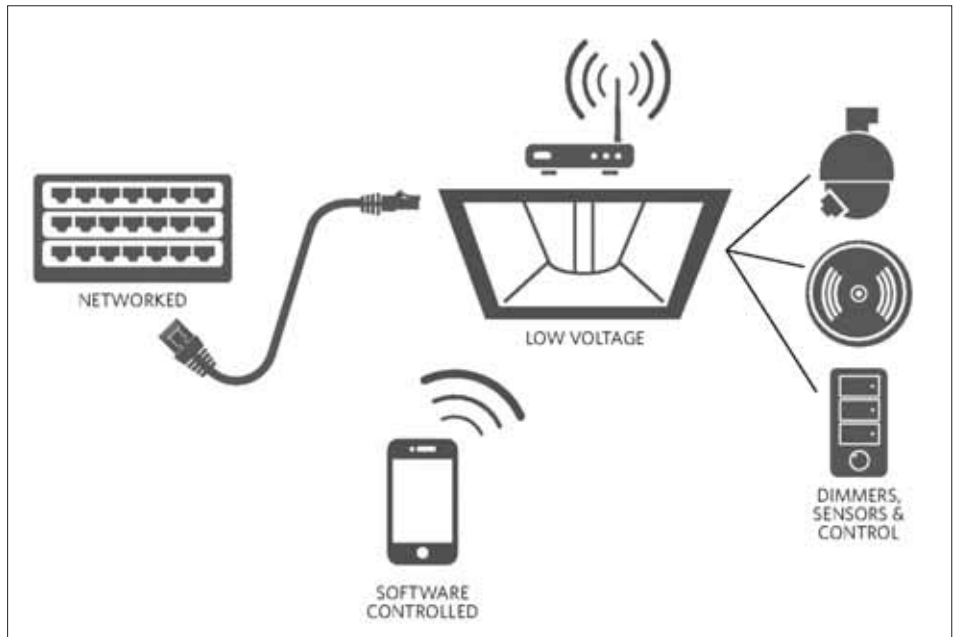
also compatible with most electronic transformers and trailing-edge dimmers.

LED modules in legacy form factors, such as MR16 must operate with the existing, legacy power infrastructure. In contrast, Power-over Ethernet (PoE) LED lighting networks operate on newer or parallel power infrastructures.

**Power over Ethernet**

Additionally, LEDs can be readily paired with sensors, wireless communication modules, and embedded processors. This versatility allows LED light fixtures to become smart networked sensor hubs, and lighting systems can experience energy savings using an isolated local embedded processor. Connecting smart LED lighting/sensor hubs to the local area network (LAN) delivers valuable future-proofing by enabling the installed LED hubs to quickly support and take advantage of emerging capabilities on the IoT (Internet-of-Things) without an expensive lighting replacement.

Power over Ethernet (PoE) is ideally suited for powering, connecting, and controlling smart LED hubs with the LAN. PoE technology is regulated by the IEEE 802.3 standard. It specifies that power and communication data be delivered across a single standard network cable wire (i.e., Cat 5)



directly to the network port of the connected devices. Using PoE lowers the cost of deploying and installing IP-enabled devices, including LED lighting and sensor hubs. Cabling costs are lower because no separate power cable is needed. A PoE network enables better overall network power management, because it provides both discrete control over the power of the connected devices and power backup during power outages with

only the network connection. PoE supports 10BASE-T, 100BASE-TX, and 1000BASE-T networks.

The original PoE standard was released in 2003 and updated in 2009. Power is supplied via power sourcing equipment (PSE) located in the switch/hub. The IEEE 802.3 standard also allows a PSE to be used in a midspan to insert power in the network. This approach supports legacy

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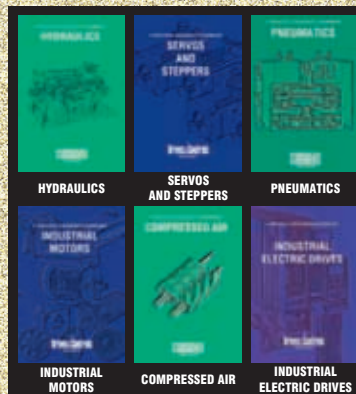
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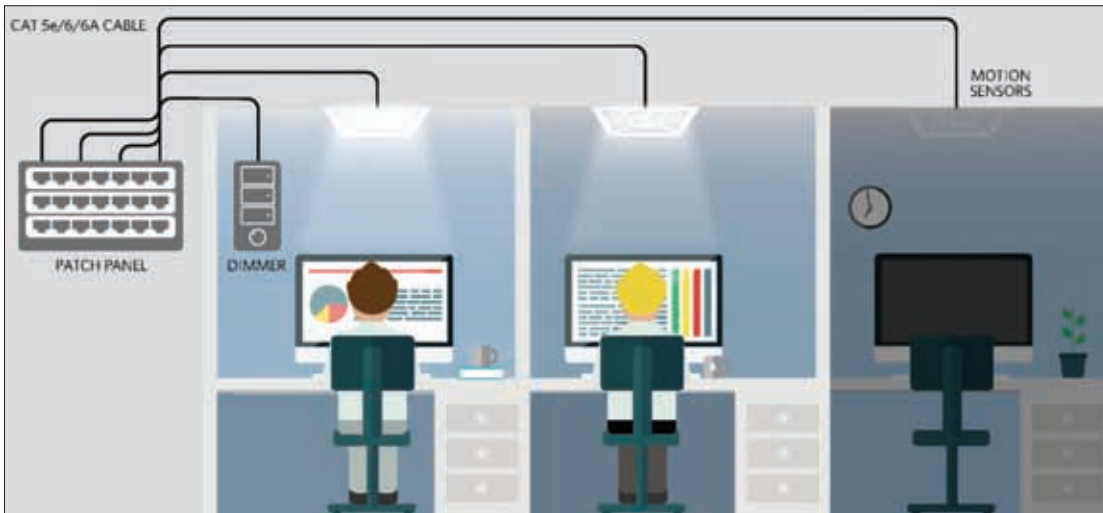
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Networked connected lighting and sensor hubs can deliver new functions anywhere lighting is used

networks and offers more control over which network segments are powered. The connected device receiving the power is commonly referred to as a powered device (PD).

To support legacy installations, the PSE can supply power over two pairs of wires, at a maximum of 15.4 W over a voltage range of 44 VDC to 57 VDC using cat 3 or better cabling. The standard also specifies that the PSE can supply 30 W (over two pairs) or 60 W (over four pairs) over a 50 VDC to 57 VDC voltage range using Cat 5 or better cabling. For these three power scenarios, the PD is limited to a maximum

power draw of 13.0W, 25.5 W, or 51 W, respectively (to account for worst-case power loss in the cable) - all over a 37 VDC to 57 VDC voltage range.

In a PoE configuration, each LED fixture can be a standard RJ45 connector plug-and-play device with its own IP address that is individually addressable. Connecting smart LED hubs (with integrated sensors and wireless access points) via PoE provides power for each LED hub to emit light. The PoE connection also enables each LED hub to collect information from its various sensors and communicate the data back to a

controller.

A PoE LED network provides additional benefits of future proofing, because the LED lighting (and integrated smart sensor hubs) are already positioned where people will gather. If a facility manager wants to add new sensor or communication modules, such as distributed short-range wireless access points, it will be accomplished at low-margin cost because the power and data are already wired to the most useful locations.

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# Improving Buck Converter Light-Load Efficiency

The buck converter switching regulator topology has evolved over the years as designers added new improvements to enhance efficiency and improve overall performance. The purpose of this article is to explain the evolutionary steps of progression and help the power supply designer understand the benefits of diode emulation, which is found in many modern buck controllers and switching regulators.

**Jerome Johnson, Applications Engineer, Intersil Corporation, USA**

Figure 1(a) shows an early buck converter using a diode rectifier during the off state of the main power switch. To achieve higher efficiency, designers modified the buck topology by replacing the diode with a synchronous FET (sync FET) as shown in Figure 1(b). While the sync FET improved efficiency over the diode, it introduced circuit behavior that had undesirable side effects under light load conditions. To overcome these adverse light load effects, diode emulation mode was added to enhance the sync FET design. Figure 2(a) illustrates the single transistor buck controller using a diode rectifier. When the switch is conducting, current builds up in the inductor. The amount of current is

a function of the voltage across the inductor and time the switch is closed (ON time). The ratio of the time the switch is closed (ON) to the time it's open (OFF) is used to regulate the output voltage.

When the switch is open (OFF), the current continues to flow in the inductor as shown in Figure 2(b). When the power switch is off, the diode provides the path for the inductor current. This is a practical solution when the buck regulator is used to regulate higher output voltages. But, with the need for lower output voltages and output currents increasing to higher and higher magnitudes, this has become less practical due to the diode losses. Losses were proportional to the voltage

drop of the diode times the magnitude of the current during the portion of the duty cycle in which the current flowed through the diode. To improve efficiency, the standard diode was replaced with a Schottky diode featuring lower forward voltage drop (approximately 0.4 V versus 0.7 V), but this also has its limits.

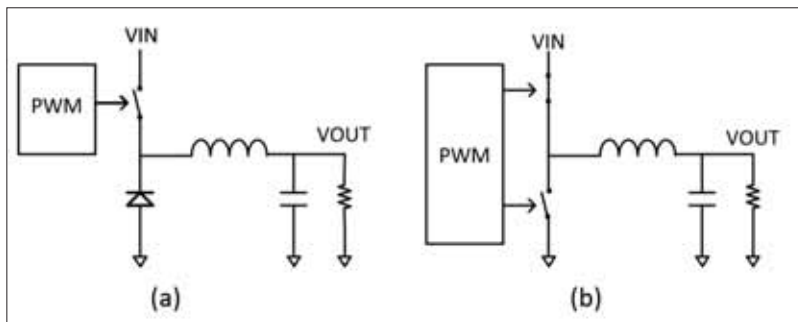
## Synchronous FET advantage

To improve efficiency even further, the diode function was replaced with a FET switch. This FET switch is called a synchronous FET, or sync FET because it is only ON during the OFF time of the main power switch. When the buck converter is switching with nominal output load, the inductor current is always zero or greater as shown in Figure 3.

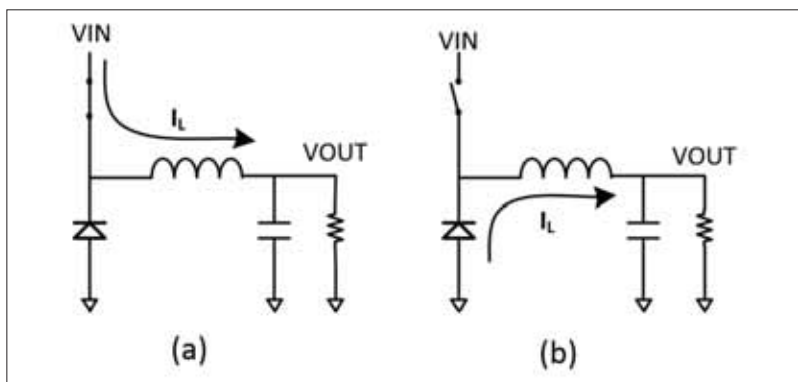
Under normal load conditions, the inductor current is always positive, flowing from the inductor's input side to the output. The current is composed of a DC portion, but it also has an AC component known as the ripple current. When the sum of the DC and AC components' inductor current remains positive for the entire switching period, the converter is said to be operating in continuous-conduction-mode (CCM). However, if the inductor current under light load conditions becomes negative or zero, the converter is operating in discontinuous-conduction-mode (DCM).

In the single switch buck converter, which uses a diode rectifier, the inductor current could never go negative because the diode allowed current flow in only one direction. Therefore, when the converter was under light load conditions, the current during DCM will appear as shown in Figure 4. Figure 5 illustrates what happens when the buck converter's diode is replaced with a sync FET and is operating under light load conditions – the current goes negative.

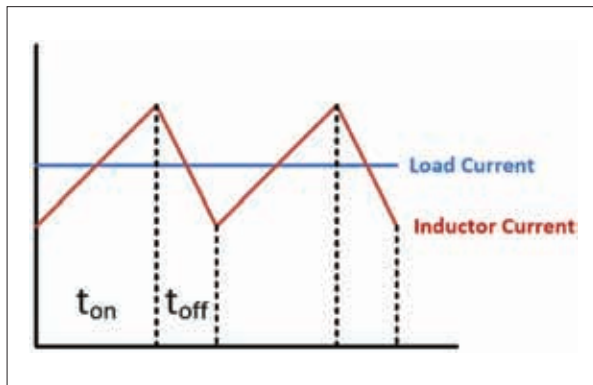
Unlike the standard DC/DC buck regulator with a diode rectifier, the sync



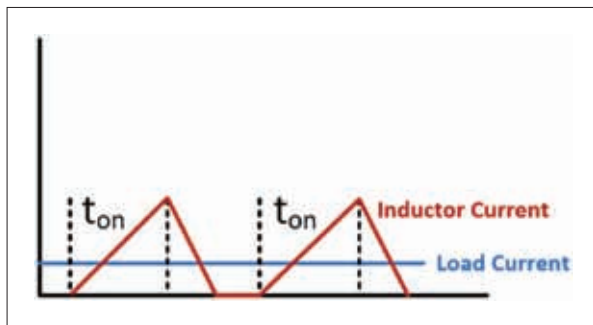
**Figure 1: Buck converter with diode rectifier (a), and (b) buck converter with sync FET**



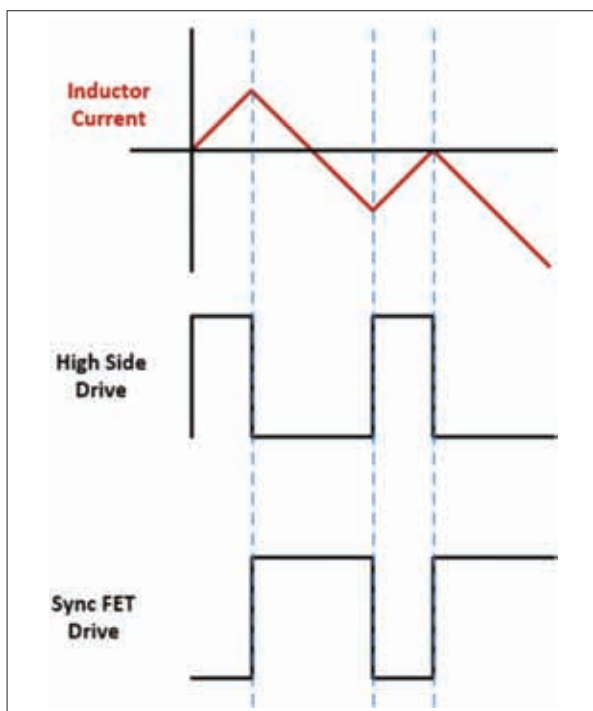
**Figure 2: Single transistor buck controller with diode rectifier (a), and (b) controller with switch open flows current to the inductor**



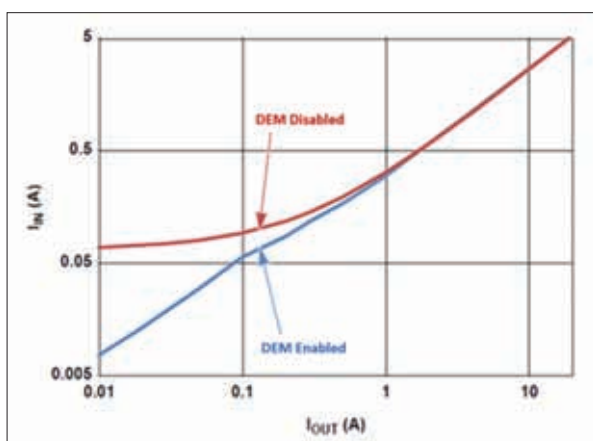
**Figure 3: Buck converter switching with inductor current that is always greater than zero current flow**



**Figure 4: Buck converter in light current load condition operating in DCM**



**Figure 5: Buck converter's sync FET allows negative current flow**



**Figure 6: Input current to the ISL8117 is reduced with DEM enabled**

FET causes the current in the inductor to flow “backwards” during DCM, stealing energy from the output filter capacitor. This behavior reduces the light-load efficiency because of the unnecessary conduction loss as the low-side MOSFET sinks the inductor current when it would be more efficient to prevent this current from flowing at all.

**Diode emulation mode advantage**

Many modern controllers include circuitry that avoids the DCM conduction loss by making the low-side sync FET emulate the current-blocking behavior of a diode. This smart-diode operation is called diode emulation mode (DEM) and functions to turn the sync FET off when the circuitry senses that the inductor current is starting to flow in the wrong direction. This circuitry monitors the voltage across the RDS(ON) of the low-side sync FET and turns off the FET when adverse conditions occur.

For example, the ISL8117 high voltage buck controller ( $V_{IN}$  60 V to 4.5 V,  $V_{OUT}$  54 V to 0.6 V, with an operating frequency of 100 kHz to 2 MHz) offers a mode option in which DEM circuitry can be enabled to enhance light load efficiency. When enabled, the DEM circuitry examines the voltage across the sync FET and activates DEM if it signals that the inductor current is going negative for eight consecutive PWM cycles while the LGATE pin is high (the SYNC FET is ON). Using detection over eight cycles prevents noise from activating DEM. If the ISL8117 enters DEM mode, the switching frequency of the controller will also decrease. Both of these actions increase efficiency by not allowing negative current flow and by reducing unnecessary gate-driver switching losses. The extent of the frequency reduction is proportional to the reduction of load current.

Figure 6 illustrates the reduced input current to the ISL8117 buck regulator circuit when DEM is enabled and when it's not enabled. The data for Figure 6 was taken using the ISL8117 evaluation board with  $V_{IN}$  at 48 V and  $V_{OUT}$  at 12 V configured to support a full-scale 20 A load. The DEM circuitry is used to enhance light-load efficiency.

**Conclusion**

If your buck regulator application requires excellent light-load efficiency, you'll want to consider the selection of a controller or regulator that offers DEM. Avoiding DCM conduction loss and reducing unnecessary gate-driver switching losses will help your next power supply design meet its performance specification targets.

# Synchronous Buck Controller Converts Directly from 48 to 1 V

Intersil introduced its first 60V synchronous buck controller able to bypass the intermediate step-down conversion stage traditionally employed in industrial applications. The ISL8117 synchronous step-down PWM controller's low duty cycle (40 ns minimum on time) and adjustable frequency up to 2 MHz enables the direct step-down conversion from 48 V to a 1V point-of-load. In such applications where a lower output voltage is required, designers have traditionally relied on modules that increase system cost, or two stage DC/DC solutions that decrease efficiency.

The controller employs valley current mode control with low side MOSFETs on-resistance, valley current sense and adaptive slope compensation. Its ramp signal adapts to the applied input voltage to improve the line regulation. A unique implementation of valley current mode and the optimized slope compensation resolves the shortcomings of traditional valley current mode controllers. Its control technique allows it to support a very wide range of input and output voltages. In essence, it is a hybrid between voltage and current mode control, displaying advantages of both modulation architectures.

The ISL8117 can operate from any voltage between 4.5 V and 60 V, and its output can be adjusted from 0.6 V to 54 V. It has an adjustable frequency range of 100 kHz to 2000 kHz and can produce minimum on-time of 40 ns (typical). With a minimum on-time of 40 ns, the controller can generate 1 V output from a 12 V bus at 1.5 MHz. It is also capable of generating a 1 V supply from a 48 V source at

lower frequency. In systems susceptible to a particular switching frequency noise, the ISL8117 can be synchronized to any external frequency source to reduce radiated system noise and beat frequency noise mitigation.

Engineers can design a complete DC/DC buck converter with 10 components, including external power MOSFETs and passives, and achieve up to 98 % conversion efficiency with 1.5 % output voltage accuracy. The DEM/Skipping Mode at light load lowers standby power consumption with consistent output ripple over different load levels. The ISL8117 high voltage controller can be combined with Intersil low dropout linear regulators such as the ISL80136, ISL80138, ISL80101A, and integrated FET switching regulators (ISL8023/24 or ISL8016) to support the bulk power rails in a typical process control industrial application.

The ISL8117 is available in 4mm x 4mm QFN and 6.4mm x 5mm HTSSOP packages. Both packages use an EPAD to improve thermal dissipation and noise immunity. Pricing for the QFN package is \$1.80 and the HTSSOP is \$1.95 in 1k quantities. Two evaluation boards are priced at \$80 – the ISL8117EVAL1Z low power ( $V_{in}$  4.5V-60V and 3.3V<sub>out</sub>/6A), and the ISL8117EVAL2Z high power ( $V_{in}$  18 V-60 V and 12 V<sub>out</sub>/20 A). Two demonstration reference design boards priced at \$60 allow designers to produce low power (factory automation or robotic) and high power (telecom) applications.

[www.intersil.com/products/isl8117](http://www.intersil.com/products/isl8117)



# Next-Gen LED Lighting Designs Driven by SiC Devices

As LED lighting designs move into higher power applications, power electronics engineers can achieve simplified architectures, higher reliability, and lower cost through the benefits of Silicon Carbide power devices. **Marcelo Schupbach, PhD., Technical Marketing Manager, Edgar Ayerbe, Product Marketing Engineer, Wolfspeed (formerly Cree Power & RF), Durham, USA**

When compared to conventional lighting sources, the benefits of solid-state lighting (LEDs) are well documented, and include long life, high efficacy, high light output with no mercury, and much lower thermal characteristics. LEDs are also relatively easy to control; however, as they are increasingly deployed in higher power, higher voltage applications, such as stadium illumination or high bay lighting fixtures, careful consideration must be paid to power architectures and topologies to ensure that they are capable of delivering high reliability, high voltage drivers that contribute to lower overall system weight, volume, complexity, and cost. One especially effective method to achieve these goals is to replace conventional Silicon (Si) switching devices with Silicon Carbide (SiC) power MOSFETs and Schottky diodes when developing these new high power systems.

## LED driver designs are crucial for cost reduction

While converting lighting designs to LEDs helps achieve higher performance and cost reduction, the LED components themselves typically represent just 25 % of the overall system cost. As seen in Figure 1, more significant savings can be achieved in the optics, the thermal management components, and the driver elements of the lighting system. To realize these savings, careful consideration must be given to the topology employed for the power conversion platform of the LED driver, which, in turn, will have implications for the thermal management elements.

When using conventional Si power switching devices (typically MOSFETs or IGBTs) at power levels above 100 W, it is not possible to implement a single-stage topology due to the switching frequency limitations of the Si devices. This forces design engineers to employ two-stage topologies, which increase cost due to their inherently greater complexity and higher part count. An example of this design is shown in the power factor

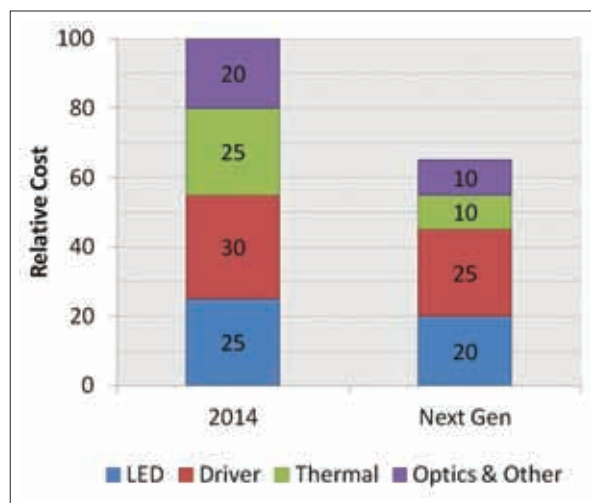


Figure 1: Relative cost comparison of next-generation high-bay lighting

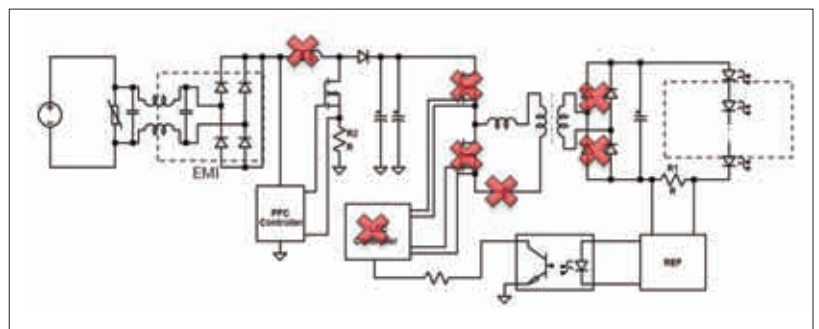


Figure 2: Two-stage driver topology using a boost PFC and LLC half bridge - the red "X" marks illustrate the additional complexity and parts required for a two-stage topology

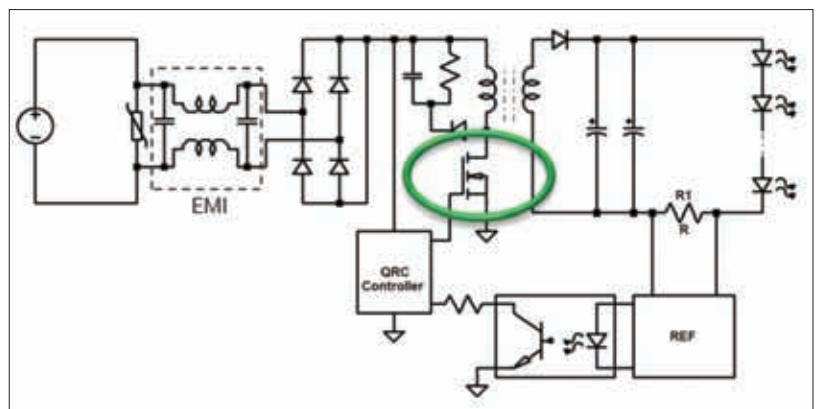


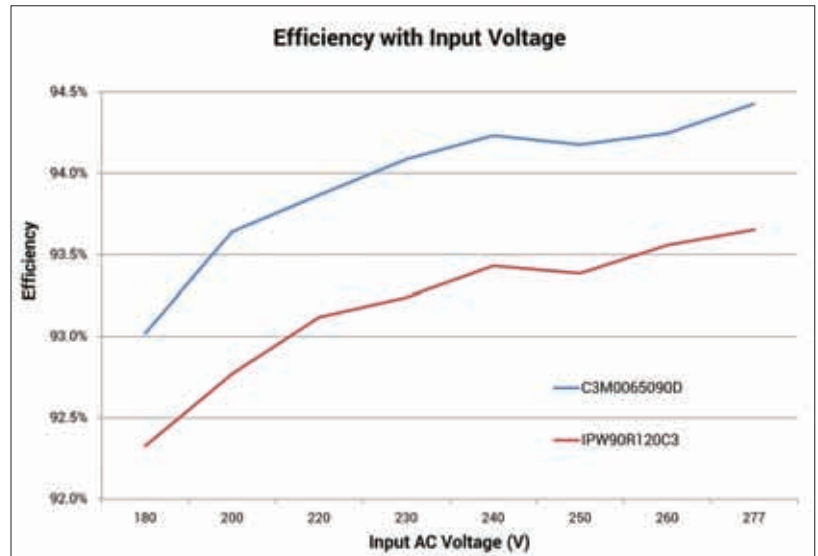
Figure 3: Single-stage flyback-based LED driver topology - the green mark represents the location of the single SiC MOSFET required for a single-stage topology

correction (PFC) boost converter plus LLC resonant half-bridge in Figure 2.

In contrast to the complexity and higher cost of the two-stage topology, a single-stage topology, such as the quasi-resonant flyback shown in Figure 3, delivers lower costs and a simplified design (i.e., lower part count). However, the limitations of traditional silicon switching devices make it impractical to design single-stage topology converters above 100 W. The demands imposed on power MOSFETs are typically higher in single-stage topologies than two-stage topologies, and these demands are further increased when wider input and output voltages are required. These demands have a significant impact on the converter's overall efficiency, the rating of the power MOSFET employed in the design, and, ultimately, the system cost. This is the primary reason why single-stage topologies have previously been limited to low power designs.

However, the latest generation SiC MOSFETs significantly outperforms Si devices, boasting figures of merit (FOM) that are 15–30x better than the best commercially-available 900V Si Superjunction MOSFETs. As such, employing SiC MOSFETs in single-stage topology converters increases their power output by approximately 3x, while delivering efficiencies and operating voltages that are equivalent to those obtained with two-stage Si-based topologies. This enables the design of single-stage topology converters with power up to 250 W–300 W that can deliver performance usually found in two-stage topologies while maintaining the cost structure of a single-stage topology converter.

By employing the latest 900 V SiC MOSFETs, these single-stage LED drivers significantly increase power density by



**Figure 5: Efficiency vs. input voltage of a single-stage flyback driver using a Cree® 900V C3M™ SiC MOSFET vs. a two-stage topology converter using 900V Si MOSFETs**

delivering volume reduction in the 40–50 % range and weight reduction in the 60–75 % range when compared to traditional Silicon-based drivers of similar power output (see Figure 4). These dramatic weight and volume reductions further add to the overall system cost savings, reducing both the size and weight of the mechanical structural components of the light fixture. Through this reduction in complexity and parts count, overall system cost in the converter is on the order of 15–20 %.

Additionally, higher voltage SiC MOSFETs such as the 1200V family can also be used to improve the efficiency and power density of LED drivers with two-stage topologies that are focused on lighting applications with power requirements above 300 W, input voltages up to 528 VAC, or wide input voltage ranges from 90–528 VAC, in addition to lighting drivers

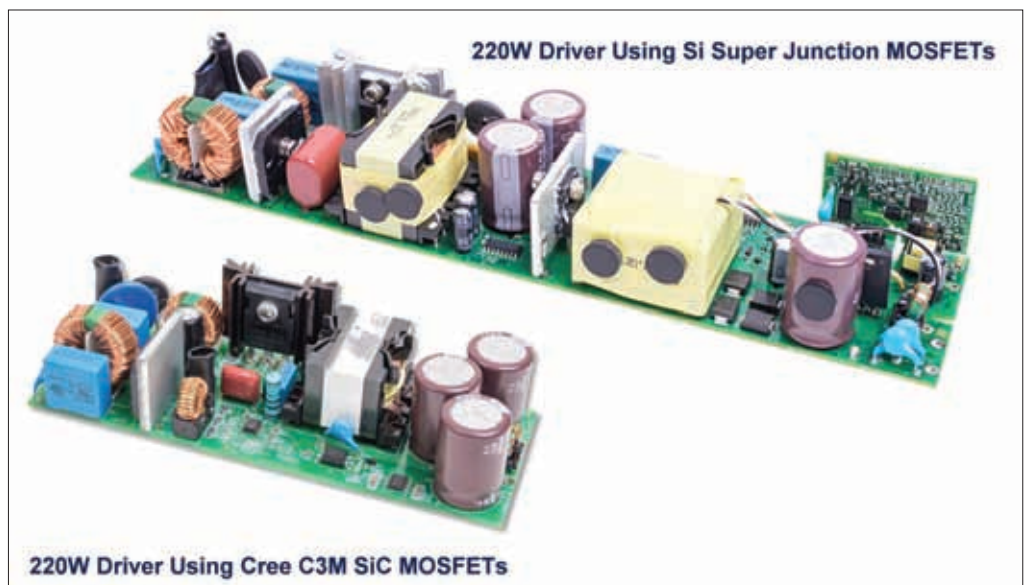
that demand efficiencies of 95 % or higher.

#### SiC MOSFET technology is critical

In many cases, employing SiC MOSFETs as switching devices is one of the keys to overcoming common design limitations when implementing a single-stage topology in a high power LED lighting application. The design of a single-stage topology power converter imposes higher voltage and current stresses to the switching devices than in a two-stage topology design, and these stresses are increased as the input voltage range is widened. The cumulative effect of these stresses impacts the overall converter efficiency, as well as the rating (and hence the cost) of the power MOSFET used in the design.

SiC MOSFETs exhibit superior efficiency over a wider input voltage range than Si

**RIGHT Figure 4:**  
Comparison of 200 W LED drivers: one using Si superjunction MOSFETs in a two-stage topology, the other using a Cree® SiC MOSFET in a single-stage topology



MOSFETs, as shown in Figure 5, which shows the efficiency vs. input voltage of two 220 W LED drivers: a two-stage topology with Si MOSFETs, and a single-stage topology with SiC MOSFETs. Both drivers have equivalent operating voltage windows (120–277 VAC), but the single-stage driver using C3M0065090D SiC MOSFETs exhibits superior efficiency, higher power density, and lower cost.

#### Reducing the cost of EMI filter components

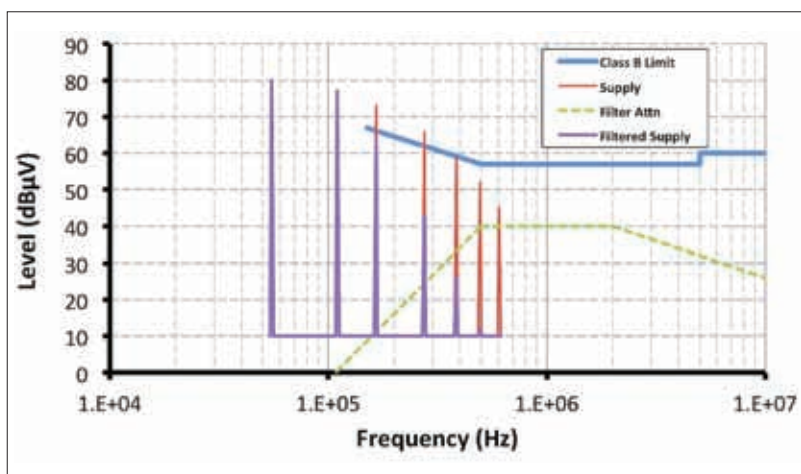
Typically, the EMI signature of a single-stage flyback converter configuration is higher than that of a continuous conduction mode (CCM) boost PFC, and hence requires more expensive EMI filters. However, using a quasi-resonant converter (QRC) flyback configuration with a variable switching frequency generates reduced EMI emission, since it spreads the RF emission over a wider frequency range.

Although the switching frequency of the first stage in a two-stage topology converter is limited to 60–150 kHz to stay within the lower EMI frequency limit (150 kHz), more complex two-stage EMI filters are usually required in the second stage to reduce harmonics for EMI compliance. The higher operating frequency (>200 kHz) that is enabled by SiC MOSFETs with the same EMI filter design delivers significantly improved harmonics, thus enabling this design to reach EMI compliance without additional cost.

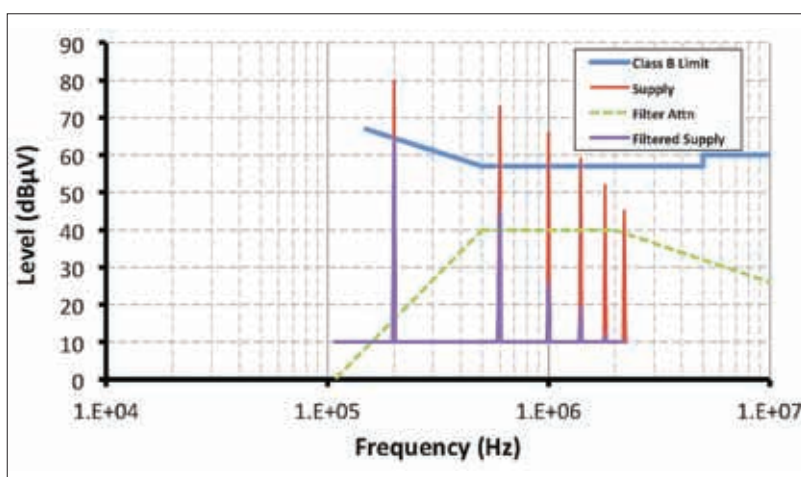
Figure 6 shows the theoretical EMI signature of a two-stage topology converter (Si switching devices) with a DCM boost PFC first stage, while Figure 7 shows the same EMI measurement of a single-stage topology converter (SiC switching devices) using the same EMI filter components.

#### Conclusions

Advances in SiC MOSFET technology have



**Figure 6: Typical EMI filter design for a conventional two-stage converter with Class B conducted EMI limit, theoretical EMI signature of the unfiltered supply (Supply), EMI filter attenuation (Filter Attn), and EMI signature of the filtered supply (Filtered Supply)**



**Figure 7: An EMI filter design for a single-stage high-frequency converter showing Class B conducted EMI limit, theoretical EMI signature of the unfiltered supply (Supply), EMI filter attenuation (Filter Attn), and EMI signature of the filtered supply (Filtered Supply)**

enabled power system designers to take full advantage of the benefits of single-stage topologies in high power lighting applications. With superior performance compared to Si superjunction MOSFETs, SiC MOSFETs have raised the output limit boundaries of single-stage topologies to 250–300 W from the 75–100 W range. New 900 V SiC MOSFETs also significantly increase the value proposition of single-stage topologies for these lighting applications by enabling lower cost, smaller size, and reduced weight. Thus, by employing SiC MOSFETs in single-stage topologies, lighting systems designers can now deliver lower cost designs than two-stage approaches while boosting performance. These single-stage topologies deliver LED driver solutions with comparable performance and lower cost than two-stage topologies at higher power levels using Si switching devices.

Additionally, SiC MOSFET technology is not limited to 150–300 W LED drivers.

Implemented in two-stage topology converter designs, these devices can be used to develop even higher power LED drivers with outputs up to 1,000 W, ultra-wide input voltage ranges up to 528 VAC at the higher end, and efficiencies of 95 % and above, with even high power density. Thus, SiC MOSFET technology is poised to become the device of choice for LED drivers.

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# Zero Voltage Switching Revolutionizes Buck Regulator Performance

Typical point-of-load (POL) applications step down from an intermediate bus voltage, 12 V or lower, to a regulated voltage of a few volts, or increasingly less than a volt. System architects would like to derive stable, regulated power rails for high-current consuming devices (processors and FPGAs) directly from distribution voltages, typically 48 V. Conventional converter limitations preclude doing so because the higher step-down ratio sharply increases power losses; a 2-stage (or more) voltage conversion chain has been the default solution. A significant improvement in efficiency can be delivered by power components that are based upon the ZVS topology. **Robert Gendron, Vice President, Semiconductor Power Solutions, Vicor, Andover, USA**

**Increased losses with high step-down ratios** are largely a consequence of the utilization of “hard” switching, under which MOSFETs turn on or off at high currents and voltages. A new buck topology utilizing Zero Voltage Switching (ZVS) cuts power losses arising from several causes – it reduces switching losses and also cuts gate driving losses, as well as eliminating FET body diode conduction.

The niPOL (non-isolated POL regulator) has benefited from improvements in device packaging, Silicon integration and MOSFET technology. While existing solutions work well over a narrow voltage range, efficiency and throughput power tend to drop somewhat at modest step-down ratios of 10:1 or 12:1. They fall off drastically for a wide input range with a step-ratio approaching 36:1, due to the hard-switched buck regulator’s inherent losses.

Losses in conventional buck topologies can be traced to a number of specific sources; predominantly from hard switching, body diode conduction and gate drive loss, which are described below.

Conduction of high currents while voltage is imposed on a switch – a situation that arises while the device transitions from off to on – causes switching losses proportional to frequency and operating voltage. Improved MOSFET technology and switching speed can reduce the time when current and voltage are simultaneously applied. But this brings its own problems; hard switching usually results in spiking, ringing, and increased EMI. The approach becomes less attractive over a wider operational range requiring higher voltage or frequency.

Losses in the synchronous switch body-

diode occur because there usually is some conduction time when the synchronous MOSFET turns off before the high-side

switch turns on. Body diode conduction requires stored charge accumulated while conducting to be swept away (reverse

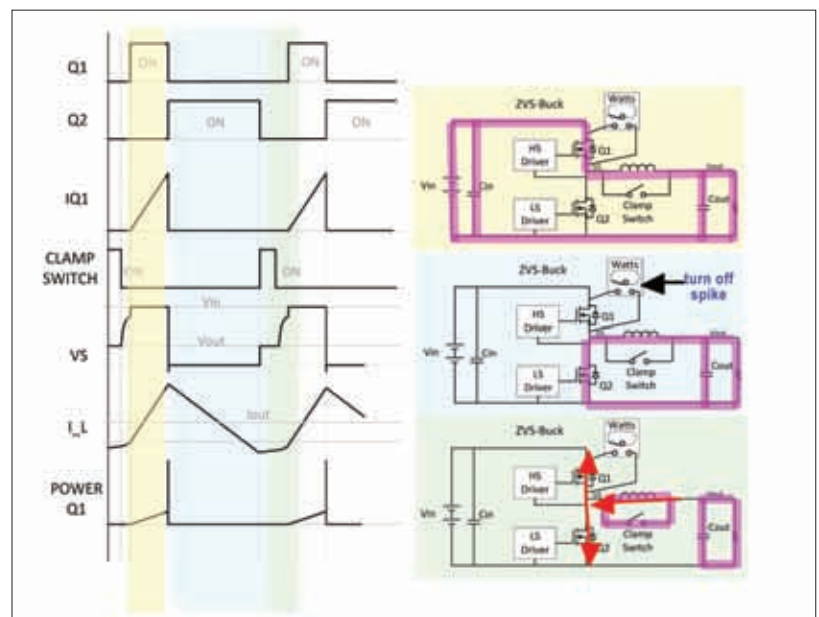
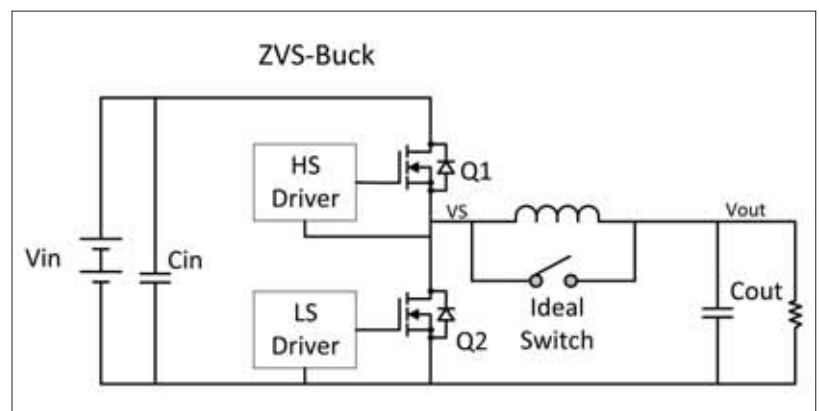


Figure 1; ZVS Buck topology and switching cycle timing diagram

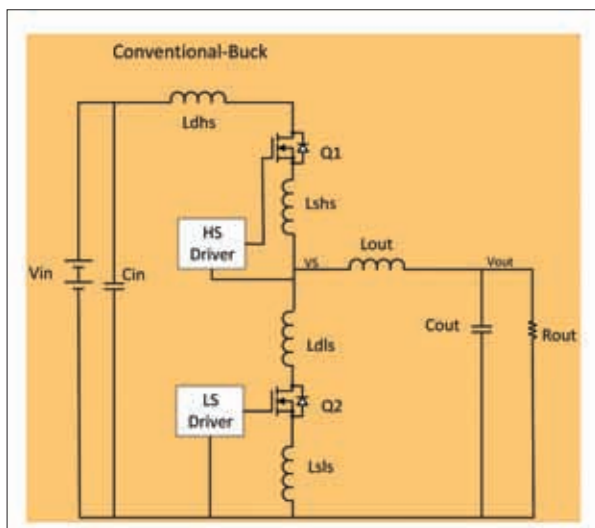


Figure 2: Conventional Buck topology

recovery) before the diode can support any reverse blocking voltage. This causes power losses which are also proportional to the switching frequency.

Each transition of the MOSFET state also takes power from the gate driving stage. The power is the same for each transition, so losses are also proportional to switching frequency.

**ZVS topology**

ZVS Buck Topology (Figure 1) is identical to a conventional buck regulator, except for an added clamp switch across the output inductor: energy stored in the output inductor is directed to ensure that switching takes place under zero-voltage conditions.

The ZVS switching cycle comprises three main states; Q1 on-phase, Q2 on-phase, and clamp phase. After Q1 turns on, current through the output inductor builds from zero to a peak set by Q1's on-time, the voltage across the inductor ( $V_{in} - V_{out}$ ) and the inductor value; energy is stored in the output inductor and charge is supplied to the output capacitor. During the Q1 on-phase, the majority of the power dissipated is in the MOSFET's on-resistance.

Next, Q1 turns off rapidly and Q2 turns on to free-wheel the energy stored in the output inductor

to the load and output capacitor. As there is a series L-C circuit involved, this current will decline as part of the initial stage of its oscillatory behavior and in due course will reverse. As Q1 turns off, there are losses proportional to the peak inductor current.

The ZVS Buck topology fundamentally operates in 'discontinuous mode'. However, a key aspect of its operation is that the synchronous MOSFET Q2 is held on for longer than might otherwise be

expected, beyond the point at which the inductor current passes through zero and reverses. In this short interval of reverse current, (some) energy is again stored in the inductor. The converter's controller sets the level of this accumulated energy at the value needed for the following phase, based on several parameters including input voltage and output load.

When the synchronous MOSFET Q2 finally turns off, the clamp switch turns on to circulate the inductor current and conserve the energy stored in the previous phase. Note that, in this clamp phase, Q2 stays off; there is no body diode conduction and no associated reverse recovery losses.

The clamp switch is opened at the end of the clamp phase, before Q1 is turned on. Now, a different resonance comes into play; the energy stored in the inductor resonates in the tank circuit formed by the output inductor and the paralleled drain-source capacitances of Q1 and Q2, so the VS node sees the first part of a sinusoidal waveform, taking it towards  $V_{in}$ . With

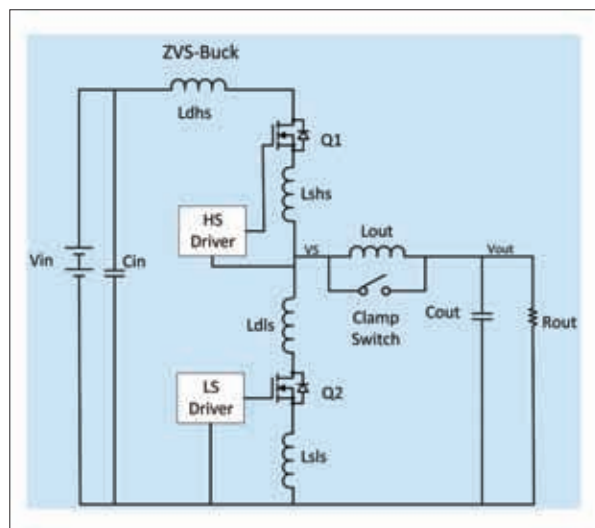


Figure 3: ZVS Buck

suitable timing (calculated by the controller) Q1 is turned on when the VS node is nearly equal to  $V_{in}$ , minimizing switching losses and the Miller effect, due to the small drain-source voltage difference.

The Miller effect is eliminated from the high-side MOSFET at turn-on: the high-side gate driver can be smaller and consume less power. The high-side MOSFET does not have to turn on particularly fast, resulting in smooth waveforms and less noise.

**Conventional vs ZVS Buck operation**

Figures 2 and 3 depict basic conventional and ZVS buck topologies. Figures 4 and 5 show waveforms from steady-state simulations of those circuits with realistic values – for today's packaging and construction – applied in respect of MOSFET package parasitic inductances, and lumped parasitic inductance of the PCB traces. In both cases, the step-down is from 36 V to 12 V at 8 A; the conventional converter has an output inductor of 2  $\mu$ H for a switching frequency of 650 kHz. For

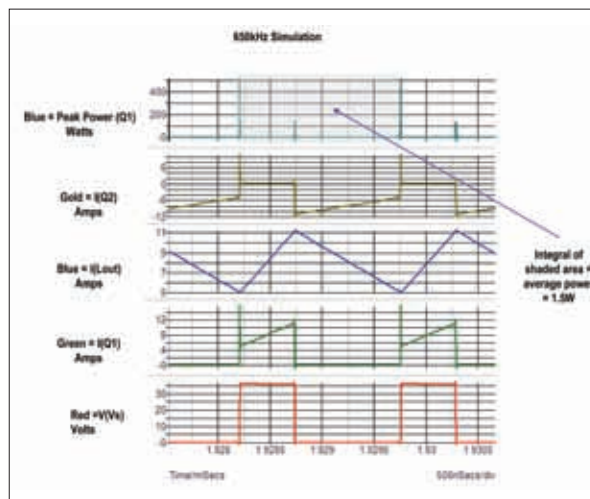


Figure 4: Conventional Buck waveforms



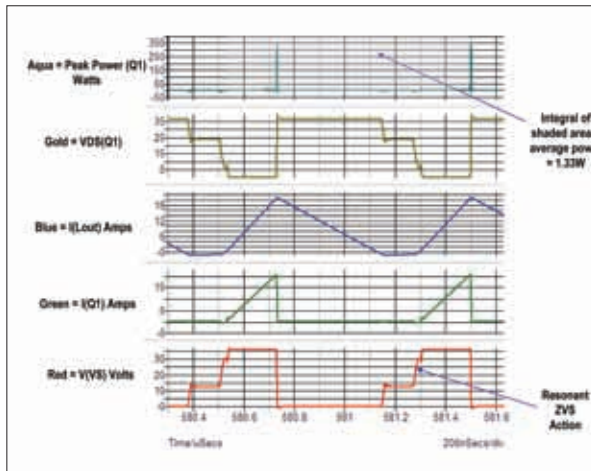


Figure 5: ZVS Buck waveforms

the ZVS Buck the inductor is 230 nH for operation at 1.3 MHz.

Note that in Figure 4 (conventional buck) inductor current is continuous, ranging between 5 A and 11 A: for the ZVS buck, operations is discontinuous, and the reversal of inductor current in the clamping phase is apparent. Figure 4 reveals high losses at turn-on and somewhat lower losses at turn-off, whereas the conduction losses in the MOSFET's on-resistance are quite low. Average power dissipation in the high-side MOSFET is 1.5 W: 0.24 W in conduction, 0.213 W through turn-off and 1.047 W over the turn-on. The turn-on element dominates: Figure 6 expands (time axis) this phase.

To avoid cross conduction, there is a 30 ns dead time between Q2 turning off and Q1 turning on; during this time, the body diode of Q2 is forward biased and it carries the current freewheeling through the output inductor. When Q1 turns on, that body diode must go through reverse recovery, before it can block the reverse voltage. This accounts for the current spike in Q1, which simultaneously sees a large  $V_{DS}$ , almost equal to  $V_{in}$ : hence the large power loss. Further effects, due to parasitic inductances, also contribute.

### ZVS Buck

The simulation shows that at 1.3 MHz the average power dissipation in the high-side MOSFET Q1, including switching losses and conduction losses, is 1.33 W. This is lower than the conventional regulator despite operation at twice the switching frequency and a much smaller inductor. Figure 5 also confirms that as the voltage across Q1 has been contrived to be nearly zero as it is turned on, the associated losses are virtually zero: also, there is no body diode conduction prior to the turn-on of Q1 and no reverse recovery effects, including reverse recovery loss in the body diode of Q2.

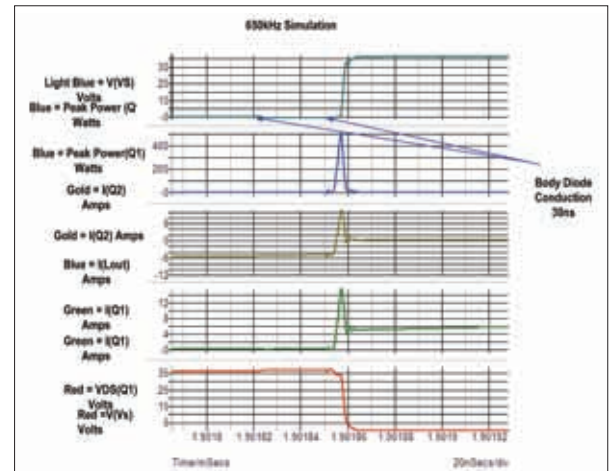


Figure 6: Detailed waveforms for Q1 turn-on

The PI33XX family (Figure 7) of wide input range DC/DC regulators is configured using ZVS topology and Picor's high performance Silicon controller architecture. The 10 mm x 14 mm SiP package requires only the output inductor and a few ceramic capacitors to form a complete buck converter. The family supports wide input range of 8 V – 36 V, to outputs from 1 V to 15 V, at high power and efficiency. As noted above, the inductor can be small and the switching frequency high, typically allowing 120 W to be output from 25 mm x 21.5 mm PCB area with 98 % peak efficiency.

The converter's discontinuous operation allows efficient operation with 20 ns minimum on-time, overcoming limitations on step-down ratios. This addresses the requirement to reduce the number of conversion stages in power distribution. A buck converter capable of supplying point-of-load directly from a 48V rail, going up to 60 V, is now a practical proposition. Figure 8 shows an efficiency curve for a 48 V to 2.5 V ZVS

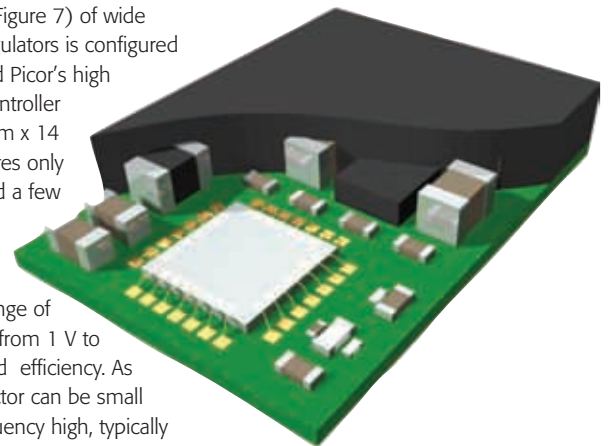


Figure 7: Construction of the PI33XX family of DC/DC converters

buck, at 10 A output. Even at the maximum input voltage of 60 V, the efficiency curve stays above 92 % and peaks up to 94 % above 50 % load.

These performance figures represent a significant improvement over conventional buck converter, demonstrating the significant improvement in efficiency delivered by power components that are based upon the ZVS topology.

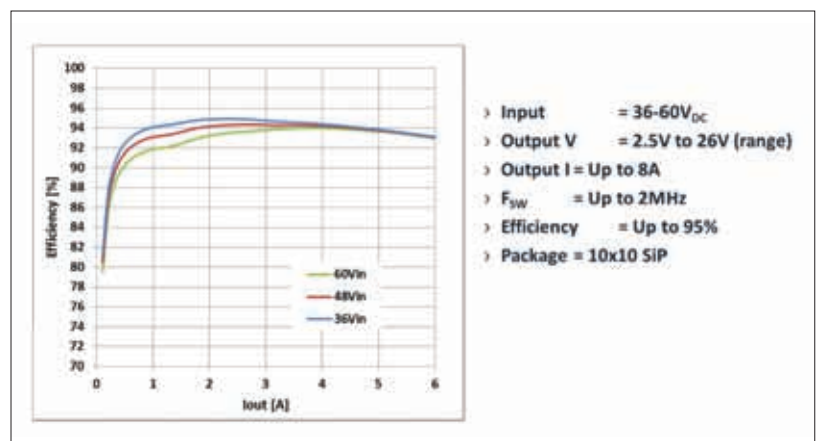


Figure 8: PI3501 efficiency curves (provisional results)

# Next Generation in Digital Power Supply Control

The continued adoption of digital control in power conversion and distribution is accredited to the flexibility and increased efficiency it delivers. However, these gains do not come free; they are the result of complex and sophisticated algorithms working at increasingly higher processing speeds in order to optimize the efficiencies of switching power supplies. **Tom Spohrer, Product Marketing Manager MCU16 Division, Microchip Technology, Phoenix, USA**

**The optimization of switch-mode power supplies** is increasingly seen as a significant opportunity for manufacturers to deliver more efficiency in end-products. The challenge, however, is maintaining that efficient operation across a wide and varying array of load conditions. The introduction of Power Factor Correction (PFC) introduced a new age of efficiency targets – both regulatory and market-driven – and it has become a major focus for semiconductor providers, striving to continually improve their solutions to digital power control. Software-based algorithms provide the potential for more flexible and efficiency solutions, when coupled to the right hardware.

## Digital control

Power conversion invariably starts with an AC source, which is then rectified to DC and further stepped down through various intermediate voltages until eventually reaching the Point of Load (POL). The

Power Factor of a system is the ratio between the true and apparent power; the closer to unity the ratio the more efficient the system. PFC is the method employed to restore the ratio to unity (or as close as possible) and may be achieved using capacitors, but it is increasingly viable to apply PFC using Buck, Boost or Buck/Boost conversion under digital control. Moving between the analog and digital domains typically adds additional latency; the control loop delay, and it describes the total time taken to apply a change to the conversion and measure the effects of that change. Under steady-state conditions this would be relatively simple but under variable loads the speed with which the control loop executes directly influences the PFC and overall efficiency.

The challenge increases when the POL stage requires low voltage but high current levels, as is often the case in modern embedded systems. Today,

microprocessors, FPGAs and ASIC invariably operate from low voltages – 3.3 V and below – but require much higher current in order to meet their overall power demands. Furthermore, the demands will vary significantly based on the operating requirements. As shown in Figure 1, the use of digital control can be applied throughout the entire power conversion flow in order to introduce not only greater efficiency but the flexibility to sustain that efficiency across a wide range of loads.

This is enabled through the continued development of sophisticated algorithms, including adaptive algorithms that can react to changes in load levels, and non-linear and predictive algorithms that can improve the dynamic response under transient conditions. And as semiconductor technology develops, manufacturers are able to employ this to increase the performance of digital control solutions, allowing higher switching

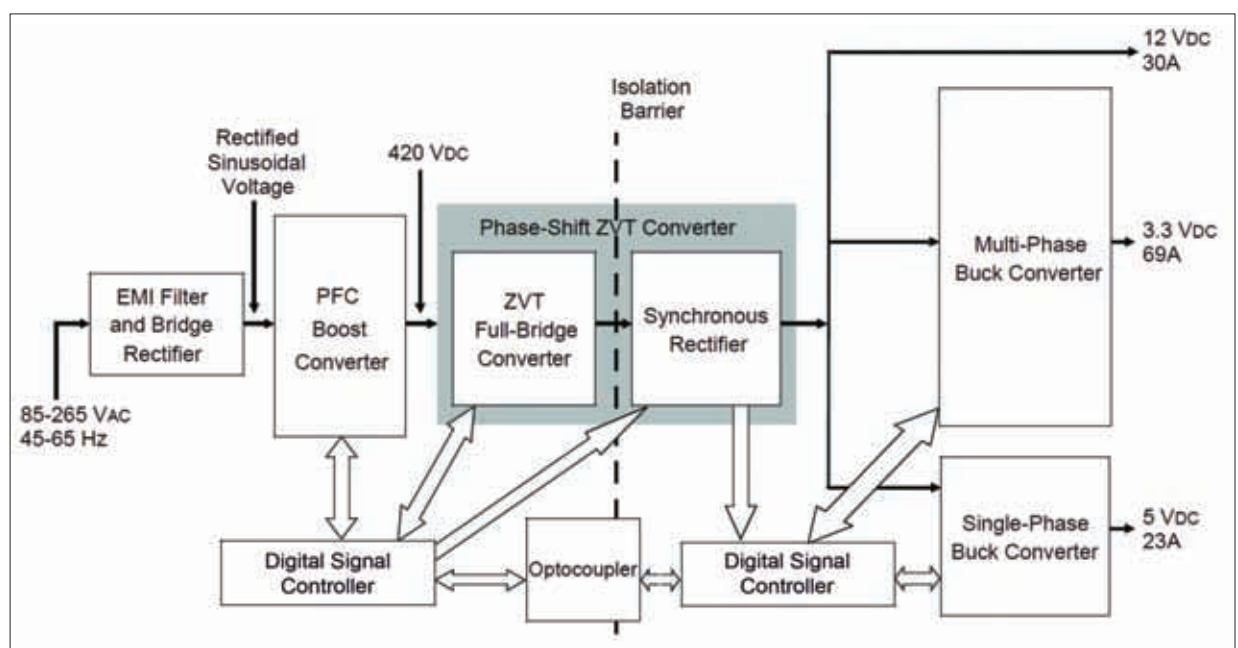


Figure 1: Detailed SMPS AC/DC reference block diagram



**Figure 2: The third generation of Microchip's dsPIC33 GS family, delivers 70 MIPS and includes features such as context-selected working register sets that further increase performance for digital power applications**

frequencies that result in not only greater efficiency but higher power density.

#### Digital signal controllers

The emergence of digital control in areas such as power conversion, motor drives and similar applications where adaptive control is advantageous, has led to the development of Digital Signal Controllers (DSCs). These devices merge the benefits of a Digital Signal Processor (DSP); extensively used in audio and video processing, and the venerable Microcontroller (MCU), to create a new class of device tuned to executing control algorithms that would be too complex for a traditional MCU, with the peripherals and interfaces not typically present in a DSP.

There is an increasing number of DSCs on the market, all of which strive to deliver on these demands. Those that best deliver exhibit a continued roadmap of architectural improvement, which allow developers to further improve the speed and accuracy of the control loop in their application, and enable them to take full advantage of the latest developments in control algorithms.

DSCs are essentially the definitive mixed-signal solution; they must combine digital processing with analog peripherals. Achieving an overall solution requires both domains to function together seamlessly, which is why fully integrated devices offer the best approach. Combining both analog and digital technology on a single device can, however, introduce design compromises, but improving performance in both domains in a balanced way is critical in delivering better solutions.

The essential components of a DSC are a core capable of efficiently executing signal processing algorithms, coupled with signal conversion in the form of one/multiple Analog/Digital Converters (ADCs), along with some form of Pulse Width Modulation

(PWM) output used to drive power transistors such as MOSFETs in the Buck/Boost conversion circuit(s). Bringing these elements together in a single architecture that supports fast control loops is the key to building a successful DSC, which in turn is the heart of efficient AC/DC and DC/DC power conversion.

#### Mixed signal solution

The third generation of Microchip's dsPIC33 GS family, the dsPIC33EP GS (Figure 2), delivers increased performance in these critical areas over the second generation. The core now delivers 70 MIPS (up from 50 MIPS) but also includes features such as context-selected working register sets that further increase performance for digital power applications beyond what the increased raw MIPS rating might suggest. By adding two additional working register sets the core now supports almost instantaneous context switching.

The performance of the analog peripherals has also been improved relative to previous generations. For example, products in this family offer up to five 12-bit ADCs, with the ADC conversion latency reduced from 600 ns to 300 ns. Together, these improvements enable a three-pole-three-zero compensator latency to be reduced from around 2  $\mu$ s to less than 1  $\mu$ s thereby reducing phase erosion to improve stability. Faster control loops also allow for higher switching frequencies and better transient response. The resulting efficiency gains made possible by the increased performance also lead to increased power density; power supplies can be designed to be smaller, using fewer and smaller discrete passive components.

A further architectural improvement in the 'GS' is the introduction of dual flash memory partitions, supporting a feature known as Live Updates. This allows a control algorithm, or any other software executed by the DSC,

to be updated in the field while the power supply remains fully operational; the new software is loaded in to the second, non-operational, flash partition and, when verified, the core switches to executing from the second flash partition. This is a feature that is particularly welcome in high-availability applications, such as server power supplies, where even small efficiency gains can result in large reductions in operational costs. Without the live update feature, such applications would be left with either updating the software during scheduled (or unscheduled) maintenance breaks in operation, or leaving the code unmodified and missing out on the potential benefits. Both of these options would be unwelcome in the server environments, of course.

#### Conclusion

The digital control of power conversion continues to develop, progressively replacing analog control due to the flexibility and potential efficiency gains it presents. While the complexity is undoubtedly a consideration for developers, the benefits can be persuading. Regulatory requirements aside, the use of digital control can clearly deliver better power conversion solutions and, with the introduction of Live Update, offer an upgrade path for solutions already deployed – even in high availability applications. DSCs represent the pinnacle of digital control in this and many other applications where complex algorithms meet high performance analog peripherals. The 'real world' of mixed signal solutions continue to offer an opportunity for performance gains at every level; fully integrated, advanced programmable solutions like the dsPIC33EP GS family represent the leading-edge of DSC technology, and will provide power supply developers with the next generation in control.

# Advantages of Digital Power and PMBus

Power-supply concepts have been well established for many years in the consumer segment, including laptop and desktop PCs, are now increasingly adopted in more industrial applications. The following article gives a detailed description of the advantages provided by digital power supplies, with a special emphasis on the possibilities offered by the PMBus interface. **Hans-Günter Kremser, Principal Field Application Engineer, Texas Instruments, Munich, Germany**

For many years, digital power supplies have been a hot topic in technical discussions held with customers. The most frequently asked questions are around the advantages provided by this technology and the customers that are already using it.

In spite of all skepticism, more and more customers decide to use a digital power supply for the following reasons:

- FPGA and processor suppliers demand a dynamic adjustment of the core supply voltage using adaptive voltage scaling (AVS) or dynamic voltage scaling (DVS). This enables dynamic performance increases or reductions depending on the individual processing load with the goal to achieve a lower power consumption.
- Remote monitoring of the power supply is required (for instance in cellular base stations).
- It is desirable to log the currents and voltages of the different output voltage paths (more information enables faster troubleshooting).
- Flexible sequencing when powering up and down the different output voltage paths during the prototyping phase.

## Different concepts

For instance, semiconductor manufacturers promote their analog switching converters featuring a PMBus™ interface. However, it is debatable whether these converters can be called 'digital' because the communication interface is the only digital element. Solutions are available for isolated and non-isolated power supplies based on common topologies. The portfolio includes converters featuring the current-mode, voltage-mode, constant-on-time, or DCAP (Direct connection to the Output CAPacitor) control schemes.

In addition, a number of switching converters featuring a PMBus interface digitize the feedback signal, compute the compensation using a processor or a

hardware block and adjust the PWM signal accordingly.

Advantages of this concept include the digital compensation and the reduced influence of temperature and aging effects. For instance, it is possible to dynamically adjust the compensation during operation, for instance if an inductive load is replaced by a capacitive

load. Even the compensation mode can be varied by modifying specific coefficients (e. g. for the second-order IIR filter included in the UCD9244). For instance, users can select whether the output voltage should be regulated to its desired value faster after a load step or if a low-pass behavior should be preferred for safety reasons. It is important to note

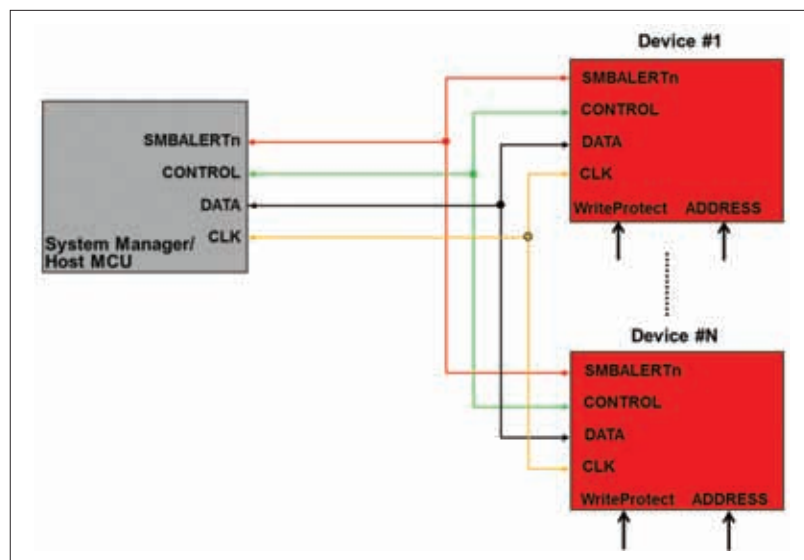


Figure 1: Block diagram of a PMBus-based power supply

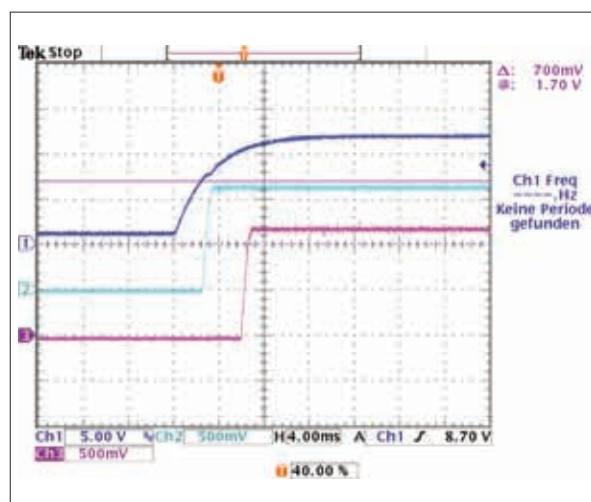


Figure 2: Core supply is powered up before the I/O supply

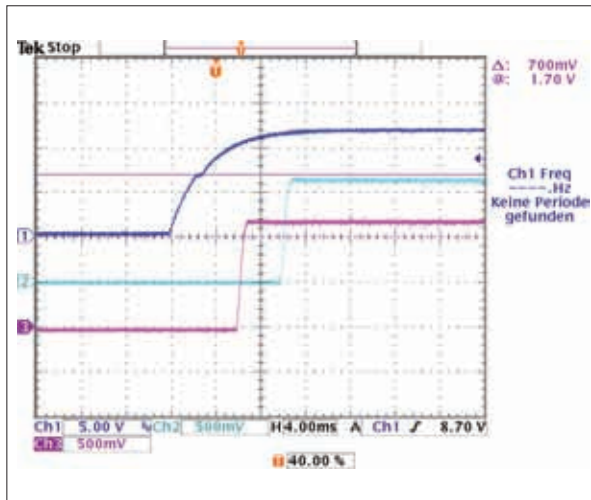


Figure 3: Core supply is powered up after the I/O supply

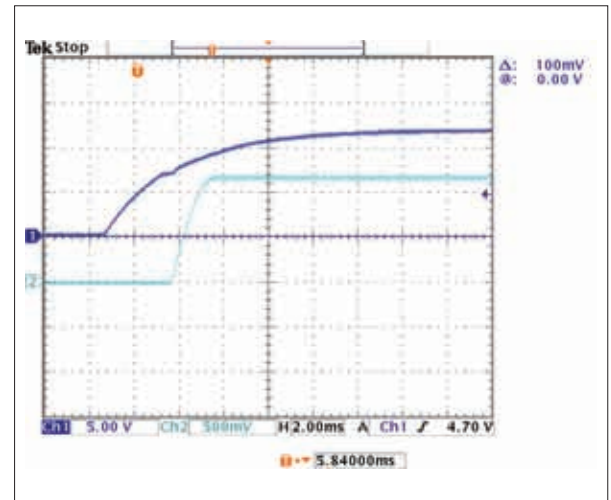


Figure 4: Soft start in approximately 2 ms

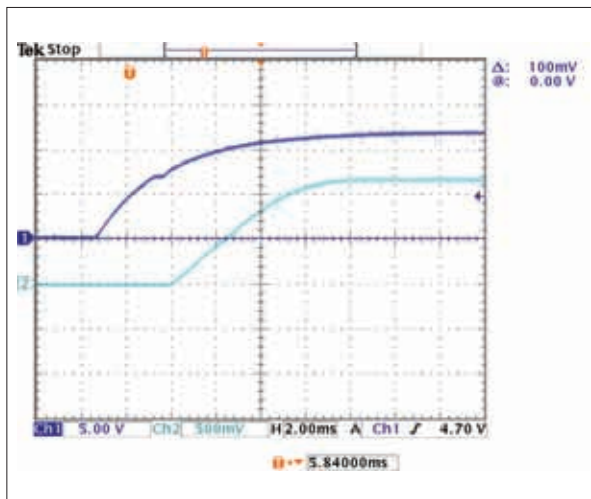


Figure 5: Soft start in approximately 8 ms

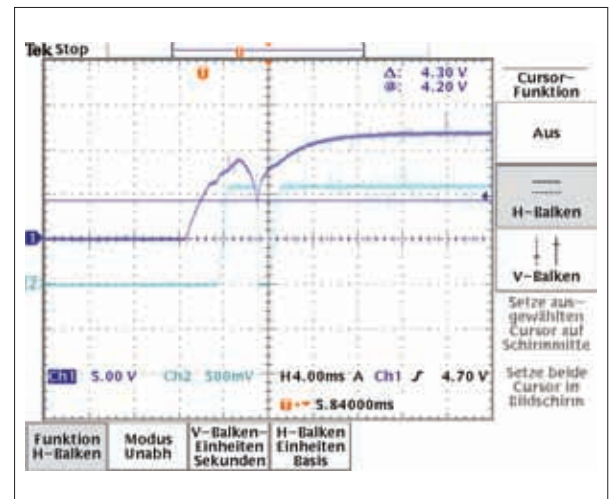


Figure 6: Hiccup mode

that no programming skills are required for this device. Instead, the required parameters can be easily specified via a graphical user interface. Of course, entirely processor-based power supplies are also available. Among others, TI provides libraries with the relevant functional blocks for its C2000 processors.

### The PMBus

Based on the I<sup>2</sup>C interface protocol, the PMBus protocol is designed for the purpose of controlling and monitoring power supplies. Figure 1 illustrates the structure of a typical PMBus system. The PMBus interface consists of clock and data lines and the SMBALERT connection. The CONTROL lines enable additional functions including powering up and down the bus-connected switching converters. The physical address of each converter is permanently set via hardware. Using the WRITE\_PROTECT command, the settings of the converter can be protected from inadvertent overwriting. Some manufacturers also provide an optional

WriteProtect pin as an additional safety mechanism. All converters must be able to start up without communicating with the host MCU. As the entire set of PMBus commands is not supported by all converters, it is necessary to consult the manufacturer's data sheet.

Both concepts provide the advantages outlined above. For the two solutions shown below, two TPS53915 12A regulators were connected to a computer and configured via a graphical user interface called Fusion Digital Power Designer. Figures 2 and 3 show oscilloscope plots of different power-on sequences of the core and I/O supply (for instance for a microcontroller). As the power-on sequence can be easily modified via software, this is very helpful for circuit designs based on initial prototypes. As shown in Figures 4 and 5, it is also possible to adjust the slope of the power-up edges.

The ability to set warning and alert levels is another important feature. For instance, output voltages and currents can

be monitored within pre-defined ranges. Furthermore, the switching frequency can also be set.

Figure 6 depicts the behavior of the output voltage in the event of a short circuit (input voltage drop). It is possible to select whether the voltage should remain switched off after an overload event or whether it should automatically be powered up again (hiccup mode).

Without the digital PMBus interface, all the features described above would require additional hardware, and some could not be implemented at all.

Customers do not have to pay any licensing fees when using PMBus ICs. The specifications and additional useful information can be downloaded for free at [www.pmbus.org](http://www.pmbus.org).

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## Logic Level Power MOSFETs

Infineon has extended its StrongIRFET™ Power MOSFET family which can be driven now directly from a microcontroller, saving space and cutting costs. Additionally, the MOSFETs are highly rugged and thus help lengthen the service life of the electronic devices. The tried and tested FET family enables high energy efficiency in electric appliances. With the logic level extension, the devices do not require a stand-alone driver - in the logic level variant the necessary gate-source voltage is reduced to 4.5 V. This makes it possible to directly connect the MOSFET with the microcontroller in many applications. The characteristic performance features of the StrongIRFET family have been retained in the logic level extension - low on-state resistance (0.52 mΩ typ. and 0.97 mΩ max.) for reduced conduction losses, and high current carrying capability for increased power capability.

[www.infineon.com/strongirfet](http://www.infineon.com/strongirfet)

## 120 Watt Planar Transformers

Coilcraft has introduced its new PoE120PL Series of high-efficiency planar transformers which are optimized for active clamp forward converters,



including use in Power over Ethernet PSE and pre-standard PD devices. The PoE120PL Series is suitable for 60-120 W applications such as thin clients, monitors, industrial Ethernet, IPTV, building management, nurse call systems, point-of-sale terminals and information kiosks. They are ideal for

90 Watt PoE++ Powered Devices (Pds). The transformers are optimized for 200 kHz and 36-72 V input. They also provide 1500 Vrms primary-to-secondary isolation and 0.229 mm clearance above the seating plane and include a 12-V auxiliary winding. PoE120PL Series transformers have a 20.83 mm x 23.37 mm footprint, with a maximum height of 10.34 mm, requiring far less board space and overall volume than a standard EFD20 wire wound package. They are RoHS compliant and feature matte tin over nickel over brass terminations. They have an ambient temperature range of -40°C to +125°C.

[www.coilcraft.com](http://www.coilcraft.com)

## AAC or SSD for 1200 V and 1700 V IGBTs

Designed to drive all standard 1200 V and 1700 V IGBTs, the 2SC0435T2G1-17 dual IGBT-driver core is a compact product with a footprint of only 57.2 mm x 51.6 mm and a height of just 20 mm. Devices use of SCALE-2+™ technology to implement Soft Shut Down (SSD) in the event of a short circuit without requiring additional components. This is particularly beneficial in applications with low stray-inductance. The core can also provide full Advanced Active Clamping (AAC) if required. Power Integrations' 2SC0435T2G1-17 driver core features an embedded paralleling capability to simplify inverter design at high power ratings. Multi-level topologies are also supported. Devices are RoHS-compatible and UL508C and UL 60950-1 recognized. Creepage and clearances fulfill IEC60664-1 for reinforced insulation OV2 and PD2.

The 2SC0115T2A0-12 dual-channel IGBT gate driver core is the most compact driver solution available for 90 kW to 500 kW inverters and converters. It provides a unique set of features which enhance system reliability and performance. The driver core concept leverages many years of real-world IGBT driver experience, improving system design speed and reducing verification cycles. Highly integrated ASIC technology also improves system reliability and performance by reducing the component count and eliminates the need for an opto-coupler. Incorporating Power Integrations' SCALE™-2+ integrated circuit and isolated transformer technology for DC/DC power and switching signal transmission, the 2SC0115T2A0-12 gate driver core suits modules up to 2400 A and switching frequencies of up to 50 kHz.

The driver core's reinforced electrical isolation targets systems with a working voltage of 900 V, which is typical for 1200 V IGBT modules and complies with the PD2 and OV II requirements of IEC 60664-1 and IEC 61800-5-1. The new gate driver core includes SSD protection for applications with low stray-inductance. For more demanding environments the 2SC0115T2A0-12 supports full AAC to control the IGBT voltage overshoot during turn-off.

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[www.power.com/products/2SC0115T](http://www.power.com/products/2SC0115T)

## Mid-Voltage MOSFET in an 8x8 Dual Cool Package

Fairchild launched its industry-leading mid-voltage MOSFET technology in a Dual Cool™ 8 mm x 8 mm package. The new Dual Cool 88 MOSFET gives power conversion engineers an alternative to bulky D2-PAK packages at half the size and with higher power density. Greater efficiencies with lower cost are enabled by the Dual Cool 88's packages advantages over D2-PAK, including smaller size, thinner profile, and 93 % lighter in weight, making them ideal for weight-sensitive applications. Compared to D2-PAK, the Dual Cool 88's package also delivers faster switching, less EMI along with the higher power density, and lower parasitic losses. The reduced parasitic losses are achieved using source clip not wire bonds, ensuring high pulse current with 63 % lower source inductance compared to D2-PAK devices.

<https://www.fairchildsemi.com/product-technology/dual-cool/>

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## Small But Powerful eGaN FET

EPC announces the EPC2039 FET, a high power density enhancement-mode gallium nitride (eGaN®) device. The EPC2039 is an extremely small, 1.82 mm<sup>2</sup>, 80 V, 6.8 A FET with a maximum on-resistance of 22 mΩ with 5V applied to the gate. This GaN power transistor delivers high performance in power conversion systems due to its high switching capabilities in a very small package. The EPC2039 has many uses but is primarily designed for high frequency power conversion applications, such as AC/DC synchronous rectification, Class-D audio, high voltage buck converters, wireless power transfer, and pulsed power (LiDAR) applications. Emerging LiDAR applications include driverless vehicles and augmented reality.

[www.epc-co.com](http://www.epc-co.com)

## Turnkey Wireless Power Kits



Integrated Device Technology introduced turnkey wireless power kits that make integrating wireless charging easy, affordable and practical for a broad range of consumer electronics. The new Qi-compliant transmitter and receiver reference kits deliver plug-and-play ease of integration, enabling engineers to incorporate wireless charging capabilities into their designs in a matter of hours. The 5-W, 5-V solution is suitable for a wide range of applications, including PC peripherals, furniture, medical devices, and other portable devices still hindered by traditional contact-based charging bases or cables. The transmitter and receiver reference kits are built around IDT wireless power semiconductors, and include reference boards and comprehensive design support collateral. Support materials include instructional videos, user manuals, foreign object detection (FOD) tuning guides, layout guides, layout instantiation modules, schematics, bill-of-materials (BOM), Gerber files, and more. Both reference kits offer 2-layer board layout files. The P9038-R-EVK and P9025AC-R-EVK are available now at suggested retail prices of \$40 and \$30, respectively, and can be ordered directly from participating distribution partners.

[www.idt.com/go/WPKits](http://www.idt.com/go/WPKits)

## Li-Ion 3-to-8 Cell Battery Pack Monitor



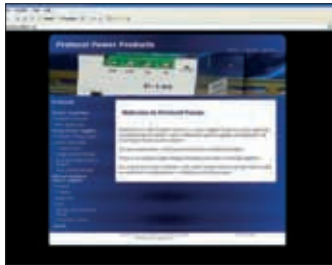
Intersil announced the ISL94203 3-to-8 cell battery pack monitor that supports Li-ion and other battery chemistries used in medical mobility carts, wheelchairs, e-bikes, handheld power tools, vacuum cleaners and solar or renewable energy storage systems. The device accurately monitors, protects and cell balances rechargeable battery packs to maximize battery life and ensure safe charging and system operation. The ISL94203 includes several programmable protection and monitoring features to safeguard battery packs from catastrophic events such as short circuit conditions and cell voltage shorts. It has an open wire check to ensure the IC is securely connected to the battery pack. The device also has a special protection feature that blows a polyfuse to render the battery pack inoperable in the event of a catastrophic failure. In addition to delivering diagnostic information, the ISL94203 can withstand battery pack hot plug events and support the full range of Li-ion chemistries. The battery pack monitor comes in a 6 mm x 6 mm, 48-lead TQFN package, and is priced at \$2.19 in 1k quantities. An evaluation kit is priced at \$328, it includes an evaluation board, interface board with USB to I<sup>2</sup>C interface, and software GUI that supports stand-alone operation or an external microcontroller.

[www.intersil.com/products/isl94203](http://www.intersil.com/products/isl94203)



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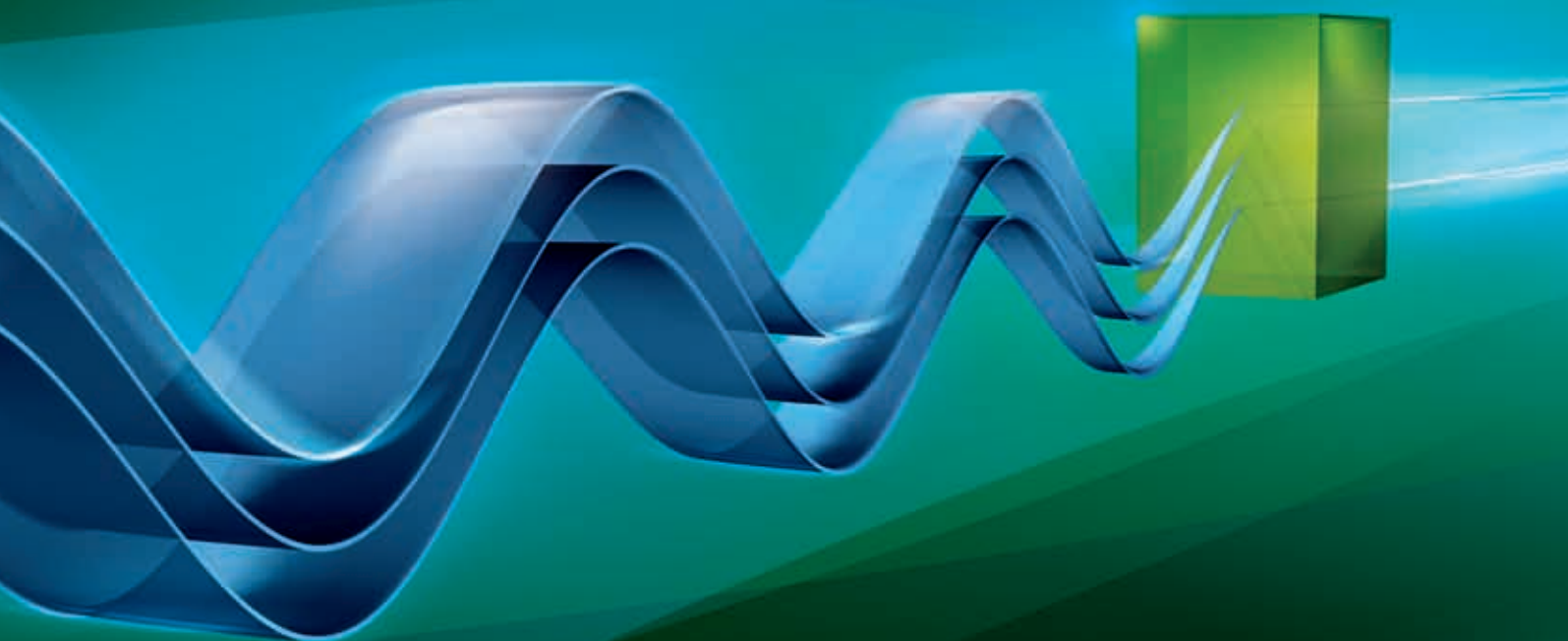
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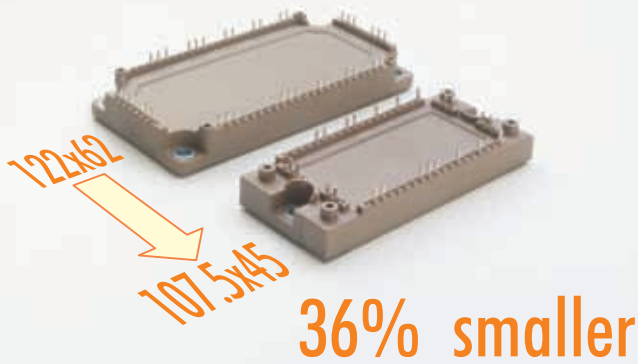


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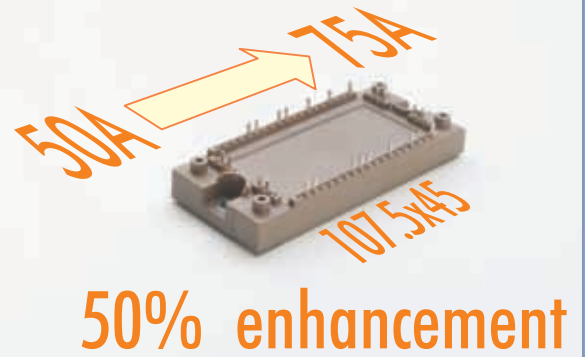


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