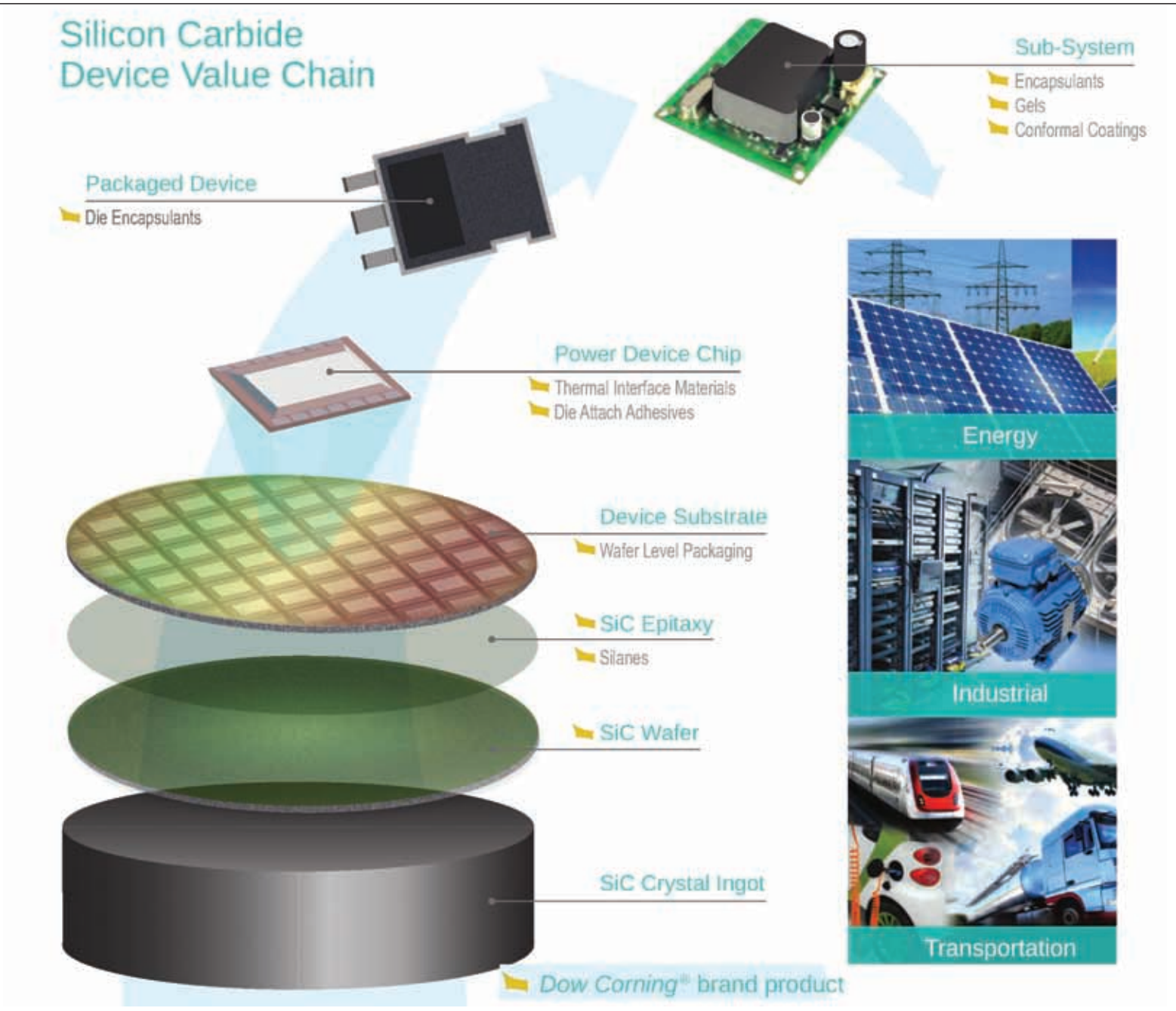
POWER ELECTRONICS EUROPE

ISSUE 4 – July/August 2016 www.power-mag.com

# SILICON CARBIDE

## High Quality 150 mm SiC Substrates for Power Electronics Applications



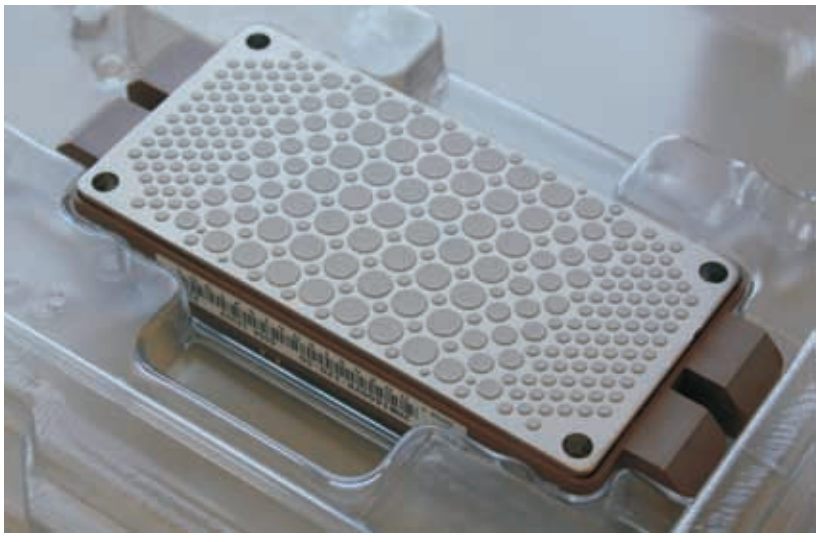

THE EUROPEAN JOURNAL FOR POWER ELECTRONICS
-----AND TECHNOLOGY-----

### Also inside this issue

Fuji Electric

*Innovating Energy Technology*

# Industrialized process for pre-pasted Thermal Interface Material (TIM)



## Features

+ Optimized for Fuji modules
+ Increase lifetime of IGBT
+ Advanced IGBT power density

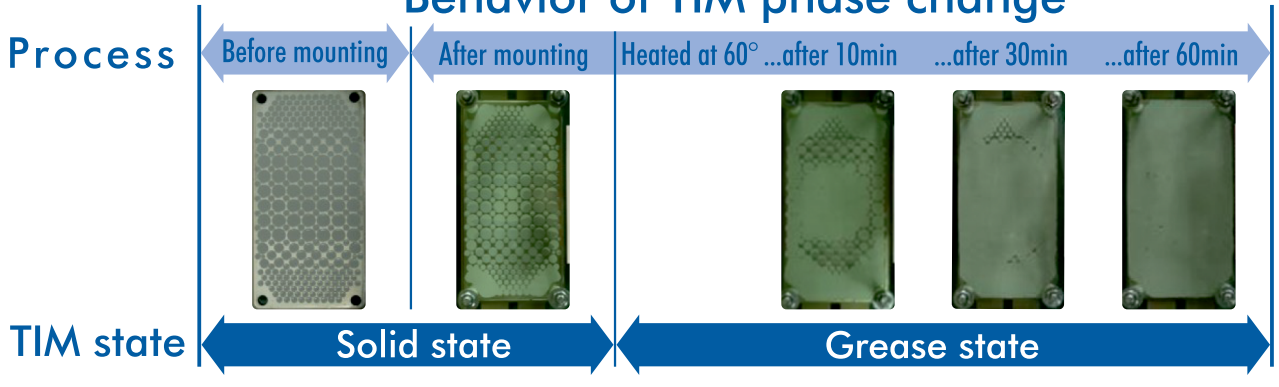
## Process - Benefits

+ Outsourcing of a dirty process
+ Stable quality level
+ Increased system reliability

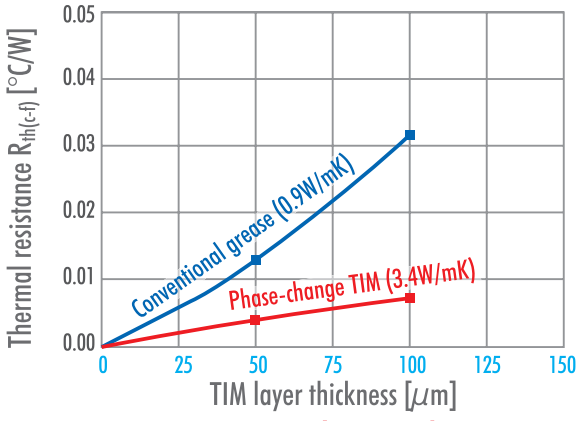
## Thermal - Benefits

+ Higher thermal conductivity
+ Uniform thermal resistance
+ Higher reliability and life time.

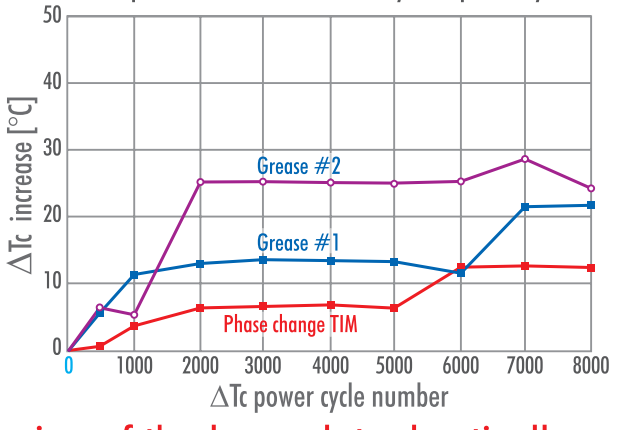
## Behavior of TIM phase change




Comparison of thermal resistance $R_{th(c-f)}$ (actual measurment)




Comparison of ΔTc transition by ΔTc power cycle




➥Fuji's PCM reduces the temperature swing of the base plate drastically

➥The new TIM is improving the ΔTc Power-Cycling capability

*For latest availability status of pre-pasted modules please contact us*


Fuji Electric Europe GmbH
Goethering 58
63067 Offenbach/Main-Germany

Fon +49(0)69-66 90 29 0
Fax +49(0)69-66 90 29 56
info.semi@fujielectric-europe.com

www.fujielectric-europe.com➥

**Editor** Achim Scharf
Tel: +49 (0)892865 9794
Fax: +49 (0)892800 132
Email: achimscharf@aol.com

**Production Editor** Chris Davis
Tel: +44 (0)1732 370340

**Financial Manager** Clare Jackson
Tel: +44 (0)1732 370340
Fax: +44 (0)1732 360034

**Reader/Circulation Enquiries**
Perception-MPS Ltd.
Tel: +44 (0) 1825 749900
Email: dfamedia@pmps.info

**INTERNATIONAL SALES OFFICES**
Mainland Europe:
Victoria Hufmann, Norbert Hufmann
Tel: +49 911 9397 643 Fax: +49 911 9397 6459
Email: pee@hufmann.info

Armin Wezel
phone: +49 (0)30 52689192
mobile: +49 (0)172 767 8499
Email: armin@eurokom-media.d

Eastern US
Karen C Smith-Kernc
email: KarenKCS@aol.com
Western US and Canada
Alan A Kernc
Tel: +1 717 397 7100
Fax: +1 717 397 7800
email: AlanKCS@aol.com

Italy
Ferruccio Silvera
Tel: +39 022 846 716 Email: ferruccio@silvera.it

Japan:
Yoshinori Ikeda,
Pacific Business Inc
Tel: 81-(0)3-3661-6138
Fax: 81-(0)3-3661-6139
Email: pbi2010@gol.com

Taiwan
Prisco Ind. Service Corp.
Tel: 886 2 2322 5266 Fax: 886 2 2322 2205

**Publisher & UK Sales** Ian Atkinson
Tel: +44 (0)1732 370340
Fax: +44 (0)1732 360034
Email: ian@dfamedia.co.uk
**www.power-mag.com**

Circulation and subscription: **Power Electronics Europe** is available for the following subscription charges. **Power Electronics Europe**: annual charge UK/NI £80, overseas $150, EUR 140.
Contact: DFA Media, 192 The High Street, Tonbridge, Kent TN9 1BE Great Britain.
Tel: +44 (0)1732 370340.
Fax: +44 (0)1732 360034. Refunds on cancelled subscriptions will only be provided at the Publisher's discretion, unless specifically guaranteed within the terms of subscription offer.

Editorial information should be sent to The Editor, **Power Electronics Europe**, PO Box 340131, 80098 Munich, Germany.



Printed by: Garnett Dickinson.

ISSN 1748-3530



## COVER STORY

## High Quality 150 mm SiC Substrates for Power Electronics Applications

Silicon Carbide (SiC) technology is being more broadly adopted by the power electronic market within applications rated at voltages of 600V or above, whereas silicon-based technology is still preferred for lower voltage class devices. The benefits of SiC devices over silicon-based counterparts are very well-known by the industry and reside in the high temperature resistance, high thermal conductivity and high critical field of SiC. All of these benefits translate into final systems with smaller form factors, higher efficiencies and lower requirements in cooling performance. This article will provide a current picture of the tremendous improvements made over the past few years in order to provide today a commercially available 4H-SiC 150 mm technology approaching and even overpassing the 100 mm technology performance. More details on page 16.

Cover material supplied by Dow Corning USA/Belgium

SEMIKRON
innovation + service

## Multiple Sourcing

# Exceeding the Standard with Products for Your Reliable Supply Chain

Highest supply chain safety through wide range of standard industry packages

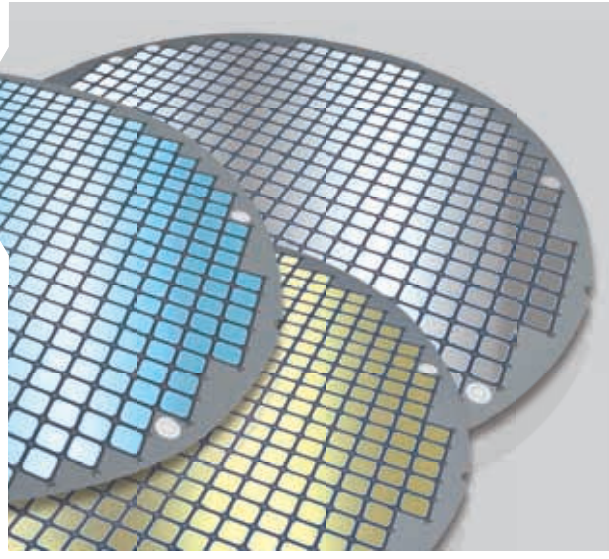
Multiple sources for IGBT and diode chips available in all voltage classes

Exceeding the standard:
- by smart integration of functionality at same space
- by optimisation of thermal and dynamic performance

Motor Drives | Wind Energy | Solar Energy | Power Quality | Utility Vehicles | Urban Transport Equipment

www.semikron.com

shop.semikron.com



# Changing Landscape of Power Electronics

According to a keynote at PCIM Europe 2016 by Navitas' CTO Dan Kinzer, IGBTs are being surpassed by 1,200V SiC-FETs in high power (multi-kW) applications like electric vehicle drive and solar string inverters. In lower power (~300 W) solar micro-inverters, high frequency 650 V GaN systems are under evaluation. As manufacturing volumes increase and costs fall, low voltage (100 V) Si used in solar optimizers may also be replaced by GaN devices. Additionally, material properties of WBG devices such as high critical E-field and high carrier mobility, enable SiC and GaN to achieve huge improvements over Silicon in current-handling and high-frequency operation. Advances in low-inductance packaging and a transition from discrete power and drive implementation to co-packaging and monolithic integration simplify and optimize end applications, enabling new form-factors and lower system costs

The power electronics industry landscape thus is evolving, showing "a new face", and power electronics consolidation is increasing, said Yole's analyst Hong Lin very recently. Last year Infineon acquired International Rectifier, this year ON Semiconductor acquired Fairchild Semiconductor, Cree outsourced its Power/RF division into Wolfspeed who in turn acquired packaging expert APEI. And in July Infineon again announced to acquire Wolfspeed. According to Yole the story is still unfolding. So who will be next? Wolfspeed and Infineon Technologies are leaders in the SiC power devices industry. The combination of both players will clearly strengthen the leading position of Infineon Technologies in the SiC power business, since Wolfspeed not only is the leader in SiC diodes and MOFETs, but also the major supplier of SiC wafers for Infineon and other power semiconductor manufacturers. This acquisition comes in a power electronics industry where SiC technology benefits are well-known and where business opportunities have been clearly identified by industrial companies.

According to Li, Wolfspeed has developed a powerful SiC MOSFET solution, which is clearly more advanced than Infineon Technologies' solutions, within the commercialization phase: Wolfspeed's Gen 3 has already been commercially available for two years and has a good reputation. From its side, Infineon just released its MOSFET component in May 2016. Within a SiC MOSFET market that is just taking off, Infineon's acquisition of Wolfspeed ensures its development in this market segment. Compared with Infineon's SiC-JFET, the new SiC-MOSFET allows a significant reduction of the switching losses. The device concept shows considerably suppressed parasitic turn-on under typical operating conditions. This results in drastically reduced recovery losses leading to very low total switching losses, so an Infineon speaker at PCIM 2016. In parallel, as No. 1 in the incumbent Silicon power business, Infineon Technologies has a well-established client portfolio. The German company has a strong understanding of the market's needs, its players, and the technical specifications related to power electronics applications. The company also has significant experience in power packaging for semiconductors, which is considered the main SiC business bottleneck for power electronics today. Last year, Wolfspeed acquired APEI to reinforce their packaging capability. Today, with the support from Infineon Technologies, Wolfspeed can further accelerate their product development and reaffirm the leadership of its technology approach. Finally, Infineon's investment and large-scale production capability could support Wolfspeed in ramping up production and expansion.

Yole views this acquisition as the beginning of a series of impressive collaborations within the SiC power business in the coming years, and this industry trend is likely to continue and to further increase in the future to accelerate the power electronics industry's consolidation phase. What strategy will other power electronics companies adopt in response to Infineon Technologies? Do they have to make strategic technical choices? Will we see new collaborations, mergers or acquisitions in the near future? According to Yole's analysts, it's likely we will. But this trend has not always a positive industry impact – fewer vendor mean fewer sources and competition what may lead to higher pricing. Both Wolfspeed and Infineon Technologies are the market leaders and this pact reinforces their dominant market position. The deal also includes the related SiC wafer substrate business for power electronics and RF power electronics. According to Yole's analyst Infineon's market share should increase to more than 50 percent if the full acquisition is confirmed.

Whether new start-ups and entrants particularly in the GaN power semiconductor market might fill the foreseeable gap is unclear – since often the business model of start-ups indeed is to be acquired by a large company at the point in time when it comes to expansion.

We will keep you informed in the future – but also on the following pages!

**Achim Scharf**
**PEE Editor**

# The Brexit and Consequences

The British public have voted to leave the European Union with a majority of around 52 percent. The full repercussions of the UK's decision are not yet known, with the new government now likely to enter months or even years of talks and negotiations with the EU.

With Pound Sterling plummeting to its lowest level in 31 years and the stock market falling sharply after this decision, what lies ahead? What will be the impact on companies and markets? What can be done to mitigate potential repercussions that Brexit will inevitably bring? Even more importantly, how can companies adapt to the important changes coming our way and identify new opportunities?

Brexit is likely to take a minimum of 2 years to materialize, with the process for withdrawal from the EU expected to start when Article 50 of the Treaty of Lisbon is triggered. Once the intention of separation is formalized, Britain will begin to negotiate withdrawal terms with EU member states on issues such as trade tariffs and the movement of UK and EU citizens, in effect laying the ground for its redefined relationship with the EU. "It is important to note that during this interim period, Britain will still be subject to existing EU treaties and laws, but will be barred from decision making processes. Therefore, existing regulations are likely to continue until negotiations are completed", Frost&Sullivan's Managing Director for Europe, Sarwant Singh, explained. "However, given that UK is the first member state to leave the EU, there is uncertainty regarding the path ahead. This could trigger a dip in business sentiment and delays in Foreign Direct Investments. On a positive note however, Brexit could pave the way for Britain to expand trade relations with the rest of the world beyond EU, and this would especially help mitigate risks arising from excessive reliance on one trading partner."

Looking at the UK financial sector, there may be risks if financial institutions lose passporting rights which presently allow for the sale of services across EU states without the need to secure local regulator approval. Britain could also see the departure of automotive plants if manufacturers cease to enjoy the benefits of tariff free trade with the EU. Currency volatility could persist in the medium term given the uncertainty of the path ahead and if the devaluation sustains, exports becoming more attractive, therefore benefitting UK based manufacturers.

For small and medium enterprises (SME), one of the issues that is now front of mind, will be how this affects their recruitment strategy. "UK businesses of all shapes and sizes have, at some point or another, relied on the EU to supplement their workforce. The UK is still in the midst of a skills shortage, and EU migrants have provided many of the vital skills that we were lacking. There is a chance that the UK will no longer be the talent magnet it used to be, resulting in more bureaucracy and a reduced candidate pool for SMEs to dive into", adds Phil Foster, Managing Director of Love Energy Savings. "The status of current EU migrants, and whether they will have to return to Europe, as well as how easy it will be for people to migrate into the UK for work, is not yet known. While the freedom of movement policy may still apply if the UK choose to remain part of the single market, there is a possibility that the need for Visas will complicate the recruitment process, making it more expensive and therefore deterring SMEs from hiring non-nationals. Ultimately, this may hinder how businesses grow in the future. The ability of the UK to allow in more migrants from outside of the EU, without exceeding any immigration quota, will also be something to keep an eye on. By no longer having to give preference to EU workers, opportunities open up for those coming to the UK from India, China and beyond".

One of the biggest expenditures for small businesses will be their energy, and the UK public have been warned recently that leaving the EU could have negative consequences on our bills. "With the possibility of rising energy prices, small business owners should look to cut back wherever they can. This can include introducing some energy efficiency policies, whether that's greener LED lightbulbs or adding movement detectors to turn off your lights automatically. There are so many small changes to be made, and they all add up to save a great deal of money for SMEs.

**www.frost.com, www.loveenergysavings.com**

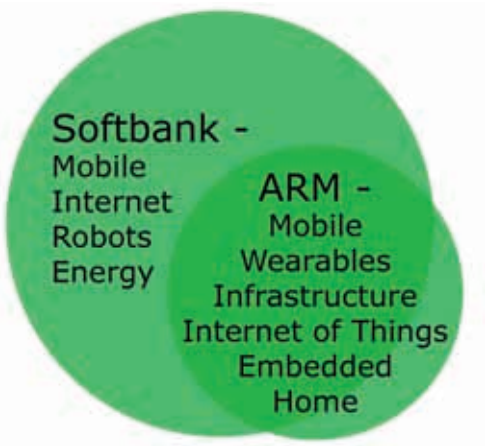
# Japanese Telecom Company Acquires British ARM Holdings Ltd.

On July 18th, Japan's Softbank Group Corp. announced a strategic agreement to buy ARM Holdings Ltd. in a $32 billion cash bid. The news of this bid has stirred many to speculate about the financial validity and the politics in face of the upcoming Brexit and the Pound/Dollar exchange rate.

Softbank originated as a software distributor in 1981 and quickly expanded to include PC- and software-media publishing. The company expanded as a securities investment firm in 1994 and continued investing in securities and technology media outlets. Since the turn of the century, Softbank has grown primarily by acquiring and growing communications companies in mobile and broadband markets, which helped insulate the Softbank from the sluggish PC market in the last decade, thanks to a prescient view of the growth in mobile technologies. With mobile handsets beginning to enter market saturation in many mature economies, the Internet of Things (IoT) has become the next great disruptive technology. "Softbank's investment in ARM might not only be paid back by further growth in ARM, but also help protect the company's other investments and drive future investment strategies", expects IHS analyst Lee Ratliff. "The cost is steep for Softbank, representing its largest investment yet, but while ARM annual revenues for 2015 were just short of $1.5 billion, the company represents a crucial piece of technology. ARM is in almost every mobile handset on the current market and microcontrollers based on ARM core technology lead the market, with approximately 24 percent of all revenues going to MCU suppliers. ARM also announced last year their intention to be in 45 percent of servers by 2020 – an aggressive but significant strategy for its system-on-chip (SoC) platforms for cloud computing growth", adds IHS analyst Tom Hackenberg.

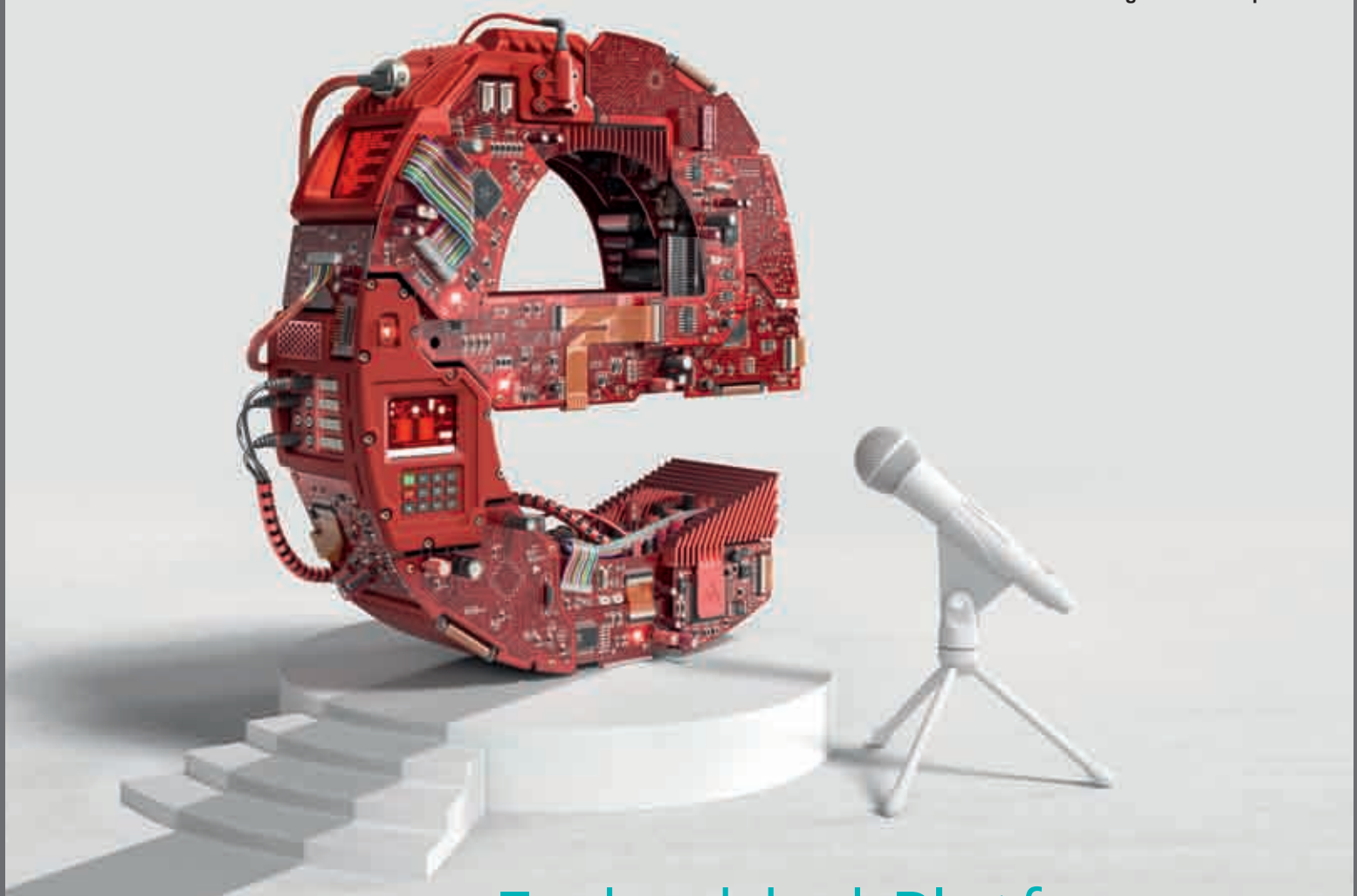
The purchase appears to be an opportune buy for Softbank, with Brexit raising the value of the Japanese Yen compared to the British Pound. Softbank's Chief Executive Officer, Masayoshi Son, advised that this move has been under consideration for some time, the decision to move forward happened only a couple of weeks ago, which coincides with the effect of Brexit on monetary conversion rates. While the UK has historically been opposed to international takeovers, the economic effects of Brexit may be weighing heavily on that strategy at this time. It seems that in order to smooth the approval process, Son contacted the new British Prime Minister, Theresa May, before the announcement, and Softbank's announced strategy to double the workforce of ARM in the UK over five years is a likely outcome of that conversation. "However, it is unclear whether the workforce increase will result in new jobs for ARM or redistribution from other regions. It is likely to be more of the former and a little of the latter. Regardless, it is unlikely that the acquisition will experience enough political opposition to disrupt the deal", Hackenberg said.

**www.ihsmarkit.com**



Messe München

Connecting Global Competence



# Embedded Platforms Conference.

International conference on future-proof hardware and software platforms.

Topics:

- IoT and security
- Microcontrollers and peripherals
- Power and sensors (incl. wireless charging)
- Embedded communication

Information & Registration:
**electronica.de/en/embeddedplatforms**

**Embedded Platforms Conference**
**November 9–10, 2016 | Messe München**

The conference is held within the scope of electronica, the World's Leading Trade Fair for Electronic Components, Systems and Applications.

electronica 2016
inside tomorrow

# Infineon Acquires Cree/Wolfspeed

After acquiring International Rectifier in early 2015 mainly because of its GaN technology Infineon has entered into a definitive agreement to acquire the Wolfspeed Power and RF division of US-based Cree. The deal also includes the related SiC wafer substrate business for power and RF power. The purchase price for this planned all-cash transaction is $850 million. The business to be acquired by Infineon has generated pro-forma revenues of $173 million in the twelve months ending March 27, 2016. The closing of the transaction is subject to regulatory approvals in various jurisdictions and is expected by the end of calendar year 2016.

"This acquisition will enable us to provide the broadest offering in compound semiconductors and will further strengthen our position as a leading supplier of power and RF power solutions in high-growth markets such as electromobility, renewables and next-generation cellular infrastructure relevant for IoT", comments Infineon's CEO Reinhard Ploss. "With Wolfspeed we will become number one in SiC-based power semiconductors. We also want to become number one in RF power. This will accelerate the market introduction of these innovative technologies, addressing the needs of modern society – such as energy efficiency, connectivity and mobility." Wolfspeed is based in Research Triangle Park, North Carolina, and has been a part of LED manufacturer Cree for almost three decades. Wolfspeed is a premier provider of SiC-based power and GaN-on-SiC-based RF power solutions. This also includes the related core competencies in wafer substrate manufacturing for SiC, as well as for SiC with a monocrystalline GaN layer for RF power applications. With these competencies, more than 550 employees and a strong IP portfolio of approximately 2,000 patents and patent applications, this deal complements Infineon's previous acquisition of International Rectifier in early 2015.Wolfspeed's SiC-based product portfolio ideally adds to Infineon's offering, since Infineon relied for a long time on SiC diodes and SiC JFETs. At PCIM 2016 the company introduced its first SiC MOSFET, long time after Cree/Wolfspeed who is now leading the market in this segment.

Major areas where the applications will profit from SiC are renewables and especially automotive. Both areas benefit from the increased power density and improved efficiency. In automotive it fits well with the recent increased commitment of the industry to plug-in hybrid and all-electric vehicles. Next-generation cellular infrastructure standards such as 5G and beyond will use frequencies up to 80 GHz. Only advanced compound semiconductors can deliver the required efficiencies at these high frequencies. GaN-on-Si allows higher levels of integration and offers its advantages at operating frequencies of up to 10 GHz. GaN-on-SiC enables maximum efficiency at frequencies of up to 80 GHz. Both technologies are crucial for next generation cellular infrastructure standards.

**www.infineon.com**

**BELOW: Reinhard Ploss (left), CEO of Infineon Technologies AG, and Chuck Swoboda, Cree's CEO agree on the Wolfspeed transaction**


# Belgium Researcher Imec Expands to Florida

Imec Florida is a new entity focusing on photonics and high-speed electronics IC design based in Osceola, Florida. Imec Florida kicked off with the signing of a collaboration agreement with the University of Central Florida (UCF), Osceola County and the International Consortium for Advanced Manufacturing Research (ICAMR), that is setting up fab facilities for the development and production of highly innovative III-V-on-Silicon electronics.

Imec Florida will be established as a design center facilitating the collaboration between imec's headquarters, based in Leuven, Belgium, and U.S.-based semiconductor and system companies, universities, and research institutes. Imec Florida's initial focus will be the R&D of high speed electronics and photonics solutions, starting with an offering of IC design research for a broad set of semiconductor-based solutions such as THz and LIDAR sensors, imagers, and a broad range of sensors. It will also provide IC design needs that will be driving the ICAMR manufacturing research. Through imec Florida, imec's design, prototyping and low-volume production service - also named imec IC-link - will provide the US market low-cost access to advanced foundry services, helping entrepreneurs to (industry and academia) design innovative products and get them to market. The new center aims to employ about 10 scientists and engineers by the end of the year and increase to 100 researchers in the next five years. Heading up the facility as General Manager will be imec's Vice President Bert Gyselinckx who previously served as General Manager at Imec in Eindhoven/Netherlands and helped to co-invent many technologies deployed by semiconductor and consumer electronics companies.

**www.imec.be**

OUR BURN-IN

THEIR BURN-IN

# DC LINK RELIABILITY

100% of our 947D DC Link capacitors are conditioned at accelerated temperature and voltage before they leave the factory. We've demonstrated that this process eliminates infant mortal failures and produces the most thermally and electrically stable DC Link Capacitors available today.

If that's the kind of reliability you're looking for, trust the one company where it's burned in.

***Call for samples with thermocouples.***

CDE ENERGIZING IDEAS

CORNELL DUBILIER

**www.cde.com | 508-996-8561**

# LED Driver ICs Cut BOM Count by 40 Percent

Power Integrations itroduced its LYTSwitch™-7 single-stage, non-isolated, TRIAC-dimmable, buck topology LED driver IC family. Capable of delivering up to 22 W without a heatsink in a SO-8 footprint, these high-efficiency devices are suitable for bulbs, tubes and fixtures. LYTSwitch-7 designs do not require bleeders; employing simple, passive damping for TRIAC management and an off-the-shelf, single-winding inductor, reducing component count to just 20, as compared to approximately 35 parts for typical dimmable LED driver boards, according to the company.

LYTSwitch-7 ICs deliver a phase-cut (TRIAC) dimming solution with a wide dimming range and monotonic dimming response. The LED drivers enable efficiency of greater than 86 % – with high PF, accurate regulation and comprehensive protection. They suit low- or high-line input as well as wide-range universal-input designs for U.S. commercial lighting applications, which operate from 90 VAC to 305 VAC with TRIAC dimming enabled in low-line installations. Devices are priced at $0.33 in 10,000-piece quantities.

**Application example**

The circuit shown in the applications example is a LED driver configured as a low-side buck utilizing the LYT7503D from the new LYTSwitch-7 family of ICs. This low component count (20 parts) dimmable LED driver is designed to power a 60 V LED voltage string at 125 mA output current from an input voltage of 90 VAC to 300 VAC. Dimming performance is optimized at low-line input (i.e. 120 VAC), while maintaining accurate regulation for non-dimmable high-line input.

LYTSwitch-7 is a SO-8 package LED driver IC family designed for non-isolated buck applications. The LYTSwitch-7 family provides high efficiency, high power factor and accurate LED current regulation. It incorporates a high-voltage 725 V power MOSFET and a control engine to switch the MOSFET in critical conduction mode (CrM) with variable on-time and variable frequency which also helps achieve low EMI, and low THD. The CrM operation results in low turn-on losses and reduces cost of output diode (slower reverse-recovery type can be used). The controller also integrates protection features such as input and output over-voltage protection, thermal fold-back, over-temperature shutdown, output short-circuit and over-current protection. The controller also allows natural dimming with only the addition of a damper resistor and an RC network for damping the input current ringing when the TRIAC turns on.

**Key design considerations**

The input fusible resistor RF1 provides multiple-purpose function – safety protection, current limiting against differential surge and acts as a damping element reducing inrush-current ringing when TRIAC dimming. Varistor RV1 acts as a voltage clamp that limits the voltage spike on the primary during line transients and surge events. A 250 VAC rated part was selected with a maximum clamping voltage specification of 710 VDC – lower than the device drain


**New LYTSwitch™-7 single-stage, non-isolated, TRIAC-dimmable, buck topology LED driver IC family**

voltage (725 V). The AC input voltage is full wave rectified by BR1 to achieve good power factor and low THD.

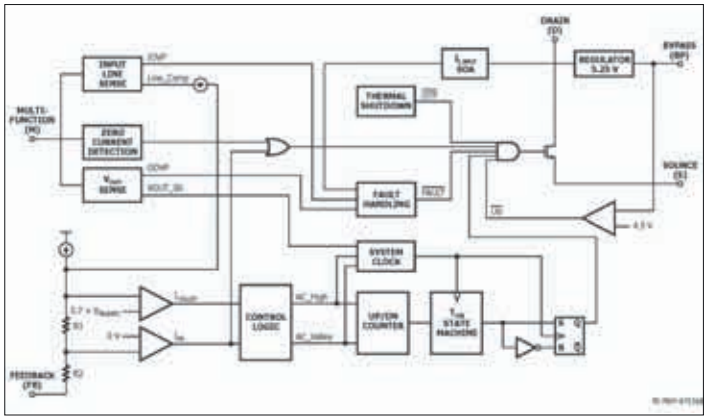
The rectified AC supply is filtered by the input capacitors C1 and C2. Too much capacitance degrades power factor and THD, so the values of the input capacitors were set to the minimum necessary to meet EMI (with suitable margin).

Inductor L1, C1 and C2 form a π filter, which attenuates conducted differential and common mode EMI currents. It also allows simple inductor construction suitable for the auto-winding inductor manufacturing approach used for low-cost high volume production. The recommended location of the EMI filter is after the bridge rectifier as this allows the use of regular film capacitors (as opposed to more expensive safety rated X-capacitors that would be required if the filter is placed before the bridge).

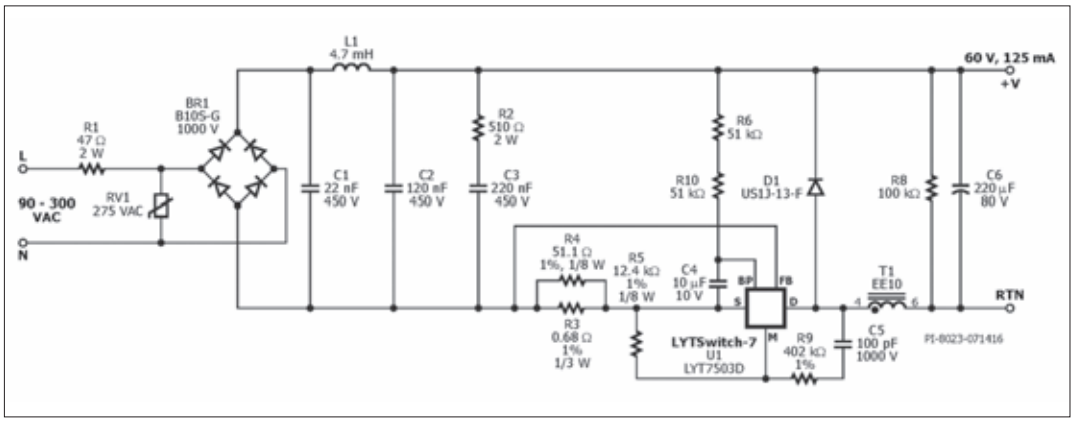
Since the integrated switch MOSFET for LYTSwitch-7 is referenced to ground, the SOURCE pin acts as an EMI shield. This allows a "dog-bone" inductor to be used in low-side configurations.

The addition of the RC damper network R2 and C3 makes the driver compatible with TRAIC (phase-cut) dimmers. The RC damper be placed before or after the bridge rectifier. In this design, the RC damper is located after the bridge rectifier for higher dimming range. Putting the RC damper before the bridge would load the TRIAC dimmer and maintain full output to a lower conduction angle but would result in reduced dimming range.

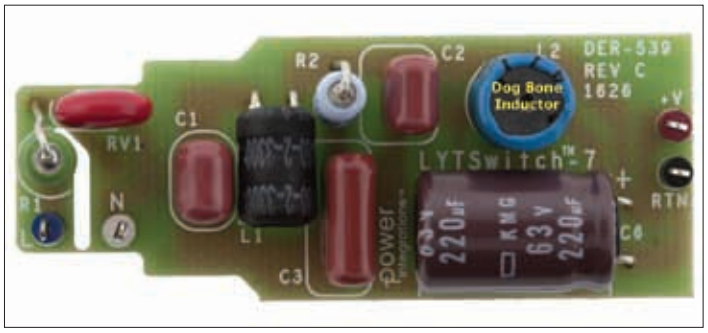
The LED driver circuit is a low-side buck configuration operating in CrM. The controller allows complete



**LYTSwitch-7 internal block diagram**




**A LYT7503D switch for 7.5 W, 60 V, 125 mA dimmable non-isolated low-side buck configuration**




**Dimmable 6.24 W, 52 V, 120 mA Low-Line LED driver using an off-the-shelf "dog-bone" type inductor application PCB**

transfer of the energy stored in the inductor to the load before starting the next switch cycle. The inductor demagnetization is sensed, detecting when the voltage across the inductor begins to collapse (towards zero) as flywheel diode (D1) conduction ceases. Capacitor C4 provides local decoupling for the BYPASS (BP) pin IC and provides power to the controller during the MOSFET on-time. The IC has an internal regulator that draws power from the high-voltage DRAIN (D) pin and charges the bypass capacitor C4 during the power switch off-time.

The typical BYPASS pin voltage is 5.22 V. To keep the IC operating normally (especially during the dead time), where $V_{IN} < V_{OUT}$, and during dimming at low conduction angles, resistors R6 and R10 are employed to keep the bypass capacitor charged.

The value of the bypass capacitor should be large enough to keep the bypass voltage above the $V_{BP(RESET)}$ reset value of 4.5 V. The suggested minimum value for the bypass capacitor is 10 µF; an X7R type is recommended if using a ceramic type capacitor. Constant output current regulation is achieved through the FEED-BACK (FB) pin directly sensing the DRAIN pin current during the MOSFET on-time via external current sense resistors (RFB) R3 and R4. The voltage drop is compared to an internal 279 mV (typical) reference voltage ($VF_{B(REF)}$).

During the MOSFET-switch off-state, free-wheeling diode D1 rectifies and conducts the voltage across T1 and the output is filtered by C6. An ultrafast 1 A, 600 V with 75 ns reverse recovery time ($t_{RR}$) diode was selected for efficiency and good regulation over line and across temperature . The value of the output capacitor C6 was selected to give peak-to-peak LED ripple current equal to 30 % of the mean value.

For designs where lower ripple is required, the output capacitance value can be increased. A small output pre-load resistor R8 discharges the output capacitor when the driver is turned off, giving a quick and smooth decay of the LED light after turn-off. Recommended pre-load power dissipation is ≤0.25 % of the output power.

The small output inductor uses a ferrite cored EE10 with an open winding window that allows better convection cooling for the winding. An off-the-shelf "dog-bone" type inductor could also be used. To ensure proper magnetic design and accurate output current regulation, it is recommended that the LYTSwitch-7 PIXls spreadsheet located at PI Expert web site should be used for magnetics calculations.

**https://piexpertonline.power.com/site/login, https://www.power.com/lytswitch-7**

# Fast E-GaN FET Driver Ease Half-Bridge Designs

Peregrine Semiconductor Corp., founder of RF SOI (silicon on insulator), offers the fastest switching GaN FET driver. Manufactured on a insulating substrate, UltraCMOS technology has no bulk or well junctions, and therefore has low parasitics. It also has low on-resistance for improved efficiency and low off-capacitance at higher operating frequency.

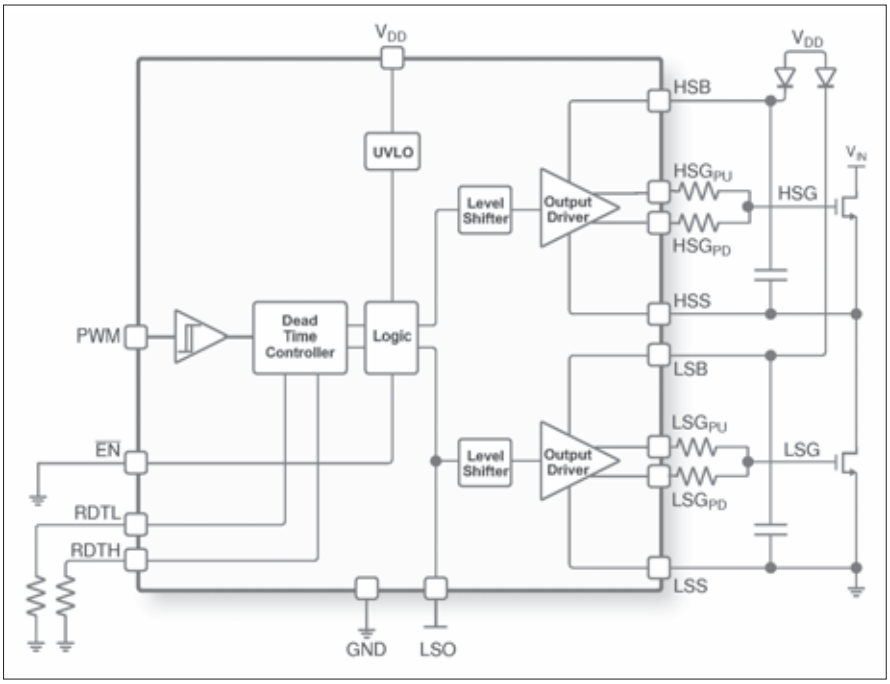
GaN-based FETs are disrupting the power conversion market and are displacing Silicon-based MOSFETs. GaN FETs operate much faster and have higher switching speeds in the smallest possible volume. The promise of GaN is that it can reduce the size and weight of any power supply. To reach their performance potential, these high-performance GaN transistors need an optimized gate driver. This FET driver must charge and discharge gate capacitance as fast as possible, and it must have very low propagation delay to allow fast signals. It also must avoid "shoot through" by not turning on high-side and low-side FETs at the same time. The PE29100 is designed specifically for this purpose. Volume-production parts, samples and evaluation kits are available now. Offered as a 2 x 1.6 mm flip-chip die, the PE29100 is $1.80 each for 1k-quantity orders.

### Technical specifications

The UltraCMOS PE29100 is a half-bridge GaN FET driver with internal dead-time control. The high-speed driver operates up to 33 MHz and handles voltages up to 80 V. It delivers a short propagation delay of 8 ns. It has a rise time of 2.5 ns and fall time of 1.8 ns when driving a 1000 pF load and 1 ns rise and fall times with 100 pF load. The PE29100 has a one-pin, single-phase input mode and has an output source current of 2 A and an output sink current of 4 A.

The PE29100 is intended to drive both the high-side (HS) and the low-side (LS) gates of external power FETs, such as eGaN FETs. The PE29100 favors applications requiring higher switching speeds due to the reduced parasitic properties of the high resistivity insulating substrate inherent with Peregrine's UltraCMOS process.

The driver uses a single-ended pulse width modulation (PWM) input that feeds a dead-time




**Functional block diagram including test circuit used for obtaining measurements. The two bootstrap diodes are used for symmetry purposes in characterization. In practice, only the HSB diode is required**

controller, capable of generating a small and accurate dead-time. The dead-time circuit prevents shoot-through current in the output stage. The propagation delay of the dead-time controller must be small to meet the fast switching requirements when driving eGaN FETs. The differential outputs of the dead-time controller are then level-shifted from a low-voltage domain to a high-voltage domain required by the output drivers.

Two external resistors control the timing of outputs in the dead-time controller block. The dead-time resistors only affect the LS output; the HS output will always equal the duty-cycle of the input.

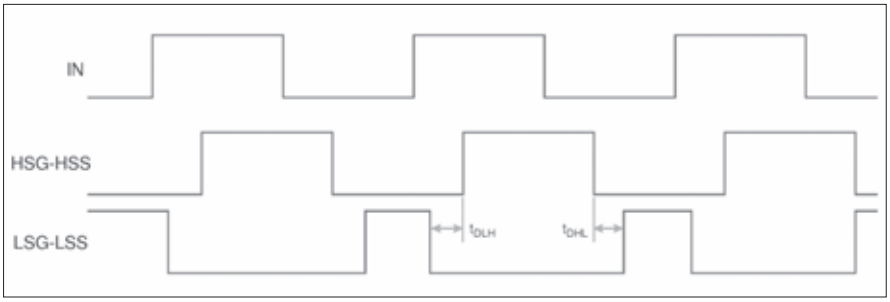
The HS FET gate node will track the duty cycle of the PWM input with a shift in the response, as both rising and falling edges are shifted in the same direction. The LS FET gate node duty cycle can be controlled with the dead-time resistors as each resistor will move the rising and falling edges in opposite directions. RDLH will change the dead-time from low-side gate (LSG) falling to high-side gate (HSG) rising and RDHL will change the dead-time from HSG falling to LSG rising. The LS bias diode and capacitor is included for symmetry only and is not required for the part to function. Removing the LS bias diode will increase the LSG voltage by approximately 0.3V.

Each of the output drivers includes two separate pull-up and pull-down outputs allowing independent control of the turn-on and turn-off gate loop resistance. The low impedance output of the drivers improves external power FETs switching speed and efficiency, and minimizes the effects of the voltage rise time (dv/dt) transients.

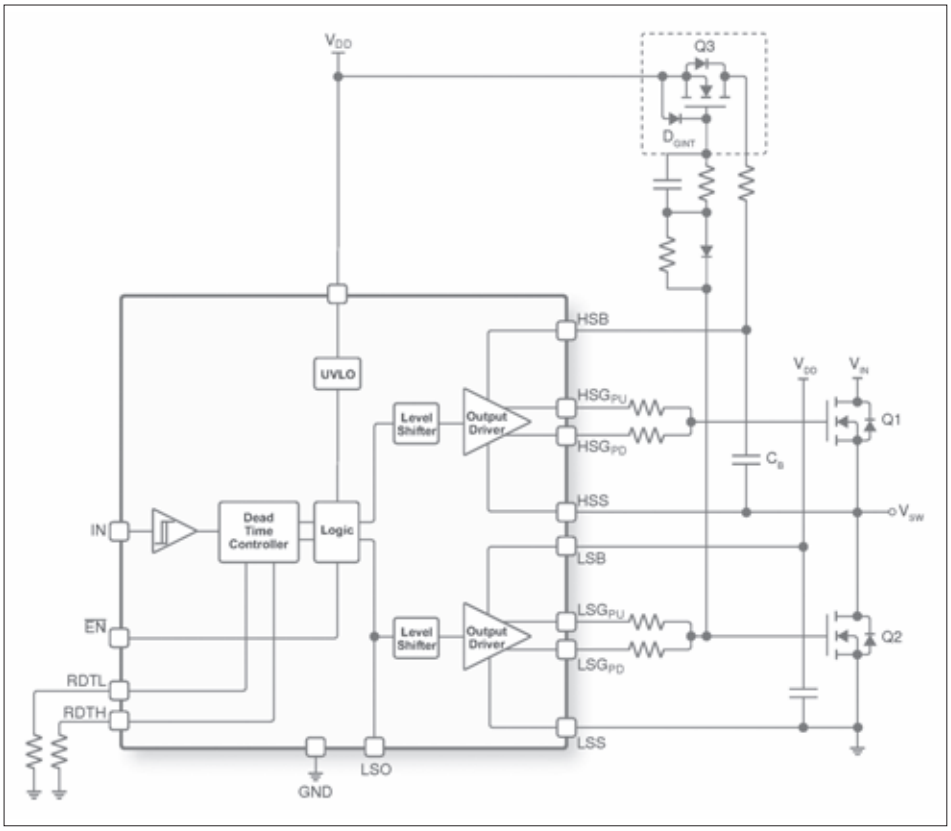
### Application circuit

A typical application of the PE29100 and its external components is a half-bridge configuration. The PE29100 is designed to provide a LS gate driver, referenced to ground, and a floating HS

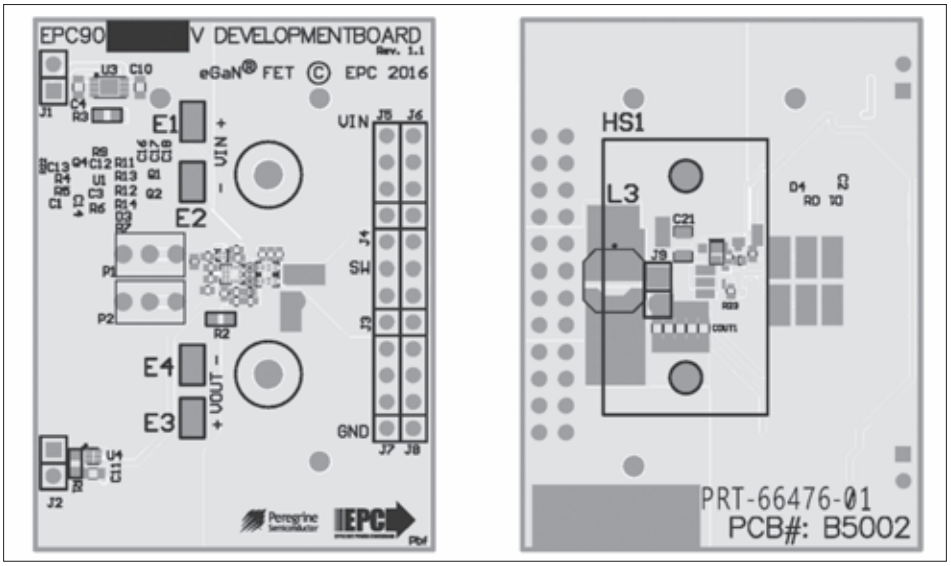
gate driver referenced to the switch node (HSS). A common technique to generate the floating HS gate drive uses a bootstrap diode in conjunction with a decoupling capacitor. However, if the LS device conducts currents through its body diode during the dead-time




**Dead-time generation via resistors affecting the LS output**




**Half-bridge application schematic**




**GaN driver evaluation board**

period, an over-voltage condition across the bootstrap capacitor can result.

A more elegant approach replaces the HS bootstrap diode with an eGaN FET (Q3). The EPC2038 is used as a synchronous bootstrap FET to prevent over-voltage of the HS device. The EPC2038 includes an internal diode and prevents the bootstrap capacitor from over-charging during the dead-time periods. This is accomplished by synchronously switching Q3 using the LSG signal so that Q3 turns on and charges the bootstrap capacitor when LSG is high, but turns off as soon as LSG turns low so that no inadvertent bootstrap overcharging occurs during the dead-time periods.

The external gate resistors are required to de-Q the inductance in the gate loop and dampen any ringing on the FET gates and the SW node. Dead-time resistors RDHL and RDLH can be adjusted to compensate for any changes in propagation delay.

**Evaluation board**

An evaluation board (EVB) was designed to ease customer evaluation of the PE29100 gate driver. The EVB is assembled with a PE29100 driver and two EPC8009 eGaN FETs in a half-bridge configuration. $V_{DD}$ is applied at J1 to bias the driver. $V_{IN}$ is applied between J5–J6 and J7–J8 to supply power to the GaN FETs. A PWM signal with an adjustable duty cycle is applied to J2 as the input. $V_{IN}$ can be monitored at test points E1 and E2, while the DC output can be monitored at test points E3 and E4. The switched output node can be observed on an oscilloscope at J3–J4 and ground (J7–J8).

Because the PE29100 is capable of generating fast switching speeds, the PCB layout is a critical component of the design. The layout should occupy a small area with the power FETs and external bypass capacitors placed as close as possible to the driver to reduce any resonances associated with the gate loops, common source and power loop inductances. Since the maximum allowable gate-to-source voltage for eGaN FETs is 6 V, resonance in the gate loops can generate ringing that can degrade the performance and potentially damage the power devices due to high voltage spikes. Additionally, it is important to keep ground paths short.

**www.psemi.com**

# We look forward to seeing you

## 10-12 April 2018
## NEC Birmingham

AIR-TECH EXHIBITION 2018 · COMPRESSED AIR · VACUUM · GENERATORS

DRIVES & CONTROLS 2018 · THE AUTOMATION, POWER TRANSMISSION & MOTION ENGINEERING EVENT

EUROPEAN OFFSHORE WIND ENERGY 2018

FLUID POWER & SYSTEMS 2018 · The Exhibition for Hydraulics & Pneumatics Industries

PLANT&ASSET MANAGEMENT 2018

SMART MACHINES & FACTORIES 2018

DFA Media Ltd · 192 High Street · Tonbridge · TN9 1BE · tel: +44 (0) 1732 370340 · info@dfamedia.co.uk

# High Quality 150 mm SiC Substrates for Power Electronics Applications

Silicon Carbide (SiC) technology is being more broadly adopted by the power electronic market within applications rated at voltages of 600V or above, whereas silicon-based technology is still preferred for lower voltage class devices. The benefits of SiC devices over silicon-based counterparts are very well-known by the industry and reside in the high temperature resistance, high thermal conductivity and high critical field of SiC. All of these benefits translate into final systems with smaller form factors, higher efficiencies and lower requirements in cooling performance. This article will provide a current picture of the tremendous improvements made over the past few years in order to provide today a commercially available 4H-SiC 150 mm technology approaching and even overpassing the 100 mm technology performance.

**Thomas Seldrum, Associate Application Engineering Specialist, Dow Corning Europe s.a., Seneffe, Belgium**

**The emergence of 150mm SiC wafers** has been a critical element to explain the wide market adoption of this technology, allowing economy of scale at a manufacturing standpoint together with the use of depreciated 150mm silicon production lines that could be converted to accommodate the silicon carbide specificities.

In order to gain even broader market adoption (using larger devices, bipolar devices, higher voltage rating devices) special attention has to be given to the decrease of extended crystal defects and the control of the surface shape and flatness which are key elements needed by lithography tools or designs used by the device manufacturers.

Figure 1: **The control of crystal stress during the growth process is key in order to minimize extended defect densities**

## Control of defect densities

The control of crystal stress during the growth process is key in order to minimize extended defect densities and also to ensure proper control of the shape and the surface flatness of the sliced wafers used for device processing (figure 1). Different extended defects are known to be detrimental to the reliable operation of SiC devices: micropipes (MP), basal plane dislocations (BPD), threading screw dislocations (TSD) and threading edge dislocations (TED):

- Micropipes are killer defects which provoke a premature catastrophic device breakdown;
- BPD have an impact on the generation of stacking faults during the epitaxy process, leading to a drift in the forward voltage drop in bipolar PiN diodes;
- TSD and TED densities impact the reverse leakage current in Schottky barrier diodes.

The summary of the current status of Dow Corning defect density control is presented in Table 1.

Micropipes are no longer a problem to manufacture large area devices. We can achieve a mean micropipe density of less than 0.3/cm$^2$, very comparable to the low density observed in 100 mm wafers. Through optimization of the growth and seed selection processes very good control of the low micropipe defect density has been achieved.

In terms of basal plane dislocations,

| Bulk Crystal | | | |
|---|---|---|---|
| **Defect Metrics** | **Units** | **100mm** | **150mm** |
| Median BPD density | $cm^{-2}$ | 400 | 800 |
| Median TSD density | $cm^{-2}$ | 300 | 200 |
| Median TED density | $cm^{-2}$ | 5200 | 3100 |
| Median EPD density | $cm^{-2}$ | 5900 | 4100 |

Table 1: **Comparison of defect densities in 4H-SiC 100mm and 4H-SiC 150mm substrates**

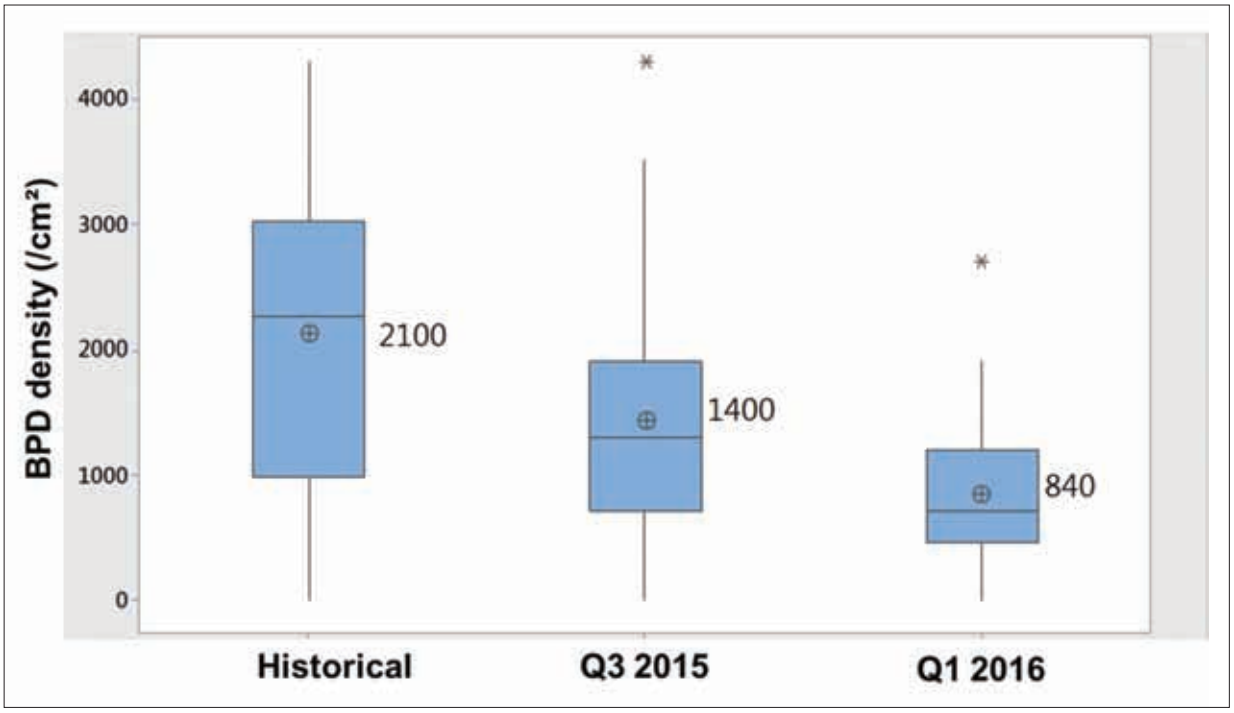



Figure 2: **Evolution over time of BPD density in 4H-SiC 150mm substrates**

the improvements made over the past months in the crystal growth process and wafering control have significantly decreased the median density and the manufacturing distribution has been drastically reduced (Figure 2). The current values are still twice higher than the median BPD density measured on 100 mm wafer, but based on the continuous decrease from the past, we expect that the BPD density will ultimately by at least on par with the 100 mm wafers in a near future.

The threading screw dislocation is very well controlled with a median value of 200/cm$^2$, better than the value for the 100 mm technology.

The threading edge dislocations dominate median total etch pit density of 150 mm substrates (similar behavior is true for 100 mm wafers). However, the 150 mm technology provides a lower median value compared to the 100 mm products.

The conclusion from this section is that the 150 mm technology developed by Dow Corning presents an overall lower defect density compared to the 100 mm substrates. The strong focus in reducing the defect density is a critical factor to ensure the broader adoption of SiC materials in the market.

## Control of the shape and flatness

Together with the reduction of extended defects, it is important to optimize the shape of the wafers via optimized crystal growth, wafering, and polishing processes. This has been specifically challenging for the 150 mm SiC substrates as the thickness of the substrates (350 µm) has been kept identical while switching from the 100 mm wafers to the 150 mm diameter. This constraint is different from what has occurred in the Silicon technology where the wafer thickness increases together with the expansion of the diameter. Maintaining thickness while increasing diameter brings additional crystal stress control requirements for 150 mm SiC.

Nevertheless, Dow Corning has overcome these challenges and 150 mm SiC substrates are now available with bow, warp, and thickness variation metrics meeting the industry requirements for handling in the processing lines (Table 2). Typical bow and warp median values achieved in the mass production lines are -3 µm and 17 µm respectively whereas the total thickness variation falls to a median of less than 5 µm and the local thickness variation (SBIR) median reaches less than 2.5 µm.

## Conclusions

Dow Corning has developed a 4H-SiC 150 mm growth and wafering process in order to meet the challenges of the electronics industry. The defect density is continuously decreasing, with today's 150 mm technology surpassing the incumbent 100 mm technology. This focus is a key factor to ensure a reliable device and high yield through the device processing and electrical wafer sorting steps. In parallel, the shape of the 150 mm wafers remain unchanged compared to the 100 mm substrates, even while the thickness has been kept constant, for an easy transfer of manufacturing processes from 100 mm to 150 mm technology.

| Bulk Crystal | | | |
|---|---|---|---|
| **Shape Metrics** | **Units** | **100mm** | **150mm** |
| Median bow | µm | -0.9 | -2.8 |
| Median warp | µm | 7.9 | 17.1 |
| Median TTV | µm | 2.4 | 4.7 |
| Median SBIR | µm | 1.3 | 2.4 |

Table 2: **Comparison of shape metrics in 4H-SiC 100 mm and 4H-SiC 150 mm substrates**

# Setting a New Standard for Power Semiconductors Tests and Measurements

Continued improvements in the performance of power semiconductors drives demand for corresponding improvements in testing technology. LEMSYS has developed a solution specifically dedicated to fast medium power semiconductor devices. With the new PRO-AC test equipment, both manufacturers and users have now access to a performant and economical solution for dynamic parameter measurement.

**Christian Rod and Pierre Goumaz, LEMSYS SA, Geneva, Switzerland**

**In a world where energy becomes more** and more valuable, efficient power electronics devices are bound to increase their market share. The necessary increase in the production capability implies a specific and adapted solution for testing these new and efficient devices, characterized by fast commutations and a high sensitivity to parasitic elements, such as inductance. In order to provide the market with such an adapted solution, LEMSYS has designed the new PRO-AC test equipment.

## Suited for device qualification and production

The new test equipment is shown in

Figure 1: **Lemsys new Pro-AC power semiconductor test equipment**

different devices and packages. Regarding the inner conception, it follows the goal of maximum simplicity. The repetitive and modular design leads to maintenance down-times as low as possible, increasing as much the production capability and decreasing the need for spare parts stock.

The mechanical adaptor is included in a specifically designed test frame that comprises a heating system for tests at devices rated temperature. This test frame can be used in a semi-automatic way (the user start the test sequence through the graphical user interface) or in a full-automatic way (the test sequence is started by the closure of the device-under-test drawer). Depending on the application, the choice between these two

Figure 2: **Main control software GUI for test edition**

Figure 3: **Display of real-time statistics in the main control software**

modes can be done easily through a dedicated user interface directly on the test frame.

The graphical user interface of the in-house developed control software (Figure 2) has been conceived to limit to its minimum the time required by the edition of a test sequence. It includes a lot of useful functionalities such as the possibility to run a test equipment auto-diagnostic, the possibility to save both plot images and measurement points in case of a failed test for analysis and reporting purposes and the real time statistics (Figure 3) allowing the user to easily keep an eye on the production quality.

## Suited for power GaN tests

Fast switching devices require a test equipment with dynamic parasitic values (inductance and capacitance) as low as possible. The PRO-AC has been designed with the primary goal to provide the lowest parasitic inductance. Indeed, measurements taken directly on the device under test, and therefore including both the test equipment and the adaptor, show a value as low as 37.12 nH, as can be observed on Figure 4.

Such a low parasitic inductance value enables the PRO-AC to perform tests on very sensitive devices, such as the GaN transistor GS66508P, in conditions that create damaging oscillations if performed on other testers.

All common switching values, such as turn-on delay, rise-time or switching losses can be measured through different tests using standard single and double-pulse waveforms. Figure 5 illustrates a turn-on test at the PRO-AC rated voltage and current, respectively 1500 V and 600 A.

Figure 6 illustrates the turn-on behavior of a C3M0065090D SiC device measured on the new

PRO-AC. It can be seen the fast switching capability of the test equipment since the measured rise-time corresponds to the typical value indicated by the manufacturer datasheet, confirming the adequacy of the PRO-AC with the test of wide-bandgap devices.

## Integration of static tests

The last key advantage of the new PRO-AC is its ability to be easily upgraded to a full AC and DC test system. It includes all the standard static tests, such as leakage current and breakdown voltage up to 3 kV, on-resistance and/or forward voltage drop up to 2000 A and gate leakage current measurements down to only a few nanoamps. Thus this test equipment is well suited for both production and qualification tests. Such an upgrade can be done without the need to upgrade

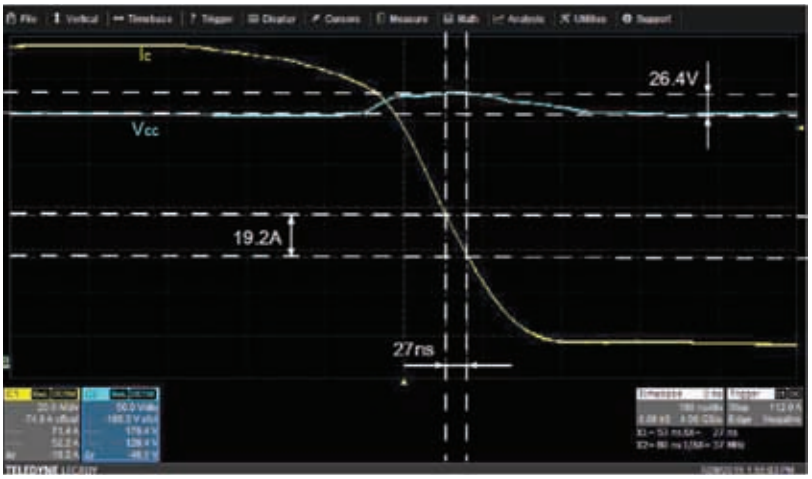



Figure 4: **Effect of the parasitic inductance on the DC-link voltage during a turn-off**


Figure 5: **1500 V/600 A double pulse waveform on a FZ1200R33KF2 IGBT module**

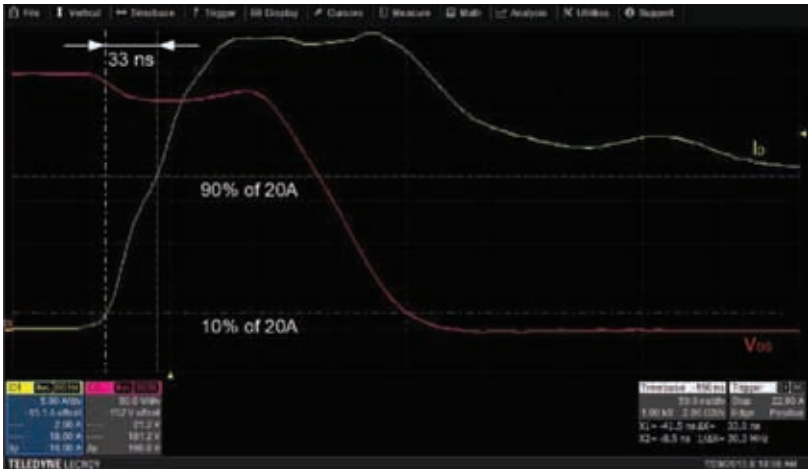



Figure 6: **Turn-on behavior of a SiC device (C3M0065090D)**

the adaptors, since they are fully compatible with LEMSYS full range of testers.

## Conclusion

Developed with the goal to gather both high technical performances and the simplest possible use, the PRO AC-DC product family will integrate a production line as easily as a qualification laboratory. According to the previously presented results, users can expect lowest stray inductance, a solution specifically designed for the new devices generation, simple usage regarding both the graphical user interface and the change of mechanical adaptor, and options including all the standard static tests.

# Quantification of Cracked Areas in IGBT Modules

Degradation of the thermal conduction path is one of the most common failure mechanisms of power semiconductor modules. Typically, solder fatigue happens due to the thermo-mechanical stresses at the interfacing contacts resulting from mismatched coefficient of thermal expansions (CTE) between different materials and causes cracking. Thermal transient measurement using Mentor Graphics' T3Ster® hardware is a characterization method for heat conduction path in power semiconductor packages. **Mohammed Amir Eleffendi, Li Yang, Pearl Agyakwa, and Mark Johnson, Department of Electrical and Electronics Engineering, University of Nottingham, UK**

**The heat flow path in this type of test** can be represented by an equivalent electrical Resistance-Capacitance Cauer-type model. T3Ster uses thermal impedance via "structure functions" as a non-destructive evaluation technique to detect structural defects in the heat conduction path. Junction-to-case thermal resistance ($R_{thjc}$) and cracked area, from structure functions, are compared to the cracked and unattached area estimated by Scanning Acoustic Microscopy (SAM) for a conventional 1.2 kV/200 A IGBT power module that is actively power-cycled to degrade the solder at the substrate-base plate interface. SAM imaging was performed at regular intervals for multiple stages of the power cycling test to observe the gradual degradation of the solder layer. The power module under test was an off-the-shelf 3-phase IGBT module consisting of three substrate tiles mounted on a copper baseplate with two IGBT chips and two free-wheeling diodes.


**Figure 1: High-power multi-chip power modules can be characterized using MicReD Power Tester® 1500A**

## Power module test procedure

The IGBT module was mounted onto a cold plate with a 25 μm thick Kapton film used as an interfacing material between the cold plate and the baseplate. The purpose of this film was to increase the case-to-ambient thermal resistance in order to achieve a temperature swing at the substrate-case interface and so accelerate the degradation of the substrate mount-down solder layer compared to other failure mechanisms. All IGBTs were biased with a $V_{GE}$ = 15 V such that the cycling current IC as well as the measurement current IM were shared between the three legs of the module. The collector–emitter voltage $V_{CE}$ is a global measurement across the whole module and therefore, it represents an "average" measurement of the three legs.

A calibration curve $T_J = f(V_{CE})$ at a constant measurement current of 200 mA was used to calculate junction temperature TJ. The cycling current IC was regulated by the power tester to preserve a constant $\Delta T_J$ = 120 K with $T_{J\,max}$ = 140°C and $T_{J\,min}$ = 20°C as estimated from $V_{CE}$ with the water temperature maintained at 20°C. The heating time and cooling time were fixed at 50 s, and 60 s respectively. This achieved a ΔT of 70 K at the substrate with T max = 90°C and T min = 20°C. The test started with an initial cycling current of 236 A which resulted in a power dissipation $P_D$ = 704 W. As the thermal

resistance increased during the test due to solder fatigue, the cycling current was regulated to keep the $\Delta T_j$ constant.

Under these conditions, the wire-bond lift-off mechanism is not the dominant mechanism and the substrate mount-down solder degrades before any wire-bond lift-off is observed. The power cycling was paused regularly every 1000 cycles, at which time a thermal impedance measurement was made of the module in situ by the 1500A Power Tester (Figure 1) and this resulted in a total of 17 thermal impedance measurements during the test.

SAM characterization was carried out during the power cycling test using a PVA TePla AM300. Scanning acoustic microscopy is a non-destructive technique that allows to image the internal features of a specimen and can detect discontinuities and voids of sub-micron thickness. It creates 2D greyscale images from the reflected ultrasonic echoes.

Defects at any of the internal layers cause discontinuity in the structure and block the ultrasonic signal preventing it from penetrating through the layers beneath the defected areas. Thus, defects in the substrate solder result in a black shadow appearing in the C scan images taken from the chip level (Figure 2). In this way, the C scan images were used to obtain distinct boundaries between the attached and discontinuous areas. However, the exact location of the defects within the structure can be unclear from SAM images, and therefore, correlative metallurgical cross-sectioning was necessary (Figure 3). Figure 4 shows the estimated attached area of the solder layer at different cycle numbers during the cycling test. As the number of cycles increases, cracking propagates through the solder causing the attached area to be reduced gradually until it reaches 43 % attached area after 17,700 cycles.

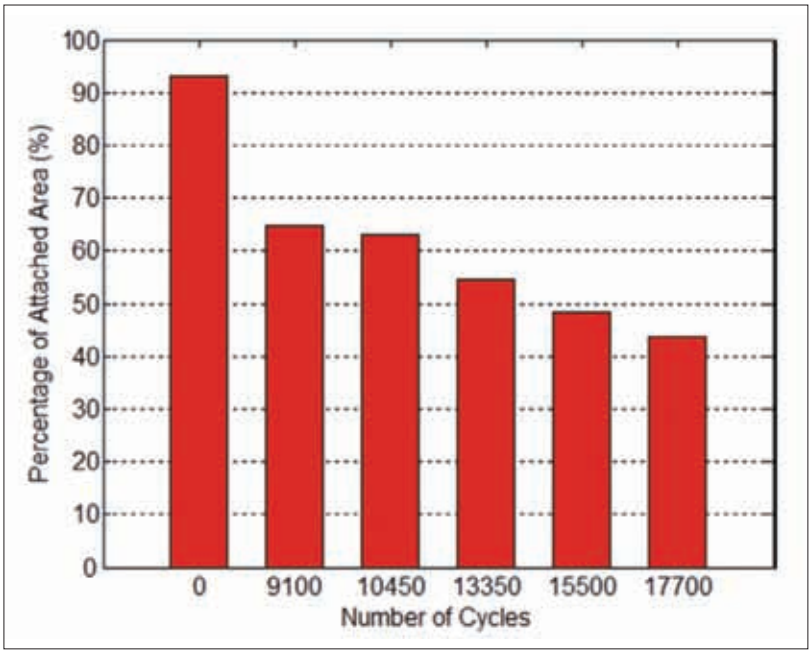



**Figure 4: Estimated attached area of solder layer during the cycling test from SAM images**

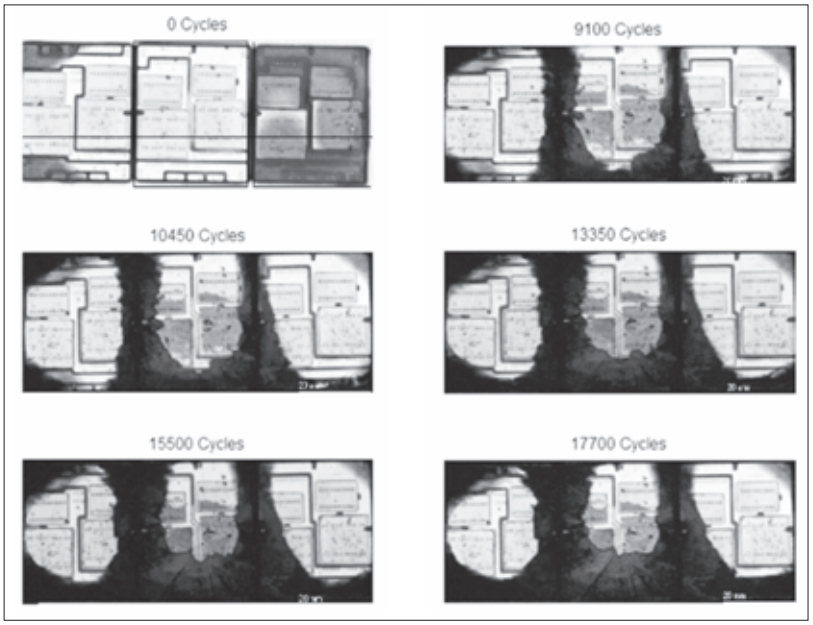
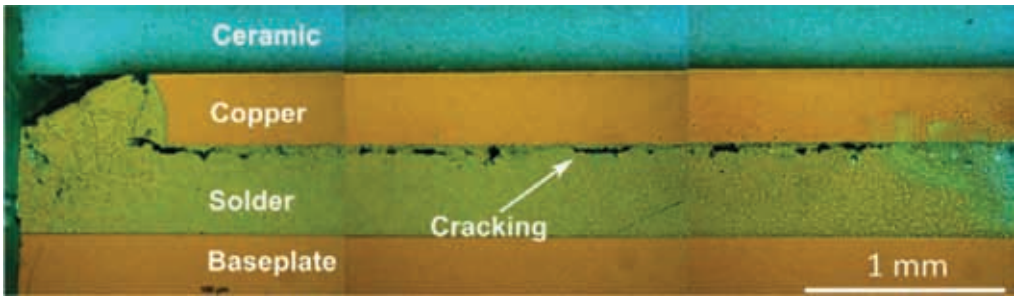



**Figure 2: Scanning Acoustic Microscopy (SAM) images at different cycles during the power cycling test**

The power cycling test was terminated after 17,700 cycles by which time the total junction-to-ambient thermal resistance $R_{thja}$ had increased by 14% from its original value. After examination, all IGBT devices were still electrically functional.

But the SAM image showed different levels of discontinuity beneath the individual IGBT devices. Therefore, an investigation was carried out to examine whether this non-uniformity in heat flow can be observed in the structure functions for the individual IGBT chips in addition to the module as a whole. For this study, thermal paste was used as the interface material instead of the Kapton film used during the power cycling test. The local thermal impedance of each individual IGBT in the module was measured and the structure function was calculated. The attached area under each individual IGBT




**RIGHT Figure 3: Image of metallurgical cross-section showing the cracking resulting from power cycling at the substrate-baseplate interface**

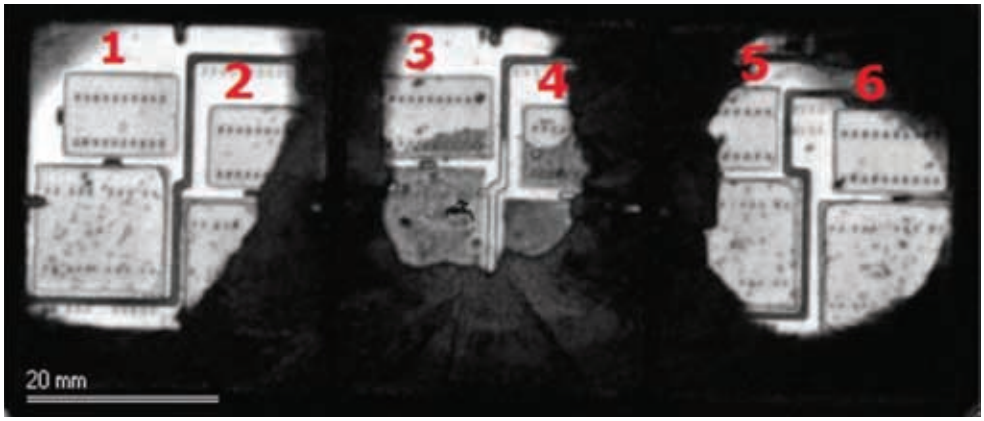



**Figure 5: SAM image of the cycled module at 17,700 cycles shows different levels of delamination under the 6 IGBT devices**

was estimated from the SAM image at 17,700 cycles shown in Figure 5.

The different thermal layers can be easily identified related to Device 1 and Device 6 as they are the least affected by solder fatigue. Features of the different layers in the structure start to disappear as the level of local delamination increases in the other devices. Device 4 is the worst affected by cracking. Hence the thermal resistance $R_{thja}$ may be directly compared with the percentage of attached area below the individual IGBTs.

## Conclusions

An evaluation using MicReD T3Ster structure functions within a Mentor Graphics 1500A Power Tester as a non-destructive testing tool for examining the integrity of the heat flow path in high power multi-chip semiconductor modules under repeated cycling. A 1.2 kV/200 A IGBT power module (with six IGBTs) was power cycled to activate the solder fatigue failure mechanism at the substrate–baseplate interface. Thermal impedance measurements and SAM imaging were performed at regular intervals during the power cycling test. From this data, the thermal structure function was calculated and the cracked area in the solder layer was estimated. Failure analysis by cross-sectioning confirmed the location of the discontinuity at the substrate–baseplate solder layer. A clear correlation was found between the change in the junction-to-case thermal resistance $R_{thjc}$ estimated from the structure function and the remaining attached area of the solder layer calculated from SAM images.

## Literature

*'Cracking Explained', Engineering Edge Vol. 5 Iss. 1-2016, Mentor Graphics Corp.*

*'Field Lifetime Estimation of Power Modules using Active Power Cycling', Power Electronics Europe, November 2015, pages 11-12*

# Low Voltage MOSFET's Behavior in FBSOA

Power MOSFETs working in linear mode need to be correctly designed at the Silicon level in order to improve ruggedness to thermal instability phenomena. In particular, modern Silicon technologies, optimized for high current and high switching frequency environments, could be less safe in linear mode than previous planar technologies, optimized for linear mode. **Filadelfo Fusillo, Senior Market and Application Engineer, and Filippo Scrimizzi, Low Power Market and Application Manager, STMicroelectronics, Catania, Italy**

**Many systems use Power MOSFETs** operating mainly in linear mode (or active region): for example, in a fan controller, the MOSFET works permanently as constant current source, with the fan connected in High Side position. The fan speed can be adjusted by varying the current value and therefore the MOSFET gate-source voltage ($V_{GS}$). In other applications, the device can work in linear mode for short time intervals, passing from ON state to OFF state condition and vice versa. The slower this transition, the more critical the device power dissipation; so, high power capability is required for MOSFETs working in linear mode. With new MOSFET technologies, huge enhancements in conduction and switching losses have been reached thanks to drastic specific $R_{DSon}$ and $Q_g$ reduction, linked to smaller and smaller device die size. These features enable considerable efficiency gain in high switching frequency applications. On the other hand, they could be very risky when the MOSFET works in linear mode because of the reduced power capability.

## Linear mode operation and safe operating area

There are basically two main operation modes for a Power MOSFET working in ON state:

- Ohmic (or triode) region: linear relationship between drain current $\left(I_D = \frac{V_{DS}}{R_{DSon}}\right)$ and drain-source voltage ($V_{DS}$) ; this is a constant resistance region;
- Saturation (or linear) region: the drain current $\left(I_D = k \cdot \left(V_{GS} - V_{TH}\right)^2\right)$ is nearly independent of the drain-source voltage ($V_{DS}$), while it can be adjusted by varying properly the gate-source voltage ($V_{GS}$).

MOSFETs working in linear mode can withstand very high power dissipation levels, due to simultaneous high current ($I_D$) and voltage across it ($V_{DS}$). When a MOSFET works as a switch, it passes continuously from OFF state (high $V_{DS}$ but zero current) to ON state (ohmic or $R_{DSon}$ region). During these transients, the device stays in linear mode for a short time interval; eventually, if these transitions become slower (i.e. high $R_G$ in the gate driving circuit), the device could dissipate high amount of energy. For a power MOSFET, the SOA curve (or Safe Operating Area) defines the maximum value of drain-source voltage ($V_{DS}$) and drain current ($I_D$) for a correct device working. Figure 1 shows an idealized SOA curve for a

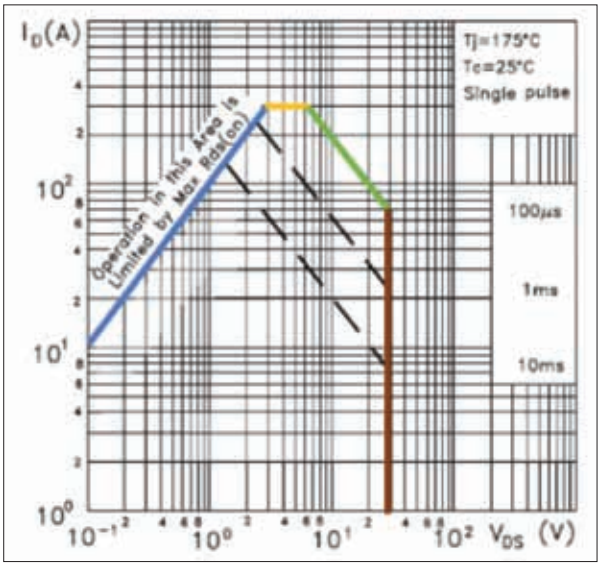



**Figure 1: Idealized MOSFET SOA curve**

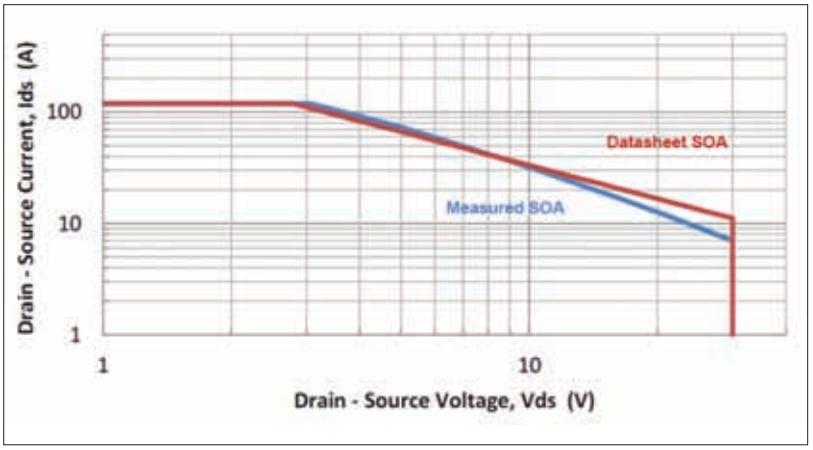



**Figure 2: Measured SOA curve**

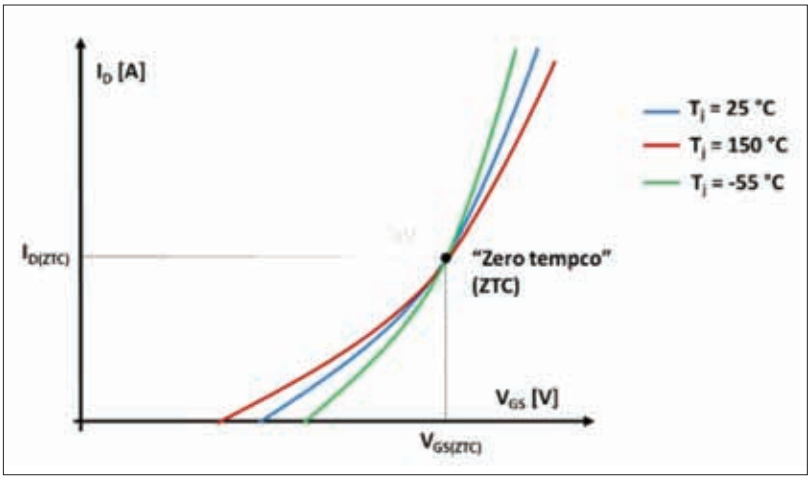



Figure 3: **MOSFET transfer curves and ZTC identification**

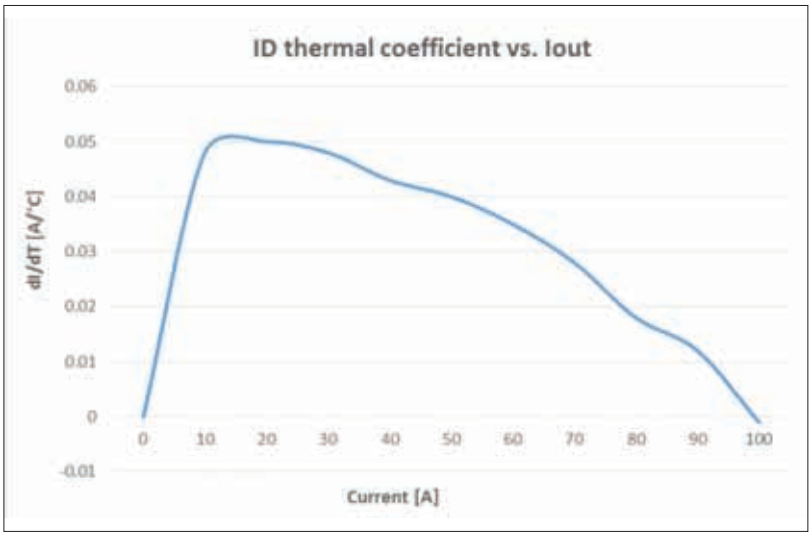



Figure 4: **ID temperature coefficient at T = 25°C**

30 V Power MOSFET, colored lines represent the SOA limits:

- $R_{DSon}$ limit (blue line): for a given $V_{DS}$, $I_D$ value is limited by the maximum $R_{DSon}$;
- Maximum $I_D$ limit (yellow line): maximum current value that the package can manage;
- Maximum power limit (green line): maximum power level allowed for $T_J$=$T_{Jmax}$;
- Maximum $V_{DS}$ limit (brown line): SOA limit defined by device breakdown voltage.

Unfortunately, real devices show different behaviors in the "maximum power" zone of the SOA at high drain-source voltage. This is linked to the "thermal instability" phenomenon, which affects Power MOSFETs working in linear mode. In fact, when the electric power generated into the device is higher than the power dissipated, the device is not able to sustain the power pulse any longer. This failure mechanism can happen even inside the idealized or theoretical SOA curve and also at low drain current values [1]. The difference between theoretical and measured SOA, for a 30V device, is explained in Figure 2.

## Thermal coefficient of drain current

The transfer characteristic of a Power MOSFET shows the drain current ($I_D$) as a function of gate-source voltage ($V_{GS}$) at a fixed junction temperature ($T_J$); this curve is a common datasheet parameter. Considering the negative temperature coefficient of the threshold voltage $\left(\frac{\Delta V_{GS(th)}}{\Delta T}\right)$, the transfer characteristics at three different junction temperatures (-55°C, 25°C and 150°C) are plotted in Figure 3.

The three curves intersect at a cross-over point called zero temperature coefficient (or "zero tempco", ZTC); in other words, for $V_{GS} = V_{GS(ZTC)}$, the device current remains stable with the temperature. For $V_{GS} > V_{GS(ZTC)}$, when the device temperature rises up, the drain current tends to decrease, reaching thermal stability conditions. And vice versa: for $V_{GS} < V_{GS(ZTC)}$, the drain current thermal coefficient is positive; when a small die zone becomes hotter than adjacent area, it conducts more drain current, creating more heat. This, in turn, allows more current to flow, due to a lower threshold voltage (negative $V_{GS(th)}$ temperature coefficient). Finally, this die area can conduct a huge amount of current, which can push the device to failure (thermal runaway) if appropriate limitations haven't been fixed up. Lower voltage and current values of ZTC reduce the zone with a positive temperature coefficient thus increasing the device thermal stability. Deep analysis on MOSFET technologies and Silicon characteristics highlight that there is a strict link between ZTC and MOSFET transconductance ($g_{fs}$): the higher gfs the higher the ZTC. Consequently, the device could work more likely in an unstable zone [2]

Modern MOSFET technologies, which guarantee excellent performances in high switching frequency and high power applications, show ever growing $g_{fs}$ values and tend to be inherently less robust to

| | Technology | $BV_{DSS}$ [V] | $R_{DSon,typ}$ [mΩ] |
|---|---|---|---|
| Device #1 | Std. trench | >40 | 1.7 |
| Device #2 | Optimized planar (for lin. Mode) | >40 | 3.6 |
| Device #3 | New advanced trench | >100 | 2.3 |
| Device #4 | Advanced planar | >100 | 4.5 |

Figure 5: **ST DUT main features**

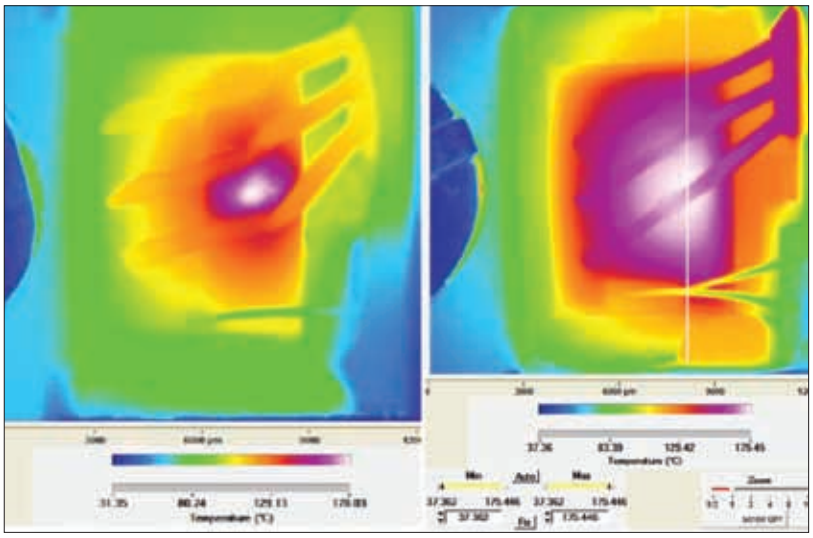


Figure 6: **Die temperature at VDS = 10 V (std. trench tech. on the left, optimized planar tech. on the right)**

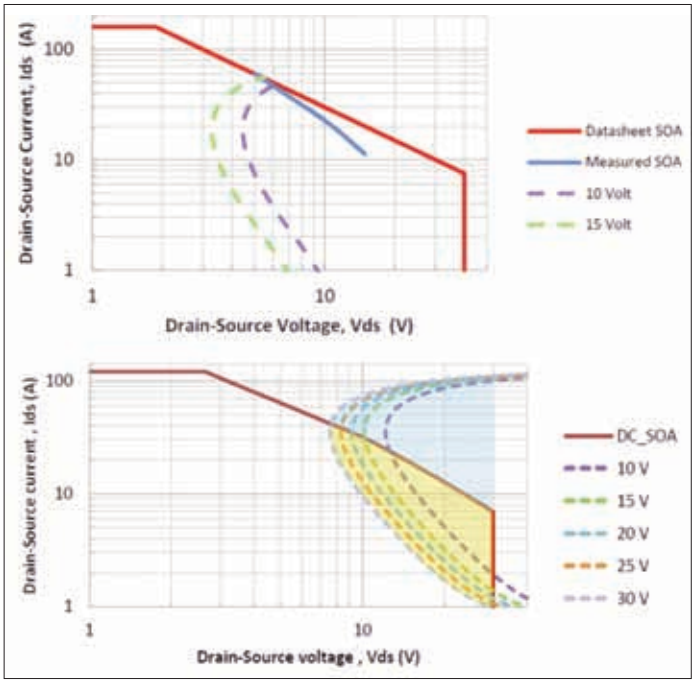



Figure 7: **Standard trench (upper) and optimized technology for linear mode (lower) thermal runaway boundaries**

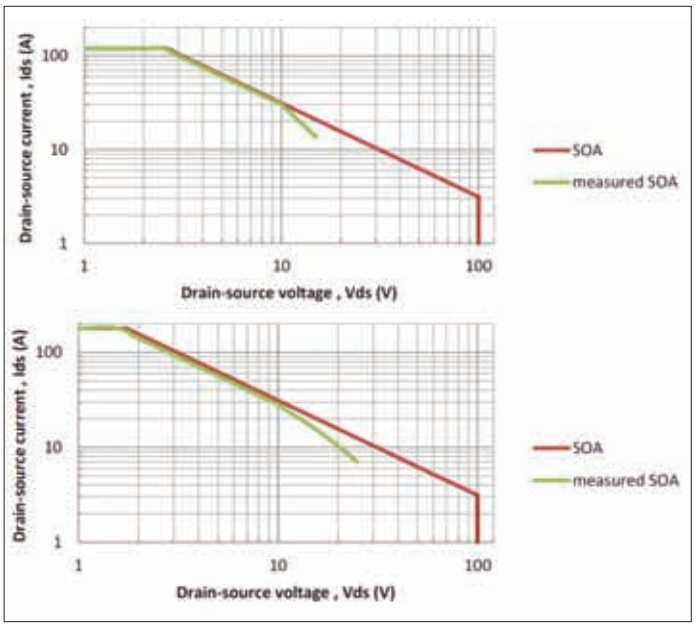



Figure 8: **Measured SOA for advanced planar (upper) and new advanced trench technology device (lower)**

thermal runaway or hot spot phenomena. In Figure 4 the drain current temperature coefficient is depicted as a function of the drain current (T = 25°C).

Thermal instability phenomenon occurs when the device cannot dissipate all the electric power generated. In other words, if $P_G$ is the electrical (or generated) power and $P_D$ is the thermally dissipated power.

## ST's MOSFET characterization

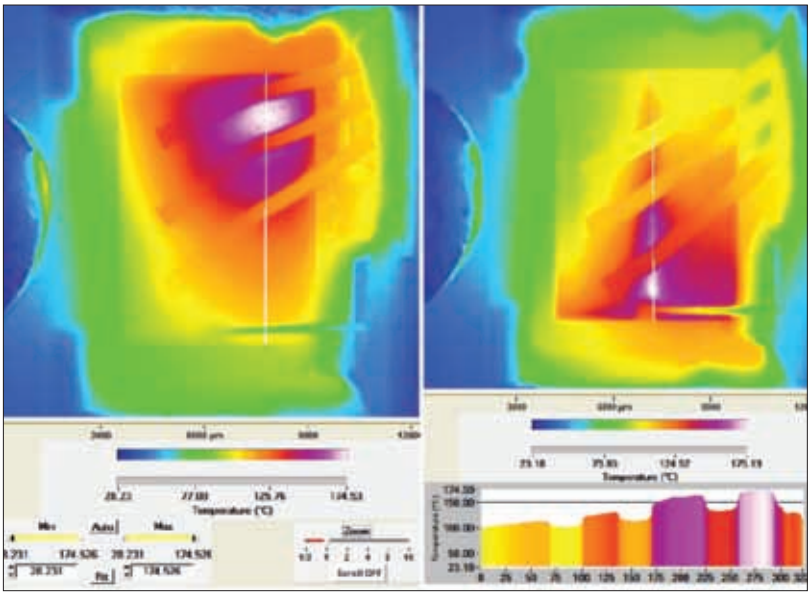
There is a strict correlation between Silicon technology features and MOSFET performances in linear mode. The device ruggedness to thermal runaway and resulting failure can be evaluated by properly combining the SOA curve and drain current thermal coefficient. Furthermore, the $R_{th}$ trend with $V_{DS}$ and junction temperature gives additional information about device performances in linear mode. We performed two different technology comparisons between ST MOSFETs: in the first one, standard trench technology is compared with optimized planar technology for linear mode working ($BV_{DSS}$ = 40 V). In the second comparison, the 100 V device realized in the new advanced trench technology is compared with an advanced planar device (Figure 5).

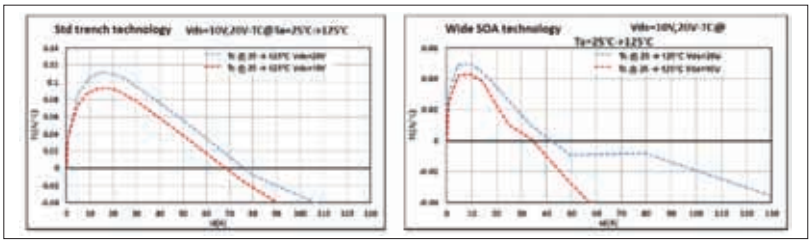
The Standard trench device shows noticeable current focusing phenomena at $V_{DS}$ > 10 V (Figure 6, left image). The reduction of the die active area implies an increase of the device's $R_{th}$ and worse power management. On the other hand, the planar technology optimized for linear mode device shows more uniform die temperature (Figure 6, right image) and a softer Rth trend when VDS increases, with better power dissipation capability. The area between the DC SOA and thermal coefficient curve is the thermal instability zone (Figure 7). The larger this area is (inside the SOA), the less robust the device is in linear mode.

Standard trench technology is able to work without failure in linear mode only at low $V_{DS}$ and $I_D$; it's not possible to test above $V_{DS}$ = 15 V (T > $T_{j max}$ = 175 °C). On the other hand, optimized planar technology guarantees better performance and higher power dissipation capabilities in linear mode at higher voltages as well as at lower voltages.

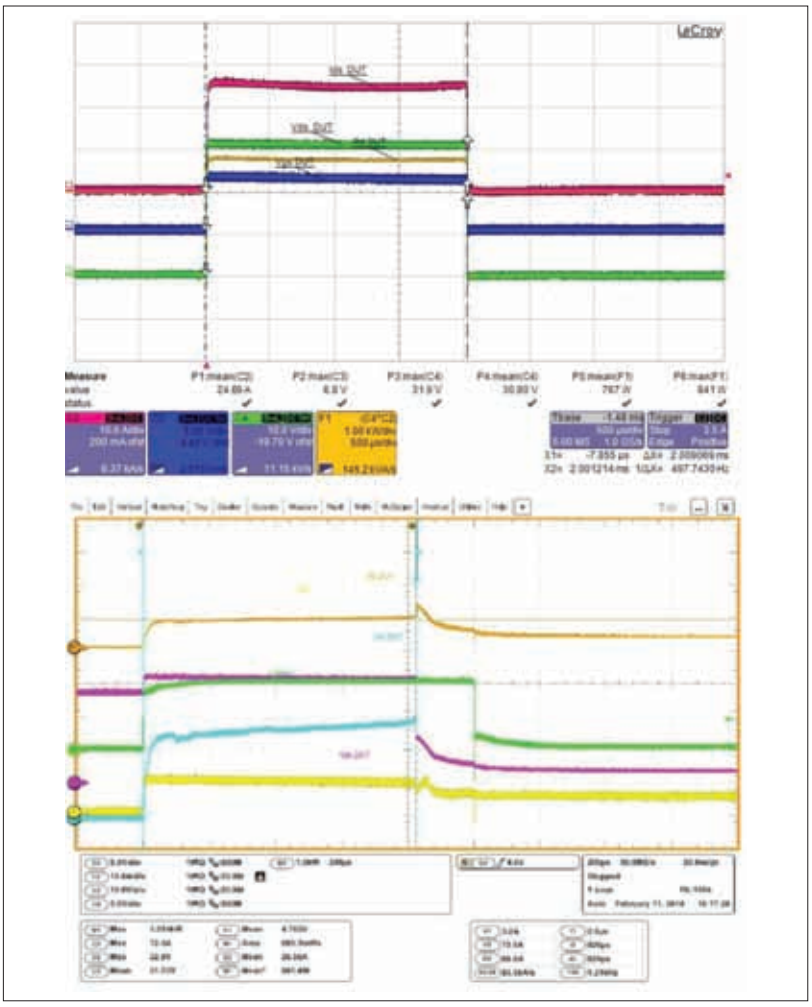
The new advanced trench technology outperforms advanced planar technology in linear mode operation because it is thermally stable for a wider range of operating conditions inside the SOA. Figure 8 illustrates the measured SOA curves for the two technologies.

The new advanced trench device is able to pass the linear mode test up to 25 V, while the advanced planar one fails for $V_{DS}$ > 15 V. Figure 9 shows the relevant






ABOVE Figure 10: **Standard trench (left) and wide SOA (right) thermal coefficient curves**



LEFT Figure 11: **Wide SOA (upper) and standard trench (lower) waveforms in hot swap applications**

LEFT Figure 9: **Thermal picture at VDS = 15 V (left) and VDS= 25 V (right)**

thermal pictures at $V_{DS}$ = 15 V (advanced planar device, left image) and $V_{DS}$ = 25 V (new advanced trench, right image).

Another reason the new advanced trench technology device achieves better performances in linear mode is because of its slightly higher threshold voltage ($V_{TH}$), ensuring quicker device turn-off and hence more ruggedness when biased in linear mode. In order to further improve linear mode ruggedness, ST has introduced a technology able to meet a wider SOA capability together with very low $R_{DSon}$. Figure 10 shows the comparison in terms of thermal coefficients between a standard low $R_{DSon}$ trench technology and its equivalent die-size wide SOA.

The wide SOA device has lower maximum thermal coefficient and narrower positive coefficient area (thermal instability zone for MOSFET); this means higher robustness in linear mode operation. As shown in Figure 11, when the device works in hot swap configuration with $V_{DS}$ = 30 V and $I_D$ = 25 A (typical working condition in a telecom environment), the wide SOA device is able to survive at least 2 ms, which is the minimum time gap required by primary customers. On the other hand, a standard trench FET fails after 800 µs.

## Conclusions

Modern Silicon technologies, optimized for high current and high switching frequency environments, could be less safe in linear mode than previous planar technologies, optimized for linear mode, due to high values of $g_{fs}$ and ZTC. So, it takes a dedicated device design, especially for new advanced trench technologies, to enhance the performances in linear mode, especially in the worst operating conditions (low $I_D$ and high $V_{DS}$), and when in higher $V_{DS}$ and $R_{th}$ such a dedicated design can create the right conditions for current focusing and hot spot events.

## Literature

*[1]. "Thermal instability of low voltage Power MOSFETs," A.Consoli, F.Gennaro, A.Testa, G.Consentino, F.Frisina, R.Letor, A.Magri' – IEEE Transactions on Power Electronics, Vol.15, N.3, May 2000.*

*[2]. AN-4161, "Practical considerations of Trench MOSFET stability when operating in linear mode," Fairchild Semiconductor.*

# TARGET YOUR BUYERS

FROM OVER 60,000
QUALIFIED CONTACTS

- **E-CAMPAIGN**
- **LIST RENTAL**
- **LEASE**

DFA media **Direct**

**Contact:** Ian Atkinson
on +44 (0)1732 370340
ian.atkinson@dfamedia.co.uk

Plant&Works Engineering
Drives&Controls
POWER ELECTRONICS EUROPE
Hydraulics&Pneumatics
THE JOURNAL OF FLUID POWER AND SYSTEMS

# Powering Up and Down in Sequence

Power sequencers are commonly used in system-level board designs where multiple power supplies are enabled in a sequential manner. Engineers, however, can easily implement a power sequencer design with a small microcontroller, and this can be modified to control varying numbers of voltage modules in different designs. **Stan D'Souza, Technical Fellow, Microchip Technology, Phoenix, USA**

**Typically, systems using a power** sequencer have different components on them that require different power supply voltages and power levels. The sequence of enabling the different voltages would ensure that there is no conflict between components being powered up and all units are powered up correctly. When shutting down the system, there may also be a sequence. The power-up and power-down sequences are programmable and time based.

Take, for example, a four-channel power sequencer in which the four voltages are 5.0, 3.3, 2.5 and 1.8 V. Each of these voltages is provided through a power module (PM). These PM units typically have five pins: input and output power, ground, enable, and trim. Users are not limited to four PMs as a modular format can support up to ten PMs that can be added or removed to meet specific needs.

An enhanced core Microchip PIC16F1509 device was selected as the MCU for this application. The peripherals used were GPIO, timer1, ADC, I?C and PWM.

The PM units can be off-the-shelf power supply blocks, sold with specific current and power capabilities. The PM used in this design is the VRAE-10E1A0 made by BEL Power Products. Each PM has five pins: input voltage ($V_{IN}$), output voltage ($V_{OUT}$), ground, enable input and output trim. The enable signal is active-high and, when enabled, the PM output voltage appears at the output voltage pin. The trim pin with the associated $R_{trim}$ resistor allows the output voltage to be set as desired.

The voltage at the trim pin is typically around 0.591 V. A DC voltage at the trim pin also allows the system to provide some voltage load regulation of $V_{OUT}$. In this design, the DC voltage is provided by a PWM-driven RC filter circuit that provides a DAC output to the trim pin. Alternately, this DC voltage can be provided by using fixed resistors from the trim pin to GND with no PWM trim DAC voltage. With this option, the PWM, with its associated hardware and firmware in the microcontroller, would be eliminated.

## Power up

The PIC16F1509 operating at 5.0 V and 4 MIPS using the internal RC clock was used to control the power-up sequence. The power-up sequence is initiated by a serial command using the I²C interface and pressing a push button.

Each PM is sequenced on at a set time interval from 1 to 16,393 ms (16.4 s) with a 1 ms accuracy. For example, PM1 can be started at 10 ms from the start command, followed by PM2 at 25 ms, PM4 at 200 ms and PM3 at 1000 ms. Each PM has a corresponding on-time value, which is a 14 bit unsigned integer value in firmware. This value is compared with a timer value incremented every millisecond. If a match between the timer value and the on-time value of the PM occurs, then the corresponding PM is turned on.

The on-off timing can be selected by the user and is saved in flash on the microcontroller. The on-off sequence can be started and stopped using the serial I²C GUI.

When a PM is turned on, the corresponding PWM output is enabled and $V_{OUT}$ is monitored via the microcontroller's ADC. The PWM duty cycle corresponds to the 8 bit DAC value for the PM. This DAC value can be changed by the user in the GUI or in the firmware.

The trim voltage is created by using a combination of $R_{trim}$ and the PWM output from the microcontroller. This PWM output is sent to an RC filter to create a DAC voltage, which, in combination with the trim-resistor, is applied to the trim pin of the PM. The output of the PM is monitored using a 10 bit ADC converter on the microcontroller.

Each PM voltage is averaged over 16 readings to give a 14 bit value. Only the most significant eight bits of this value are used to reference the $V_{OUT}$ voltage value of each PM. The reference voltage of the ADC is $V_{DD}$ or 5.0V. For example, if the PM output voltage is 2.5 V, then the accuracy of the measurement would be (2.5 V/5.0 V)/256 = 1.95 mV. All output voltages are constantly monitored to verify they are within the specified over and undervoltage limits specified. If the PM voltage goes above or under the under or overvoltage limits, then a failure is signaled and the system is automatically shut down.

## Power down

The MCU also controls the programmable power-down sequencing of the four power modules. The power-down sequence is initiated on a serial command from the I²C, any fault condition on the PMs or input voltage, and pressing a push button.

Each PM is sequenced off at a set time interval from 1 to 16,393 ms (16.4 s) with a 1 ms accuracy.

For example, PM4 can be shut at 20 ms from the stop command, followed by PM2 at 25 ms, PM3 at 200 ms and PM1 at 1000 ms.

Each PM has a corresponding off time value, which is an unsigned integer (14 bit value). This value is independent from the on-time value. This value is compared with a 16 bit counter value incremented every millisecond. If the two are equal, then the corresponding PM is turned off.

The off-time values are user selectable and are saved in flash. In case of a fault condition power-down, a new power-up sequence will be automatically initiated depending on the number of retries selected by the user. Typically, a user may specify two or three retries. After all retries return a failure, the system is shut down and the fault condition is signaled.

Using the I²C GUI interface, the user can figure out which PM condition or input voltage caused the failure. The user must take the appropriate corrective action to remove the failure condition and reset the system using the I²C serial command or the GUI, and then retry the power-up sequence.

## Microcontroller

Since four channels of PMs are used in

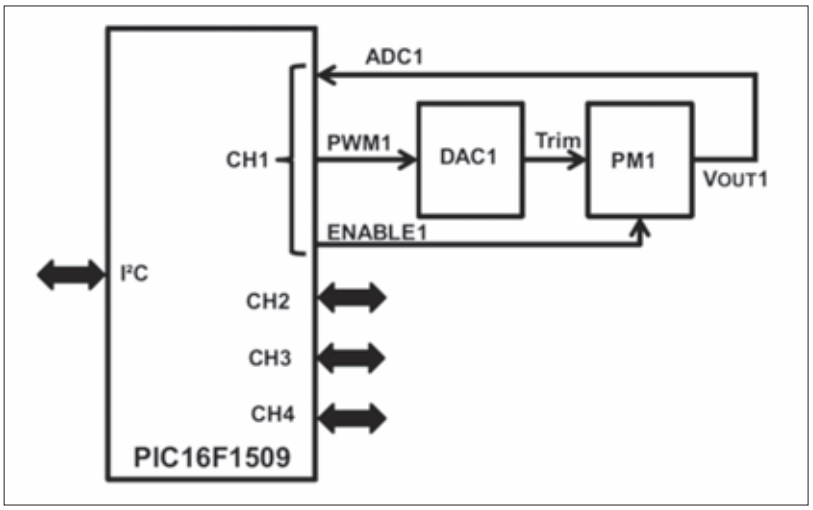



**Figure 1:** System block diagram

this design, at least four IO lines for the enable and disable function are required. Also required are four ADC channels, four PWM outputs and two lines for I?C. An additional ADC channel was used to sample the input voltage, the MCLR, the VDD, the VSS and the programming pins; a total of 20 pins. Figure 1 shows the system block diagram.

The MCU is powered by 5.0 V via a 5 V regulator. The internal 16 MHz RC clock is used to run the CPU at 4 MIPS. The hardware and firmware can be modified to accommodate up to ten PMs. If more PMs are required, the number of IOs will increase and a larger microcontroller would have to be selected. If fewer PMs are required, then a smaller device can be used.

The trim voltage requirements can also be adjusted. If the user wants to trim the PMs using only the external resistor, then the DAC voltage and the associated PWM is not required. The software to drive the PWM and DAC will also be eliminated. Each PM has its own normal over and under-voltage limit. The PMs also have margin under and over limits for the trim voltage.

An I?C slave interface is implemented on the MCU for serial communications with an external I²C GUI. An MCP2221 I?C-to-mini-USB interface chip can be implemented by users in their own hardware or, if required, they can implement a different I²C interface.

All the firmware for IO, timer1, ADC, PWM, flash memory and I²C peripherals has been created and initialised using the free MPLab Code Configurator (MCC) software.

The ADC routine essentially runs through and samples the voltage of modules 0 to 4. Module 0 corresponds to the input voltage, which always gets monitored for a failure. A failure of the input voltage causes a shutdown. No retries will be attempted. The 10 bit ADC routine samples each voltage 16 times and then uses the average 8 bit value to check for an error with the corresponding under- and over-voltage limits.

In the hardware used, the voltage reference is 5.0 V or $V_{DD}$ of the system. A 5.0 V reference will work fine when sampling and converting 1.8, 2.5 and 3.3 V. However, for the 5.0 V module and the input voltage, a resistor divider is needed to bring the full-voltage range within the 5.0 V reference.

The resistor divider factor for the 5.0 V module is 0.55 and the input voltage divide factor is 0.239. Users will have to use this value during the calculation of the under- and over-voltage limit values and define them appropriately in the header files. This is especially true if the user decides to use values other than those used here.

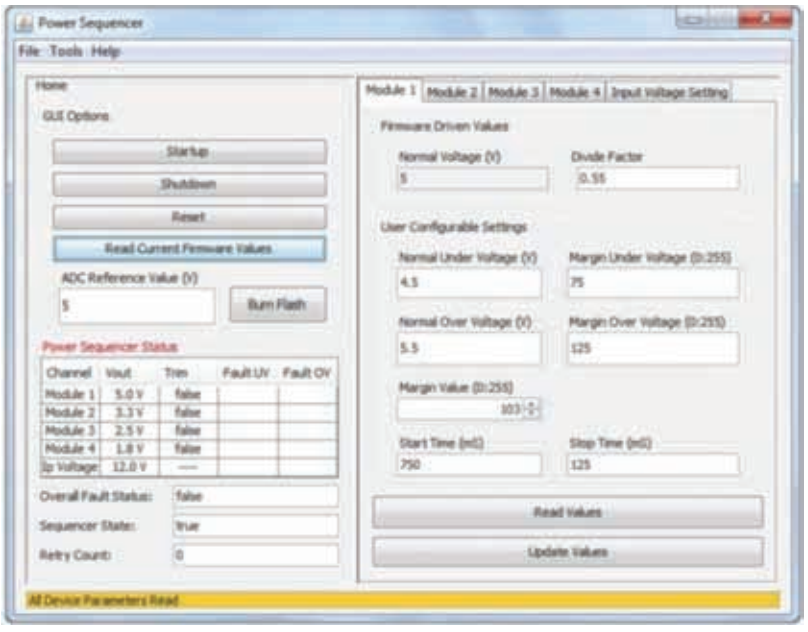



**Figure 2:** Power sequencer graphical user interface (GUI)

### Power sequencer GUI

The power sequencer GUI has been designed for the user to enter relevant data, monitor relevant data and control the power sequencer application. The GUI is shown in Figure 2. The main window has the system options on the left and the module options as tabs on the right.

In the system options, the user can start, stop, reset and read the current firmware values. The status window allows the user to define the $V_{OUT}$ corresponding to the module index. These values can be modified by the user and will be saved when the GUI is closed. The user can also enter the ADC reference value, which for this application note is set at 5.0 V. Finally, the user can burn the updated module settings onto the flash program memory by clicking on the burn-flash button.

Under each module tab, the user can

also set or read existing values for each module. Module 1 is the 5 V module and the user can set the normal and margin, over- and under-limits for this module, along with start and stop times in milliseconds. Also, the voltage divide factor can be edited and entered in this tab. In each module tab, the DAC value can be incremented or decremented using the up and down arrow at one side of the DAC value box. The value increments or decrements and, if the module is on, then the output voltage will be read and updated.

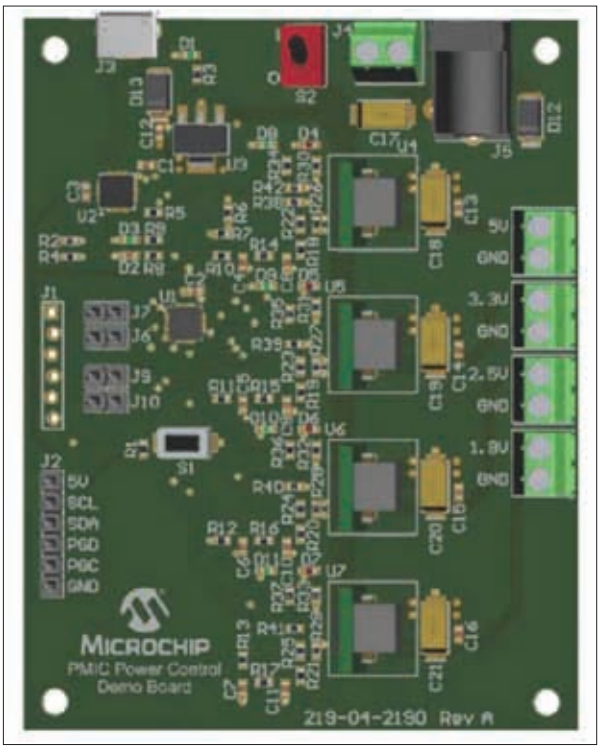



**Figure 3: Power control demo board**

To see the voltage change, more than one increment or decrement may have to be performed. This feature allows the user to increase or decrease the output voltage during a system test when voltages reach their limit. This is called voltage limit testing and allows the user to test a complete system when one or more of the output voltages reaches their under- or over-voltage limits. The voltage values are displayed as actual voltage values (3.3 or 2.5 V). The DAC value and the margin limits are displayed as 8 bit values from 0 to 255.

## Conclusion

An engineer can implement a power sequencer using a PIC16F1XXX device. The user can easily modify this to control four voltage modules in their own design. Additionally, they can add more power modules to their applications or remove modules for a smaller application. The hardware and firmware have been created in a modular format to accomplish these goals easily. The completed board is shown in Figure 3.


# Fast Isolated Gate Driver for High-Voltage Applications

Developed for high-voltage applications where isolation and reliability is required, the UCC21520 from Texas Instruments delivers reinforced isolation of 5.7 kV RMS along with a common mode transient immunity (CMTI) greater than 100 V/ns, and it has a propagation delay of 19 ns and channel-to-channel delay matching of less than 5 ns which enables high switching frequency, high-power density and efficiency. To fully enhance the performance of the latest high-voltage power semiconductors, such as SJ MOSFETs, trench/field stop IGBTs, SiC and GaN transistors, a universal gate driver becomes a critical interface which not only supports enough peak source/sink current, but also facilitates fast dynamic response with robustness and protection for higher switching frequency and higher efficiency applications. The universal capability of the UCC21520 with up to 18 V $V_{CCI}$ and 25 V $V_{DDA}$/$V_{DDB}$ allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver with MOSFETs, IGBTs or SiC MOSFETs. The two output buffer stages of UCC21520 provides 4 A source and 6 A sink current, which provides satisfied rising and falling time (<30 ns) with load capacitance up to 10 nF. However, in some scenarios where the load is larger than 10 nF, external totem-pole buffer stage with discrete transistor should be applied for achieving required rising and falling switching time. It has two identical designed channels with both propagation delay matching and pulse width distortion less than 5 ns, which make it possible to parallel the output channel and double the gate drive strength.

**www.ti.com/UCC21520-pr-eu**

## Parameter Analyzer for Characterizing Semiconductor Devices

Tektronix introduced the 4200A-SCS parameter analyzer that accelerates (power) semiconductor devices, materials and process insights. The new 4200A-SCS instrument features a modern industrial design, a new graphical user interface and a range of helpful self-learning tools such as expert instructional videos embedded into the instrument, compared to the established 4200-SCS. This is particularly important for applications such as semiconductor device research, device failure analysis or reliability testing where instruments are a shared resource among multiple users. Consisting of Source Measure Units for I-V characterization, Capacitance-Voltage module for AC impedance measurements, and Ultra-fast Pulse Measure Unit that performs pulsed I-V, waveform capture, and transient I-V measurements, the 4200A-SCS provides critical parameters needed for materials research, semiconductor device design, development or production. Knowing that various measurements adds additional complexity to semiconductor research, also the 4200A-CVIV four channel IV/CV switch module will be offered. This module for use with the 4200A-SCS mainframe provides on-the-fly switching between SMU (I-V) and capacitance-voltage (C-V) measurements, allowing users to move C-V measurements to any device terminal without lifting prober needles or moving cables.

**www.tek.com/parameter-analyzer**

## Protecting Lithium Batteries from Thermal Runaway

Although Lithium-Ion battery cells and packs typically feature active and passive safety devices and protection circuitry to prevent or mitigate potential cell failures, the last resort is typically a mechanical safety vent that is intended to release the internal pressure of the cell or pack when a specified pressure is reached. One of the most popular pressure relief devices for lower-pressure applications is the rupture disk, a passive pressure relief device long adopted by the Oil, Gas and Chemical process industries to protect pressure vessels, tanks and other equipment from over-pressurization. Rupture disks are available in various designs, sizes, shapes and set pressures and can be installed on cylindrical, button, prismatic, or pouch cell designs.

However, as battery cells become increasingly smaller, so must the rupture disks that protect them.

Miniaturization of rupture disks presents unique challenges, best met utilizing reverse buckling technology. Unlike traditional forward-acting disks where the load is applied to the concave side of a dome, in a reverse buckling design, the dome is inverted toward the source of the load. Reverse buckling disks are typically sturdier than forward-acting disks which are thin and difficult to handle, and as a result have greater longevity, accuracy and reliability over time. But as burst diameters decrease dramatically it becomes challenging to design a reverse buckling disk that will reliably collapse through such small orifice sizes. To resolve this issue, BS&B has created novel structures that control the reversal of the rupture disk to always collapse in a predictable manner. This includes a hybrid shape that combines reverse buckling and forward bulging characteristics that are pre-collapsed. In this type of design, a line of weakness is typically placed into the rupture disk structure to define a specific opening flow area when the reverse type disk activates. Small, nominal size rupture disks are sensitive to the detailed characteristics of the orifice through which they burst which requires close cooperation between the rupture disk manufacturer and the user to achieve the optimum mounting and installation arrangement. With small size pressure relief devices, the influence of every feature of both the rupture disk and its holder is amplified. For miniaturized products, BS&B manufactures the rupture disk from Stainless Steel, Aluminum and Nickel alloys to achieve compatibility with lithium battery operating conditions.

**www.bsbsystems.com**


ROHM Semiconductor showcased its new 3 gen SiC power module BSM180D12P3C007 rated at 1200V/180A which integrates mass-produced trench SiC MOSFETs and SiC SBDs in the same footprint like previous modules. The new module implements SiC-MOSFETs with their advanced UMOS structure going without JFET region and maximizing SiC characteristics. It provides low on-resistance together with high speed switching performance, and - thanks to the extremely low forward voltage and the fast recovery performance of the built-in SiC-SBDs - it has almost no recovery loss. According to the manufacturer, the module achieves 77 % lower switching loss than conventional IGBT modules and 42 % lower switching loss than planar SiC modules utilizing a 2nd gen SiC-DMOS structure. This not only enables high-frequency operation but also contributes to smaller cooling systems as well as smaller peripheral components which in consequence paves the way to greater energy savings and end-product miniaturization.

**www.rohm.com/eu**

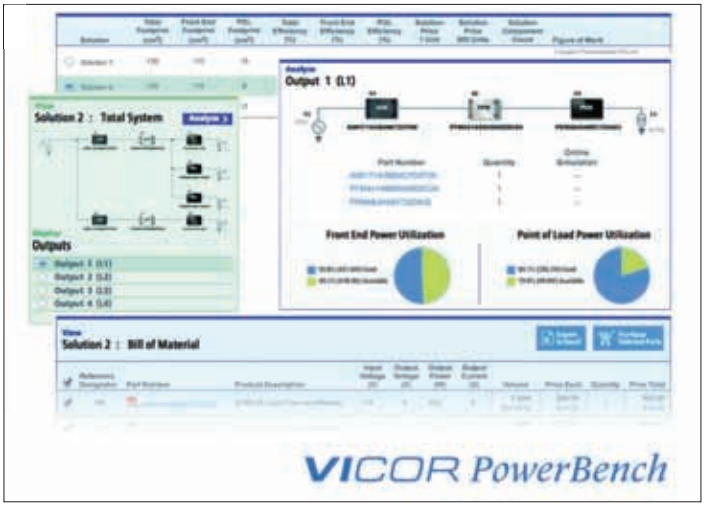
# 600 V/5 A HV-IPD Simplifies PWM Control of BLDC Motors

Toshiba Electronics Europe has expanded its HV-IPD (high-voltage intelligent power device) line-up with a 600 V, 5.0 A part for PWM control of BLDC motors. The TPD4207F combines controller and driver logic, high-voltage MOSFETs in a three-phase bridge output, bootstrap diodes and comprehensive protection functionality. Full control of a BLDC motor is achieved by simply applying signals from a host microcontroller or motor controller IC to the TPD4207F inputs.


Super Junction MOSFETs (DTMOS IV) and driver IC are employed in a multi-chip configuration. The package has been designed by separating all small signal pins from the power pins. Built-in functionality includes over-current and under-voltage protection and thermal shutdown. The TPD4207F is supplied in a compact SOP-30 package with a footprint of 20.0 mm x 11.0 mm x 2.0 mm. Typical on resistance is just 0.44 Ω. Suitable for high-efficiency, low-noise sine-wave motor control, the new HV-IPD allows μdead-time to be configured from a minimum of 1.0 μs.

**www.toshiba.semicon-storage.com/eu/**

# Power Designer Configures Modular Power Systems




Vicor's new Power System Designer online design tool simplifies and accelerates the creation of compact, multi-output, modular power systems from the input source – either AC or DC – to system loads. Engineers simply specify their AC or DC input source and operating range, and their required output voltages and respective power (or current), regulation and isolation specifications, and the tool automatically generates and identifies the best alternative solutions, each solution characterized by figures of merit including Highest Operating Efficiency, Lowest Component Count, Lowest Cost, Smallest Footprint and Recommended Best Fit. Each solution can be viewed, analyzed and optimized using Vicor's fully editable Whiteboard tool to meet the exacting performance requirements of the target application. For any selected design, the Power System Designer tool can display a visual representation of the mechanical layout of the system and generate a complete Bill-of-Materials along with ordering and pricing information. The tool facilitates power system design by enabling specification, analysis and configuration of complete, multi-output, power systems.

**www.vicorpower.com**

# Insulated Metal Baseplate IGBT Module

Vincotech launched a new industry-standard low-profile package for mid-power inverters. Engineered mainly for industrial drives, solar power and UPS applications, the VINco E3 package features SLC (SoLid Cover) technology, which combines an insulated metal baseplate and direct potting resin to achieve both high thermal and high power cycling capability. Equipped with the latest low-loss Mitsubishi 7 gen chips, this package also achieves high power density. The new VINco E3 line's first release is the VINcoDUAL E3 half-bridge, with sixpack and PIM configurations to follow. First engineering samples may be sourced on demand.

**www.vincotech.com/products/**

## Arbitrary 4-Quadrant Power Sources

**www.rohrer-muenchen.de**
Rohrer GmbH
Tel.: +49 (0)89 8970120

## Busbars

**www.auxel.com**
Auxel FTG
Tel: + 33 3 20 62 95 20

## Capacitors

**www.psl-group.uk.com**
PSL Group UK Ltd.
Tel +44 (0) 1582 676800

## Certification

**www.productapprovals.co.uk**
Product Approvals Ltd
Tel: +44 (0)1588 620192

## Connectors & Terminal Blocks

**www.auxel.com**
Auxel FTG
Tel: +44 (0)7714 699967

## DC/DC Connverters

**www.power.ti.com**
Texas Instruments
Tel: +44 (0)1604 663399

**www.protocol-power.com**
Protocol Power Products
Tel: +44 (0)1582 477737

## Diodes


**www.neutronltd.co.uk**
Neutron Ltd
Tel: +44 (0)1460 242200

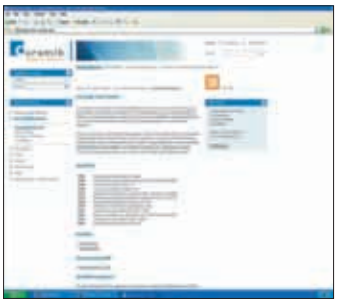
**www.microsemi.com**
Microsemi
Tel: 001 541 382 8028

**www.voltagemultipliers.com**
Voltage Multipliers, Inc.
Tel: 001 559 651 1402

## Diodes

**www.proton-electrotex.com/**
Proton-Electrotex JSC/
Tel: +7 4862 440642;

## Direct Bonded Copper (DPC Substrates)



**www.curamik.co.uk**
curamik® electronics GmbH
Tel: +49 9645 9222 0

## Discrete Semiconductors

**www.digikey.com/europe**
Digi-Key
Tel: +31 (0)53 484 9584

**www.microsemi.com**
Microsemi
Tel: 001 541 382 8028

## Drivers ICS

**www.power.ti.com**
Texas Instruments
Tel: +44 (0)1604 663399

## EMC/EMI

**www.dextermag.com**
Dexter Magnetic Technologies, Inc.
Tel: 001 847 956 1140

## Ferrites & Accessories

**www.dextermag.com**
Dexter Magnetic Technologies, Inc.
Tel: 001 847 956 1140

## GTO/Triacs

**www.mark5.com**
Mark 5 Ltd
Tel: +44 (0)2392 618616

## Hall Current Sensors


**www.dgseals.com**
dgseals.com
Tel: 001 972 931 8463

## Harmonic Filters

**www.murata-europe.com**
Murata Electronics (UK) Ltd
Tel: +44 (0)1252 811666

## High Voltage and High Power Electronics

**Dean Technology, Inc.**
www.deantechnology.com
+1 (972) 248-7691

## IGBTs

**www.microsemi.com**
Microsemi Tel: 001 541 382 8028

**www.power.ti.com**
Texas Instruments
Tel: +44 (0)1604 663399

## Line Simulation

**www.hero-power.com**
Rohrer GmbH
Tel.: +49 (0)89 8970120

## Magnetic Materials/Products

**www.dextermag.com**
Dexter Magnetic Technologies, Inc.
Tel: 001 847 956 1140

**www.rubadue.com**
Rubadue Wire Co., Inc.
Tel. 001 970-351-6100

## Mosfets

**www.mark5.com**
Mark 5 Ltd
Tel: +44 (0)2392 618616

**www.microsemi.com**
Microsemi
Tel: 001 541 382 8028

**www.neutronltd.co.uk**
Neutron Ltd
Tel: +44 (0)1460 242200

## Optoelectronic Devices

**www.digikey.com/europe**
Digi-Key Tel: +31 (0)53 484 9584

**www.power.ti.com**
Texas Instruments
Tel: +44 (0)1604 663399

## Packaging & Packaging Materials

**www.curamik.co.uk**
curamik® electronics GmbH
Tel: +49 9645 9222 0

## Power Amplifiers

**www.rohrer-muenchen.de**
Rohrer GmbH
Tel: +49 (0)89 8970120

## Power ICs

**www.digikey.com/europe**
Digi-Key Tel: +31 (0)53 484 9584

**www.power.ti.com**
Texas Instruments
Tel: +44 (0)1604 663399

## Power Modules

**www.psl-group.uk.com**
PSL Group UK Ltd.
Tel +44 (0) 1582 676800

**www.fujielectric-europe.com**
Fuji Electric Europe GmbH
Tel: +49 (0)69-66902920

**www.microsemi.com**
Microsemi Tel: 001 541 382 8028

**www.proton-electrotex.com/**
Proton-Electrotex JSC/
Tel: +7 4862 440642;

## Power Protection Products

**www.power.ti.com**
Texas Instruments
Tel: +44 (0)1604 663399

## Power Semiconductors

**www.psl-group.uk.com**
PSL Group UK Ltd.
Tel +44 (0) 1582 676800

**www.proton-electrotex.com/**
Proton-Electrotex JSC/
Tel: +7 4862 440642;

## Power Substrates

**www.universal-science.com**
Universal Science Ltd
Tel: +44 (0)1908 222211

## Resistors & Potentiometers

**www.isabellenhuette.de**
Isabellenhütte Heusler GmbH KG
Tel: +49/(27 71) 9 34 2 82

## RF & Microwave Test Equipment.

**www.ar-europe.ie**
AR Europe
Tel: 353-61-504300

## Simulation Software

**www.power.ti.com**
Texas Instruments
Tel: +44 (0)1604 663399

**www.universal-science.com**
Universal Science Ltd
Tel: +44 (0)1908 222211

## Smartpower Devices

**www.irf.com**
International Rectifier Co. (GB) Ltd
Tel: +44 (0)1737 227200

## Switched Mode Power Supplies

**www.biaspower.com**
Bias Power, LLC
Tel: 001 847 215 2427

## Switched Mode Power Supplies

**www.power.ti.com**
Texas Instrumments
Tel: +44 (0)1604 663399

## Thermal Management & Heatsinks

**www.universal-science.com**
Universal Science Ltd
Tel: +44 (0)1908 222211

## Thermal Management & Heatsinks

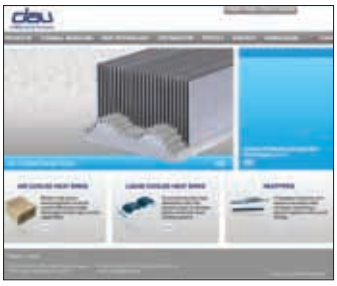
**www.psl-group.uk.com**
PSL Group UK Ltd.
Tel +44 (0) 1582 676800

## Thermal Management & Heatsinks

**www.abl-heatsinks.co.uk**
ABL Components Ltd
Tel: +44 (0) 121 789 8686

**www.curamik.co.uk**
curamik® electronics GmbH
Tel: +49 9645 9222 0

**www.dau-at.com**
Dau GmbH & Co KG
Tel: +43 3143 23510



**www.power.ti.com**
Texas Instrumments
Tel: +44 (0)1604 663399

## Thyristors

**www.mark5.com**
Mark 5 Ltd
Tel: +44 (0)2392 618616

**www.proton-electrotex.com/**
Proton-Electrotex JSC/
Tel: +7 4862 440642;

## ADVERTISERS INDEX

LpS 2016

LED professional SYMPOSIUM +EXPO

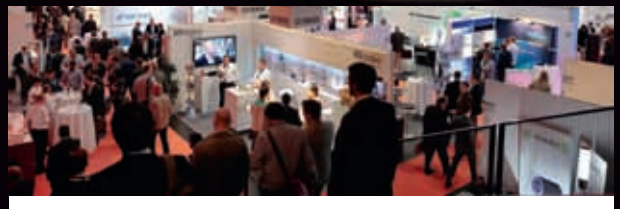
**EARLY BIRD TICKETS**
Available until July 1st.

# 6TH LED professional Symposium +Expo

## Smart Technologies for Lighting Innovations

### International Conference on Lighting Trends & Technologies

- Latest insights from research and industry leaders
- Nobel Prize Laureate Prof. Shuji Nakamura
- 80+ lectures in 4 conference tracks
- 1500+ professionals from more than 40 countries



### International Exhibition for Lighting Technologies & Applications

- State-of-the art showcases for R&D and design engineers
- Cutting-edge products, equipment and services
- Highly-focused B2B sourcing and collaboration platform
- 100+ international exhibitors including the top leaders

### Lectures from Renowned Organizations

- EU Commission, LightingEurope, Zhaga, EPIC, IBM, NXP
- Infineon, Silvair, WadeLux, Bartenbach, GE, Zumtobel
- UniBright, Glamox, Nichia, Lumileds, Cree, Osram
- Fraunhofer, Yole, Holst Center, Joanneum, CSEM

### Interactive Workshops & Forums

- Tunable Lighting Workshop by HI-LED
- Design-meets-Technology Forum by APIL
- Horticultural Lighting Workshop by EPIC
- Int'l lighting and photonics cluster forums

### Innovation Platforms

- Technical innovations presented by start-up innovators
- Light-Art-Designs by lighting designers and students
- Product launches presented by industry leaders

### Social Networking Opportunities

- Opening ceremony and expo reception
- Get-Together boat cruise on Lake Constance
- Int'l press conference with more than 25 media partners

Organized by Luger Research e.U. - Institute for Innovation & Technology

## Sept 20th - 22nd 2016 | Bregenz | Austria

**www.lps2016.com**

TRIDONIC enlightening your ideas

auer LIGHTING

SEMIKRON
innovation+service

## Power Electronic Stacks

# When Time to Market Counts


**You want to...**

- **reduce time to market**
- **limit your financial investment**
- **control your cost of development**
- **save costs on manufacturing of stack assemblies**

We are the global market leader in power electronic stacks with over 200,000 assemblies in the field. Five global stack centers provide optimized, pre-qualified and field-tested stack assemblies. Our stacks feature short lead times while still easy to customize for your needs. Our global stack centers provide worldwide coordination, engineering, manufacturing and test to localize manufacturing of your stack assemblies.

**Further information: www.semikron.com/power-stacks**