Key Parameters

Rated Output Current (1 MHz) (1)	12.5 A
Operating PWM Frequency Range (2)	3 MHz
Operating Input Voltage Range	60 V
Bias Supply Voltage	12 V

Output Current and PWM Frequency Ratings are functions of Operating Conditions. See Notes 1 & 2.

Features

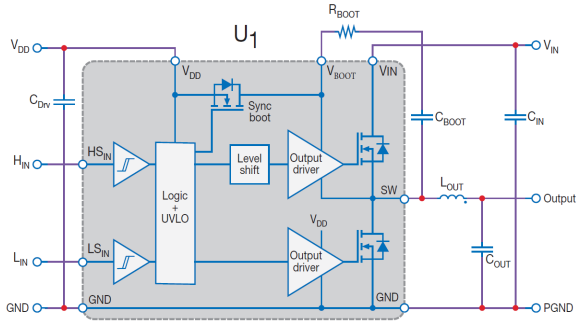
- Separate and independent high side and low side control inputs
- Input signal compatible with 3.3 V CMOS logic or 15 V analog controller
- 20 ns minimum input pulse width
- 20 ns delay time input to output
- 1 ns switching time at output node
- Robust level shifter operating from negative transient conditions
- False trigger immunity greater than 100 V/ns at output node
- Synchronous charging for high side bootstrap supply
- Regulated gate drive buffer output to drive output FETs at safe operating level
- Undervoltage lockout for high side and low side power supplies
- LGA Chip Scale Package

Applications

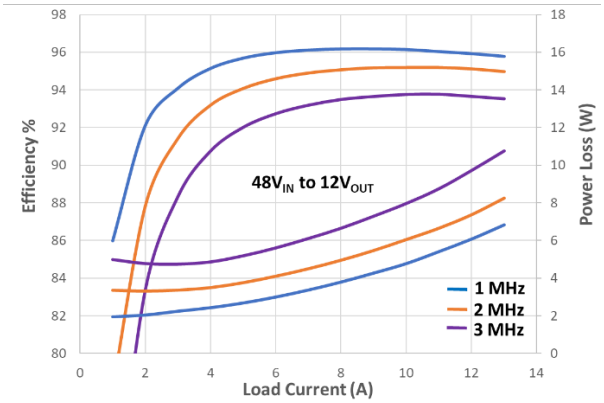
- Buck and Boost Converters
- Half-Bridge, Full Bridge or LLC Isolated Converters
- Class D Switching Audio Amplifier
- Single Phase and Three Phase Motor Drive Inverter

Typical Application

Synchronous Buck Converter

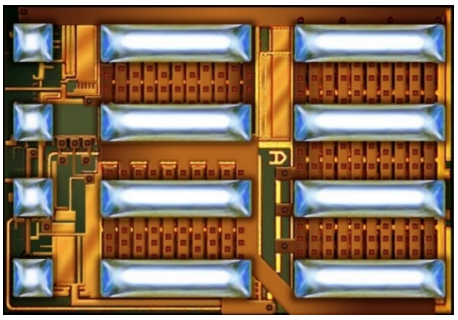


Performance Curves



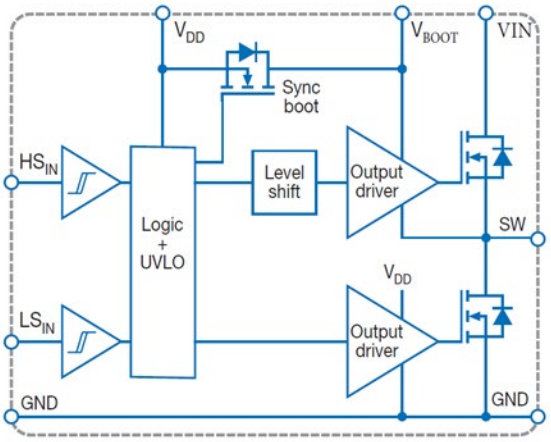
Buck Converter Topology, V_{IN}=48V, V_{OUT}=12V, Deadtime=10ns, L=2.2uH, DCR=3mΩ, R_{BOOT}=2.2Ω, EPC90120 PCB, Airflow=800 LFM.

Die Photo



3.85 mm x 2.59 mm x 0.63 mm

Functional Block Diagram



General Description

The EPC2152 is a single chip driver plus eGaN® FET half-bridge power stage. Integration is implemented using EPC's proprietary GaN IC technology. Input logic interface, level shifting, bootstrap charging and gate drive buffer circuits along with eGaN output FETs configured as a half-bridge are integrated within a monolithic chip. This results in a chip-scale LGA form factor device that measures only 3.85 mm x 2.59 mm x 0.63 mm.

The two eGaN output FETs in half-bridge topology are designed to have same $R_{DS(on)}$. Integration of eGaN FETs with on-chip gate drive buffers practically eliminate effects of common source inductance and gate drive loop inductance. Monolithic integration combined with a pinout that uses low inductance LGA solder bumps, result in a high-current output node that can switch within 1 ns under full load with PWM frequency up to 3 MHz.

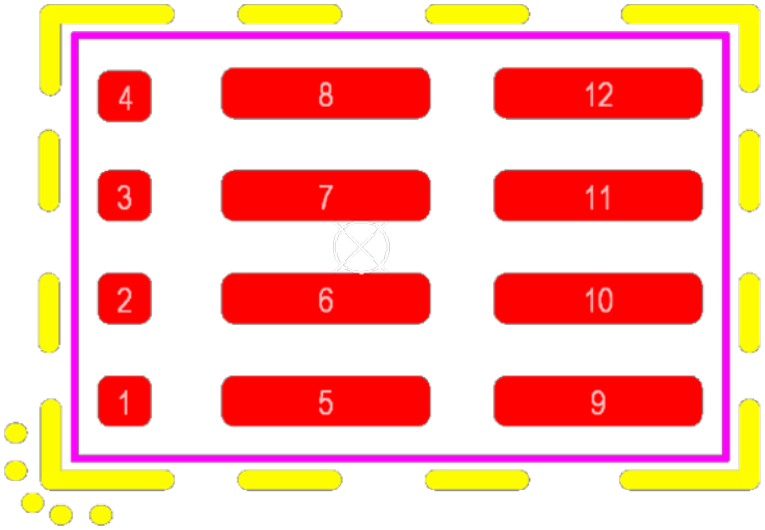
The charging path for the floating bootstrap supply is integrated using GaN FET driven by a synchronous circuit. This eliminates the need for an external bootstrap diode with associated reverse recovery charge that may result in significant power loss at high frequency switching. This synchronous bootstrap charging circuit also minimizes the voltage drop in the bootstrap charging path to ensure adequate voltage for the bootstrap power supply.

Robust level shifters from low side to high side channels are designed to operate correctly even at large negative clamped voltage and to avoid false trigger from fast dV/dt transients exceeding 100 V/ns.

Internal regulation of the gate drive voltage based on feedback from the driven output FETs ensures a safe gate voltage level while still turning on the output FETs to a low $R_{DS(on)}$ state. Additional protection is provided by separate high side and low side under-voltage lockout (UVLO) circuits with lockout levels referenced to the gate drive buffer circuit to avoid operating the output FETs in a high $R_{DS(on)}$ state.

The EPC2152 device is capable of interfacing to digital controllers that use standard 3.3 V CMOS logic levels or to analog controllers that use voltage levels of up to 15 V. Separate and independent high side and low side logic control inputs allow external controllers to set deadtimes for optimal operating efficiency.

Pinout Description



Pin#	Pin Name	Pin Type	Description
1	V_{BOOT}	S	Floating bootstrap power supply referenced to SW, connect external bypass capacitor from V_{BOOT} to SW
2	V_{DD}	S	Operating power supply referenced to GND, connect external bypass capacitor from V_{DD} to GND
3	HS_{in}	S	High side PWM logic input, level referenced to GND
4	LS_{in}	S	Low side PWM logic input, level referenced to GND
5, 9	VIN	P	Input bus voltage. Connected to high side eGaN FET drain terminal.
6, 7, 10, 11	SW	P	Output switching node. Connected to output of eGaN half-bridge power stage. The floating bootstrap power supply, V_{BOOT}, is also referenced to SW.
8, 12	GND	P	Power ground. Connected to low side eGan FET source terminal. The operating power supply, V_{DD}, is also referenced to GND.

Pin Type : P=Power, S=Signal and Supply

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise. All ratings at T_A = 25˚C.

Symbol	Parameter	Min	Max	Units
V_{IN}	Input Voltage (VIN to GND)	0	80	V
V_{SW}	Output Switching Node (SW to GND)	$-V_{SD}$ (3)	80	V
V_{DD}	Low Side Supply Voltage (V_{DD} to GND)	-0.3	15	V
V_{BOOT} - V_{SW}	High Side Supply Voltage (V_{BOOT} to SW)	-0.3	15	V
HS_{in}	High Side Logic Input (HS_{in} to GND)	-0.3	15	V
LS_{in}	Low Side Logic Input (LS_{in} to GND)	-0.3	15	V
T_J	Junction Temperature	-40	150	C
T_{STG}	Storage Temperature	-40	150	C

ESD Ratings

Symbol	Parameter	Min	Max	Units
HBM	Human-body model (JEDEC JS-001)	+/-1000		V
CDM	Charged-device model (JEDEC JESD22-C101)	+/-500		V

Thermal Characteristics

$R_{\theta JA}$ is determined with the device mounted on 1 in^2 of copper pad, single layer 2 oz copper on FR4 board.

Symbol	Parameter	Typ	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.55	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	4.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	48	°C/W

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise. All ratings at T_A = 25˚C.

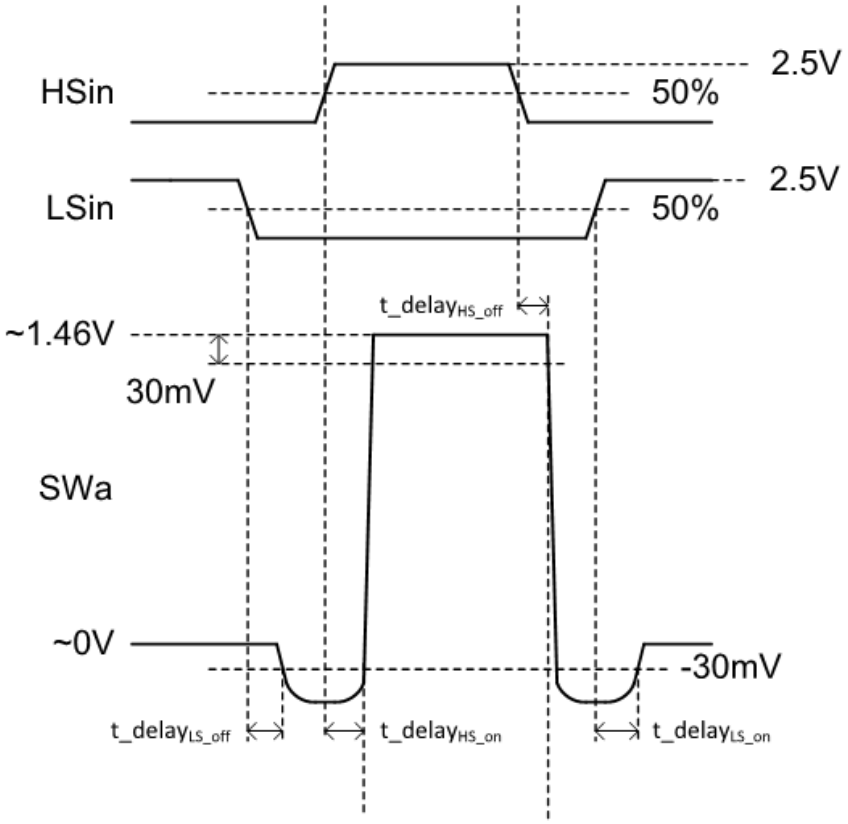
Symbol	Parameter	Min	Typ	Max	Units
V_{IN}	Input Voltage (VIN to GND)	0		60	V
V_{SW}	Output Switching Node (SW to GND)	$-V_{SD}$ (3)		60	V
V_{DD}	Low Side Supply Voltage (V_{DD} to GND)	11	12	13	V
V_{BOOT} - V_{SW}	High Side Supply Voltage (V_{BOOT} to V_{SW})	11	12	13	V
HS_{in}	High Side Logic Input (HS_{in} to GND)	0		15 (4)	V
LS_{in}	Low Side Logic Input (LS_{in} to GND)	0		15 (4)	V

Electrical Characteristics

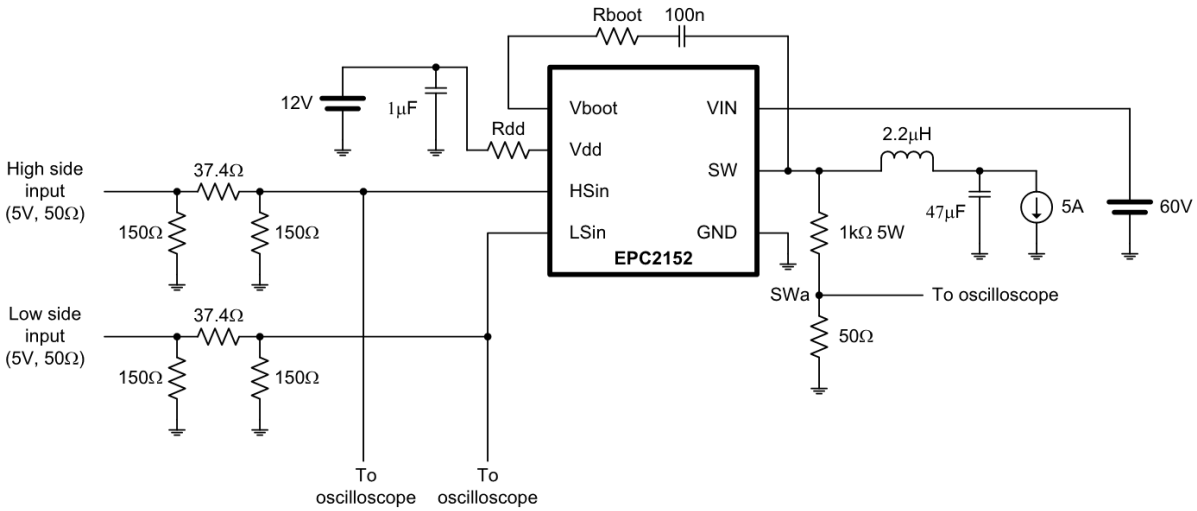
All ratings at T_A = 25˚C. Nominal V_{IN} = 48 V, V_{DD} = 12 V, (V_{BOOT} – V_{SW}) = 12 V unless indicated otherwise.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Operating Power Supply						
I_{DDQ}	Off State Total Quiescent Current	HS_{in} & LS_{in} = OFF, V_{DD}=12V		22		mA
I_{DD_1MHz}	Total Operating Current @1MHz	PWM=1MHz, 50% On-Time		29		mA
I_{DD_3MHz}	Total Operating Current @3MHz	PWM=3MHz, 50% On-Time		42		mA
Bootstrap Power Supply						
I_{BOOTQ}	Off State Bootstrap Supply Current	HS_{in} = OFF, (V_{BOOT} – V_{SW}) = 12V		8		mA
I_{BOOT_1MHz}	Bootstrap Supply Current @1MHz	HS PWM=1MHz, 50% On-Time		13		mA
I_{BOOT_3MHz}	Bootstrap Supply Current @3MHz	HS PWM=3MHz, 50% On-Time		20		mA
V_{SYNC_BOOT}	Sync Boot Generated (V_{BOOT} -V_{SW})	PWM=1MHz 25%, C_{BOOT}=0.1uF		11.7		V
Undervoltage Lockout						
$V_{DD\ (UVLO+)}$	UVLO Trip Level V_{DD} Rising	LS_{in} = ON, V_{DD} Ramps Up		7.25		V
$V_{DD\ (UVLO-)}$	UVLO Trip Level V_{DD} Falling	LS_{in} = ON, V_{DD} Ramps Down		6.50		V
$V_{BOOT\ (UVLO+)}$	UVLO Trip Level (V_{BOOT} -V_{SW}) Rising	HS_{in} = ON, V_{BOOT} Ramps Up		7.25		V
$V_{BOOT\ (UVLO-)}$	UVLO Trip Level (V_{BOOT} -V_{SW}) Falling	HS_{in} = ON, V_{BOOT} Ramps Down		6.50		V
Logic Input Pins						
V_{IH}	High-level Logic Threshold	HS_{in}, LS_{in} Rising	2.4			V
V_{IL}	Low-level Logic Threshold	HS_{in}, LS_{in} Falling			0.8	V
V_{IHyst}	Logic Threshold Hysteresis	V_{IH} Rising – V_{IL} Falling		500		mV
R_{in}	Input Pulldown Resistance	HS_{in}, LS_{in} = Open or High Z		5		kΩ
Output Power FETs						
$R_{DS(on)\_HS}$	High Side FET $R_{DS(on)}$	I_{DS} = +/-10A, HS_{in}=ON, LS_{in}=OFF		10		mΩ
$V_{HS\_DS\_Clamp}$	High Side 3rd Quadrant Clamp	I_{DS} = -10A, HS_{in} & LS_{in} = OFF		-2		V
$R_{DS(on)\_LS}$	Low Side FET $R_{DS(on)}$	I_{DS} = +/-10A, LS_{in}=ON, HS_{in}=OFF		10		mΩ
$V_{LS\_DS\_Clamp}$	Low Side 3rd Quadrant Clamp	I_{DS} = -10A, HS_{in} & LS_{in} = OFF		-2		V
I_{LEAK_VIN-SW}	Leakage Current VIN to SW	HS_{in} = OFF, VIN = 80V, SW = 0V			100	uA
I_{LEAK_SW-GND}	Leakage Current SW to GND	LS_{in} = OFF, SW = 80V			100	uA
Dynamic Characteristics (Logic Input to Output Switching Node) (see Timing Diagram and Test Circuit for Definition)						
$t\_delay_{HS\_on}$	High-Side On Propagation Delay	SW = 0V and HS FET Turn-On		20		ns
$t\_delay_{LS\_on}$	Low-Side On Propagation Delay	SW = 60V and LS FET Turn-On		20		ns
$t\_delay_{HS\_off}$	High-Side Off Propagation Delay	SW = 60V and HS FET Turn-Off		20		ns
$t\_delay_{LS\_off}$	Low-Side Off Proprgation Delay	SW = 0V and LS FET Turn-Off		20		ns
t_match_{on}	Delay Matching LS_{off} to HS_{on}	LS Turn-Off to HS Turn-On		0		ns
t_match_{Off}	Delay Matching HS_{off} to LS_{on}	HS Turn-Off to LS Turn-On		0		ns
PW_min	Minimum Input Pulse-Width	50% to 50% Width		20		ns

Timing Diagram



Test Circuit for Dynamic Characteristics



Truth Table

V_{DD}	V_{BOOT}-V_{SW}	HSin	LSin	HS FET	LS FET
<UVLO	-	-	-	OFF	OFF
>UVLO	<UVLO	-	0	OFF	OFF
>UVLO	<UVLO	-	1	OFF	ON (5)
>UVLO		0	0	OFF	OFF
		0	1	OFF	ON
		1	0	ON	OFF
		1	1	BOTH ON (6)	

Notes

Note 1: Output current rating is measured with Vin = 48V, Vout = 12V, PWM frequency = 1MHz, PCB mounted using EPC90120 Eval Board, 800 LFM airflow, operating at ambient temperature of 25C with temperature measured on top of the die, with emissivity adjusted to 0.95, not to exceed 125C at thermal equilibrium. Actual maximum output current depends on power dissipation, maximum allowed junction temperature, thermal management method and the operating environment.

Note 2: Operating PWM switching frequency range is a function of power dissipation, maximum allowed junction temperature and minimum duty cycle. Running at higher PWM switching frequency lowers the maximum output current rating.

Note 3: The output switching node (SW) is clamped by the LS FET negative source drain voltage in the 3rd quadrant with both HS and LS FETs in the off states during the deadtime period.

Note 4: For logic input voltage above 5V, a 5KΩ resistor in series should be inserted to limit the input current into the logic input pins HS_{in} and LS_{in}.

Note 5: LS_{in} commands LS FET to turn-on to charge bootstrap supply through sync boot

Note 6: Internal logic follows HSin, LSin respectively and does not lock-out when both HS and LS FETs are commanded to turn on together. Users need to implement shoot through prevention logic depending on application topology. Deadtime insertion circuit must not generate overlapping pulse widths shorter than minimum pulse width specifications, that might cause both HS and LS FETs to turn-on together.

Application Information

Layout Guidelines

Monolithic integration of the half-bridge output FETs as well as their associated gate drivers significantly reduce parasitic common source inductance (CSI) and gate drive loop inductance. What remains is the high frequency power loop inductance that is controlled by the PCB layout of the DC input capacitors in relationship to the current flow direction through the pin configuration and layout geometry of the output FETs in the half-bridge power stage. Experimental data confirmed that the efficiency curves can be impacted by as much as 4% depending on the power loop inductance varying from 0.4 nH to 3 nH [Reference 1]. Another negative effect of excessive power loop inductance is the over-voltage spike at the SW node. Decreasing the high frequency loop inductance results in lower voltage overshoot, increased input voltage capability, and reduced EMI.

A recommended layout technique for the EPC2152 device is shown in Figure 1a. [Reference 2]. This PCB layout uses the concept of creating a low-profile magnetic field cancellation loop in a multilayer PCB as shown in Figure 1b. The design utilizes the first inner layer connected to the GND plane as a power loop return path. Separated only by a thin substrate, the top layer power loop and first inner layer current return path directly underneath generate opposing magnetic fields with induced currents that have opposite direction. The result is a cancellation of magnetic fields that translates into a reduction in parasitic inductance.

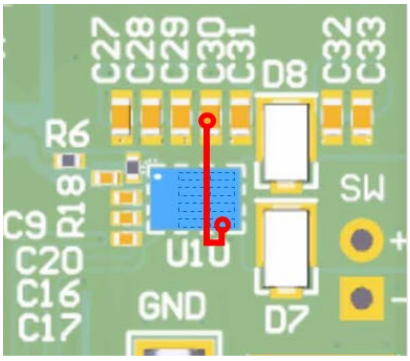


Figure 1a

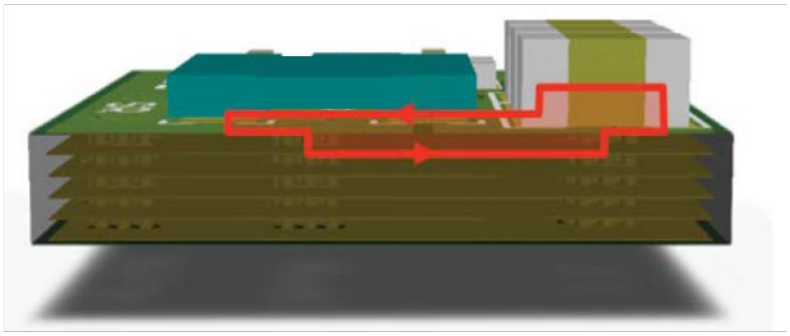


Figure 1b

Application Information

Top Side Cooling

The chip-scale packaging (CSP) of the EPC2152 device offers the possibility of six-sided cooling, with effective heat extraction from the bottom, top, and sides of the die. Designers can opt for using the device in still air or with airflow by simply using the underlying PCB for heat dissipation. By mounting the device on a multi-layer PCB with 2 oz. copper using the recommended layout guideline as demonstrated in the EPC90120 development board [Reference 2], the device can operate continuously in still air at an ambient temperature of 25C under the operating conditions of V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 10 A while switching the synchronous buck converter at 1MHz.

To extend the output current capability, the addition of a heatsink to the device can increase power throughput. Figure 2 shows a simple method to attach a heatsink to the EPC2152 CSP device. The approach makes use of low profile threaded mechanical SMD spacers [Würth Elektronik WA-SMSI SMT Steel Spacer, M2 Thread] that are simply soldered into the PCB. The spacer sets the heatsink height above the board to 1 mm and when a compliant thermal interface material is applied to the backside of the device, provides the correct compression and thermal interface impedance. The heatsink can be mechanically fastened by just inserting screws through the threads of the SMD spacers. An increase of output current capability up to +60% has been demonstrated using this method [Reference 3].

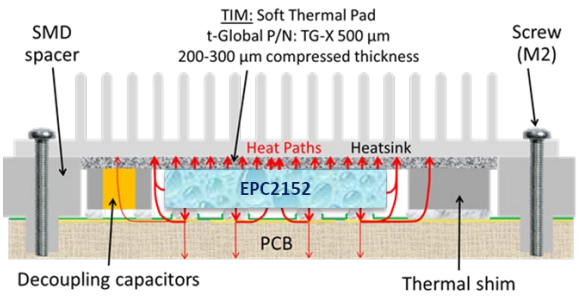


Figure 2a

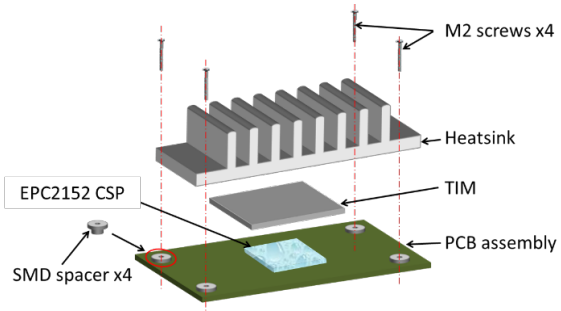


Figure 2b

Application Information

Adjusting Switching Speed

The EPC2152 device is designed to switch in less than 1 ns to minimize output FET switching losses. Using the recommended layout guidelines, shown in Figure 1 can minimize the high frequency loop inductance to less than 0.2 nH as demonstrated in EPC90120 development board [Reference 2]. However, the fast di/dt at turn-on can induce a higher than acceptable over-voltage spike at the SW node. Designers can reduce the rise time of the SW node by inserting an optional R_{BOOT} resistor in series with the bootstrap bypass capacitor C_{BOOT} as illustrated in Test Circuit for Dynamic Characteristics. This helps to reduce over-voltage spike in the positive going edge during hard switching conditions. To reduce the negative transient voltage spike below ground for negative going edge during hard switching conditions, designers can insert optional R_{DD} resistor in series with the bias supply bypass capacitor C_{DRV} also shown in the same Test Circuit. The switching waveforms using different values of R_{BOOT} on rising SW node are shown in Figure 3a under the operating conditions of V_{IN} = 48 V, V_{OUT} = 12 V and I_{OUT} = 10 A. Increasing R_{BOOT} value helps to decrease switching speed, lower over-voltage spike and reduce ringing. The power loss penalty is only 0.2% at I_{OUT} = 10 A with R_{BOOT} increasing from 0 Ω to 20 Ω as shown in Figure 3b. The associated peak over-voltage spike above V_{IN} of 48 V ranges from 35V over with R_{BOOT} = 0 Ω to only 8 V over at R_{BOOT} = 10 Ω (Figure 3a). At R_{BOOT} = 20 Ω the waveform is critically damped.

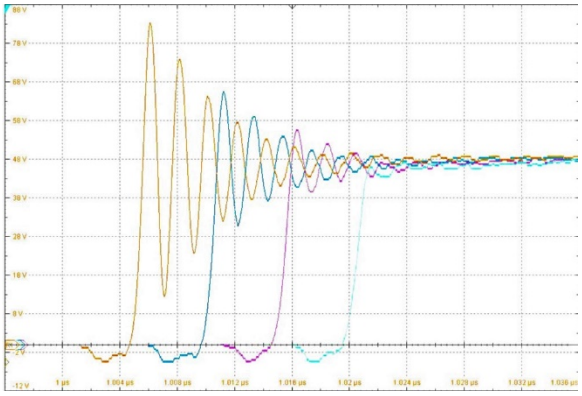


Figure 3a

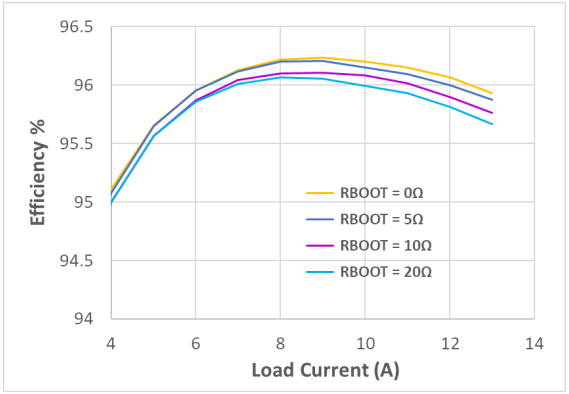


Figure 3b

Application Information

EPC90120 Development Board

A quick way to evaluate the EPC2152 device in actual application is the EPC90120 development board that measures 50mm x 50mm. The board configures the EPC2152 to operate as either buck or boost converter with all critical components in place. The layout supports optimal switching performance using the recommended layout guideline. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is shown in Figure 4a and a picture of the board is shown in Figure 4b.

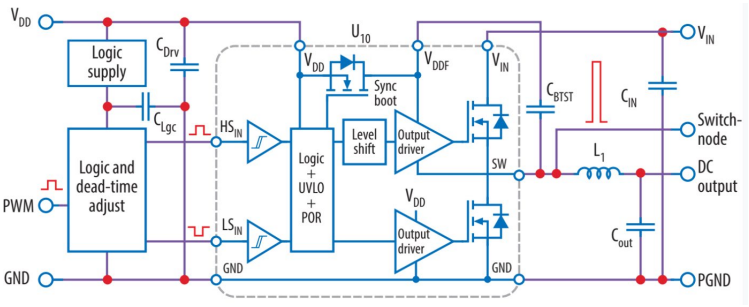


Figure 4a

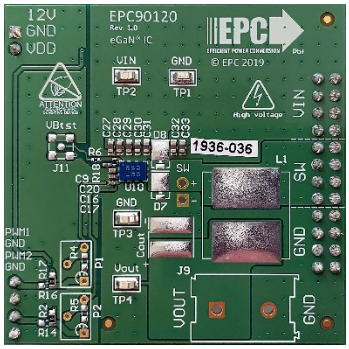


Figure 4b

References

[1] EPC White Paper WP010 - Optimizing PCB Layout. This white paper explores the optimization of PCB layout for an eGaN FET based point of load (POL) buck converter, comparing the conventional designs and proposing a new optimal layout to further reduce parasitic.

WP010 Download Link: bit.ly/EPCWP010 .

[2] EPC90120 Development Board Quick Start Guide. This QSG guide describes the EPC90120 development board in details containing the Bill of Materials (BOM), the circuit schematic as well as quick start procedure for buck and boost converter configurations. The layout uses the optimized guideline and users can download the Gerber files from EPC website.

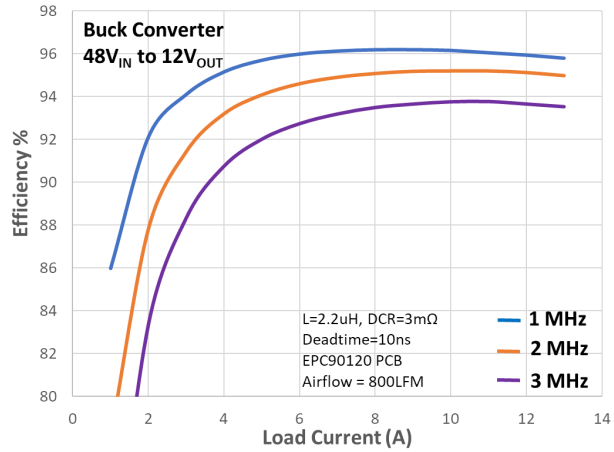
EPC90120 QSG Download Link: bit.ly/EPC90120 .

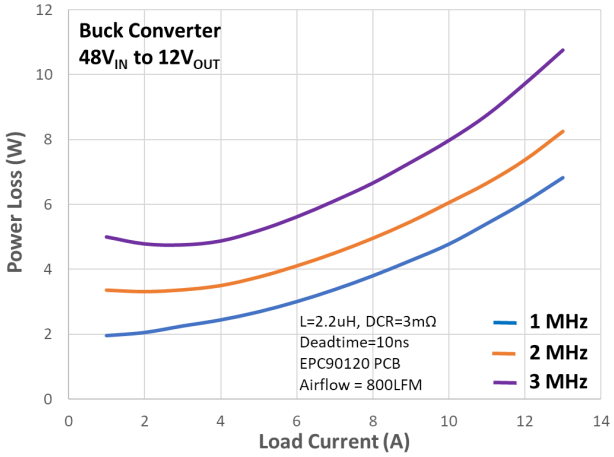
EPC90120 Gerber File Download link: bit.ly/EPC90120Gerbers .

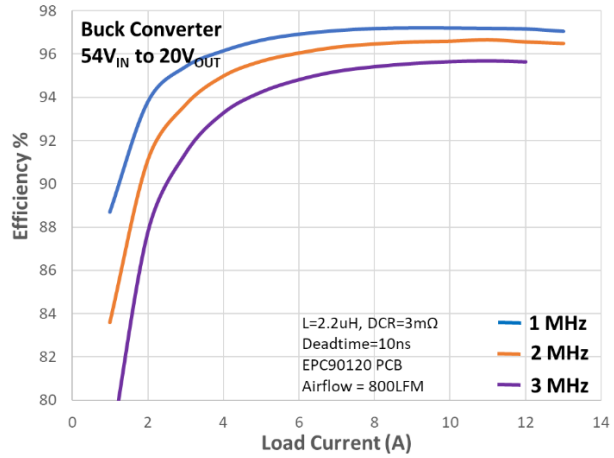
[3] EPC How2AppNote 012 - How to Get More Power Out of an eGaN Converter with a Heatsink.

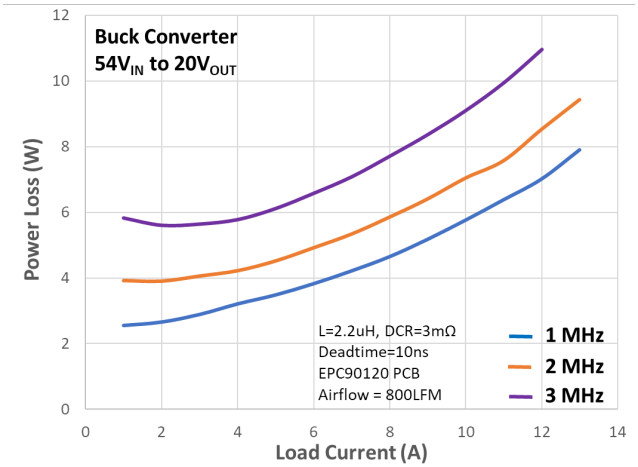
How2AppNote 012 Download link: bit.ly/EPCH2AN012

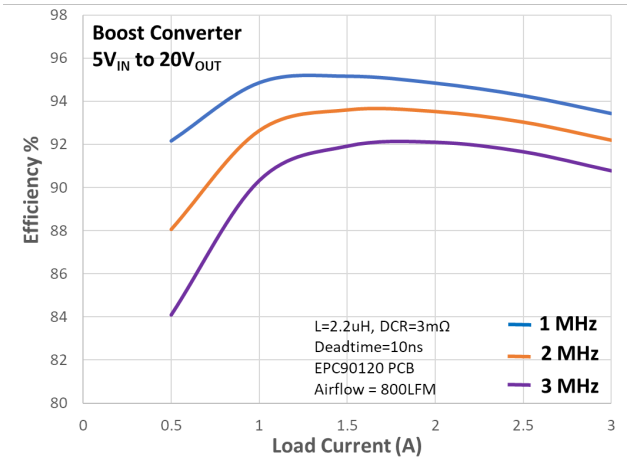
Typical Performance Characteristics

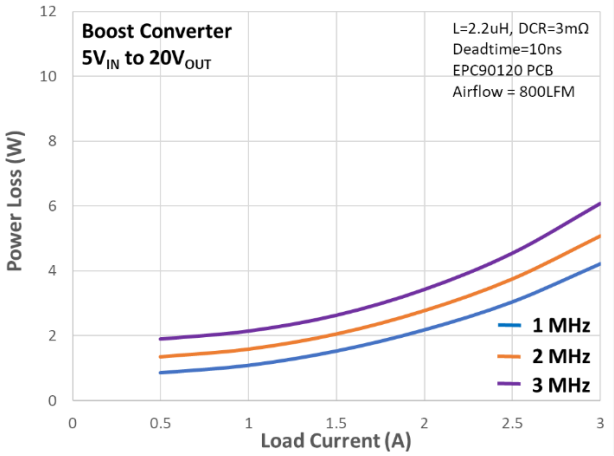






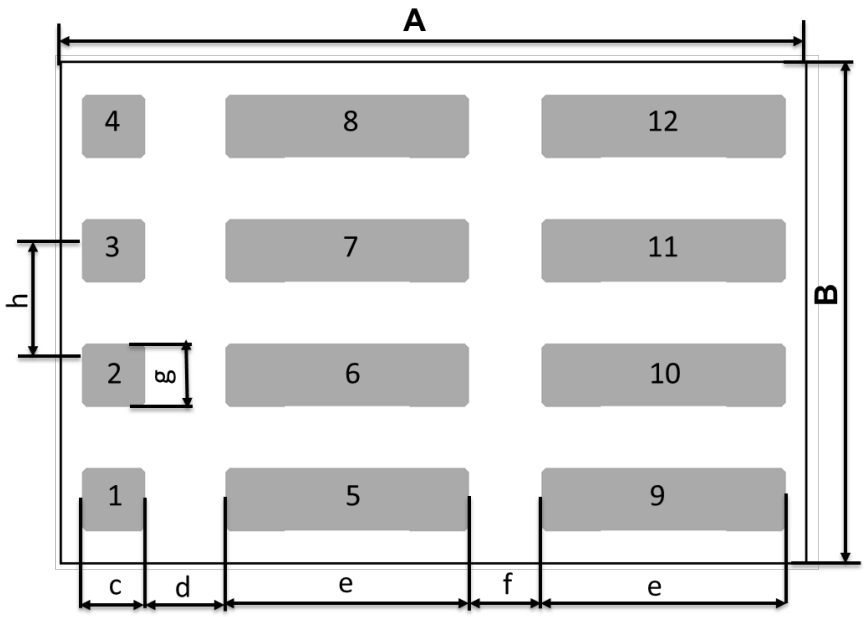






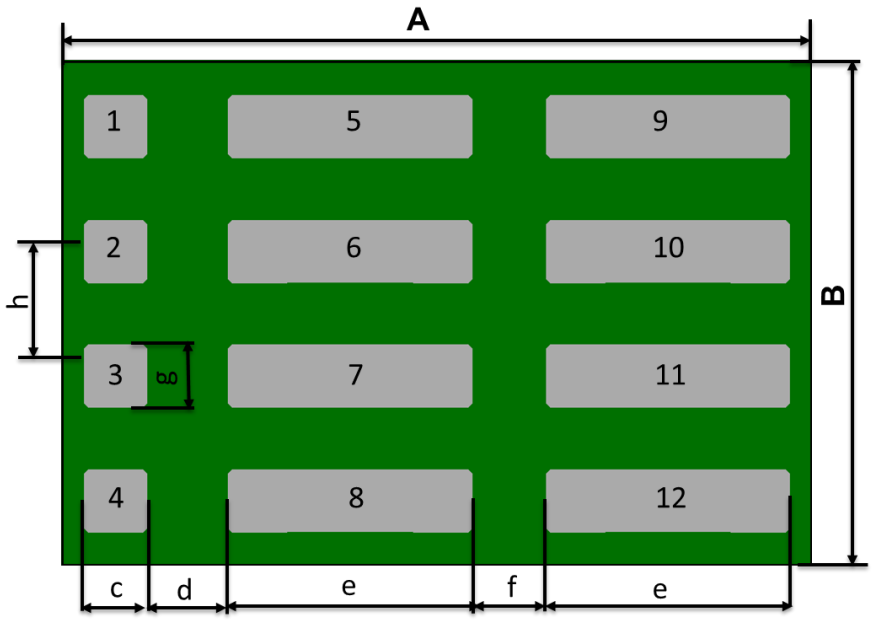
Packaging Information

DIE OUTLINE, Pad View



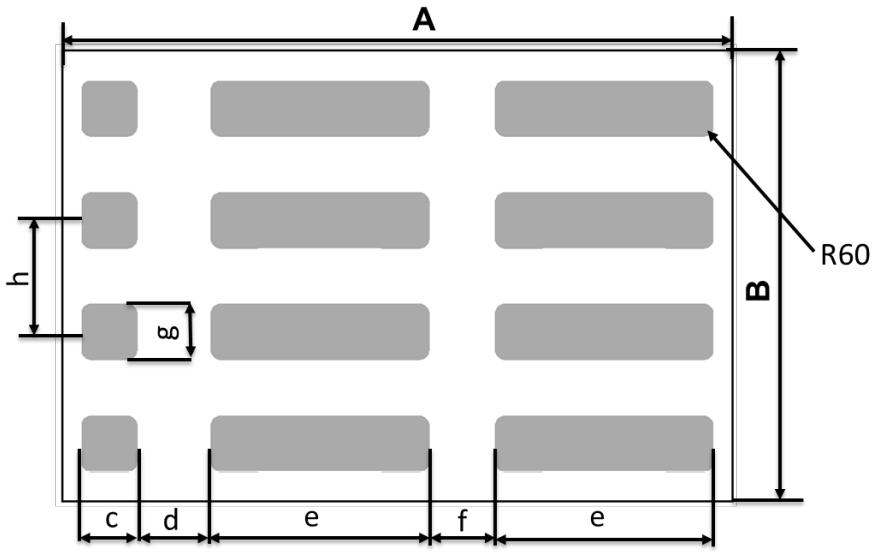
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	3820	3850	3880
B	2560	2590	2620
c		320	
d		420	
e		1250	
f		380	
g		320	
h		640	

RECOMMENDED LAND PATTERN
(measurements in µm, The land pattern is solder mask defined)



DIM	MICROMETERS
A	3850
B	2590
c	320
d	420
e	1250
f	380
g	320
h	640

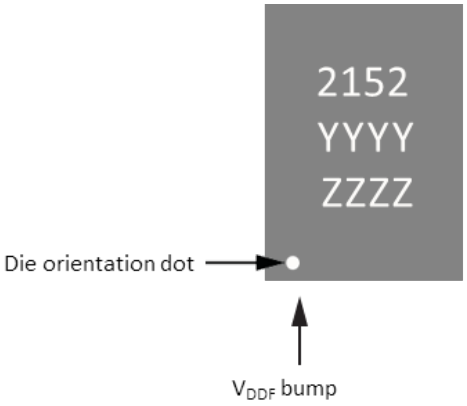
RECOMMENDED STENCIL DRAWING (measurements in µm)



DIM	MICROMETERS
A	3850
B	2590
c	320
d	420
e	1250
f	380
g	320
h	640

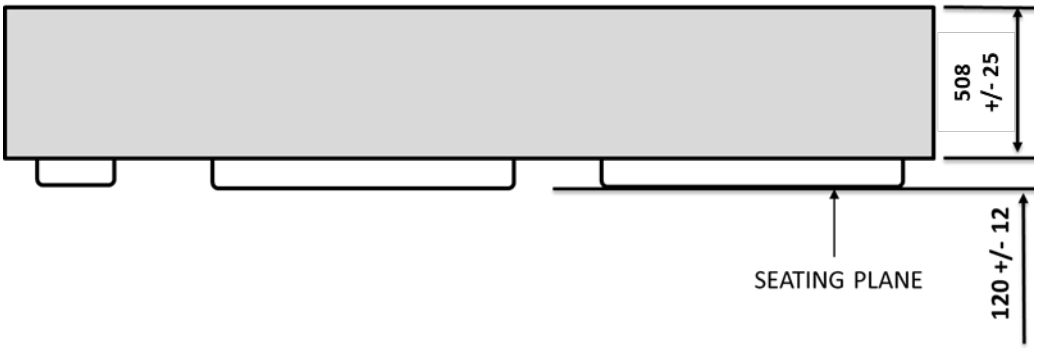
Recommended stencil should be 4mil (100 µm) thick, laser cut stainless steel, opening per drawing.
The corner has a radius of R60
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.
Additional assembly resources are available at epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

DIE MARKINGS

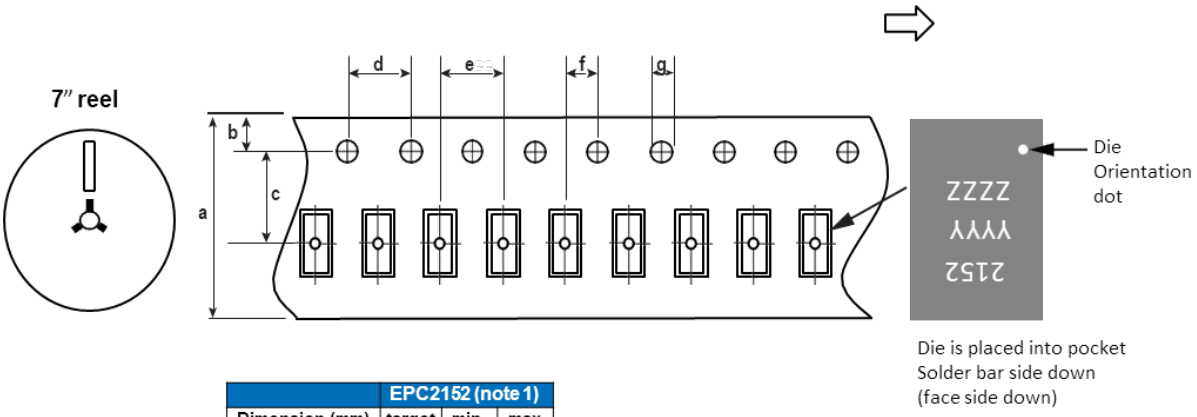


Part Number	Laser Markings		
	Part # Marking Line1	Lot_DateCode Marking Line2	Lot_DateCode Marking Line3
EPC2152	2152	YYYY	ZZZZ

SIDE VIEW, not to scale



TAPE AND REEL CONFIGURATION, 4mm pitch, 12mm wide tape on 7”reel



	EPC2152 (note 1)		
Dimension (mm)	target	min	max
a	12.00	11.70	12.30
b	1.75	1.65	1.85
c (see note)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

Revision 1.0 March 16, 2020