

EPC2619 – Enhancement Mode Power Transistor

 V_{DS} , 80 V $R_{DS(on)}$, 3.3 mΩ I_D , 29 A

PRELIMINARY



RoHS

Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:

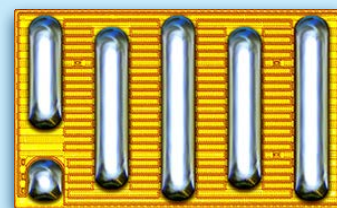
Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	96	
I_D	Continuous ($T_A = 25^\circ\text{C}$)	29	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	164	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	64	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 1 \text{ mA}$	80			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$, $V_{DS} = 64 \text{ V}$		0.01	1	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.02		
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5 \text{ V}$, $T_J = 125^\circ\text{C}$		0.05		
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.007		
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 5.5 \text{ mA}$	0.7	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 16 \text{ A}$		3.3		mΩ
V_{SD}	Source-Drain Forward Voltage [#]	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.6		V

[#] Defined by design. Not subject to production test.



Die Size: 2.5 x 1.5 mm

EPC2619 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- DC-DC Converters
- Isolated DC-DC Converters
- Sync Rectification to 12 – 20 V
- Battery Chargers, Storage, and Stabilizers
- Solar Optimizers
- Motor Drive
- Power Tools
- eBikes and eScooters
- Robots
- DC Servo
- Medical Robots and DC-DC
- Class D Audio
- USB PD 3.1 Chargers
- Point of Load Converters

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint
- Excellent Thermal

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2619>

Dynamic Characteristics[#] ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		1180		pF
C_{RSS}	Reverse Transfer Capacitance			3.0		
C_{OSS}	Output Capacitance			310		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		400		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			530		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 16\text{ A}$		8.3		nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 50\text{ V}, I_D = 16\text{ A}$		2.1		
Q_{GD}	Gate-to-Drain Charge			1.0		
$Q_{G(TH)}$	Gate Charge at Threshold			1.4		
Q_{OSS}	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		27		
Q_{RR}	Source-Drain Recovery Charge			0		

[#] Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50 V.

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50 V.

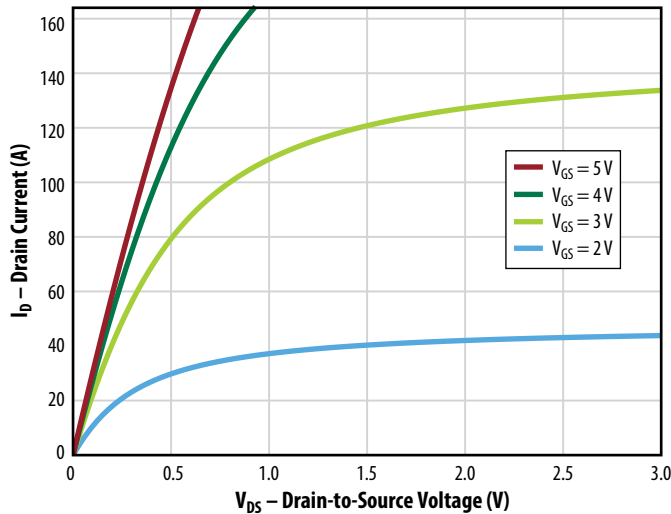
Figure 1: Typical Output Characteristics at 25°C 

Figure 2: Typical Transfer Characteristics

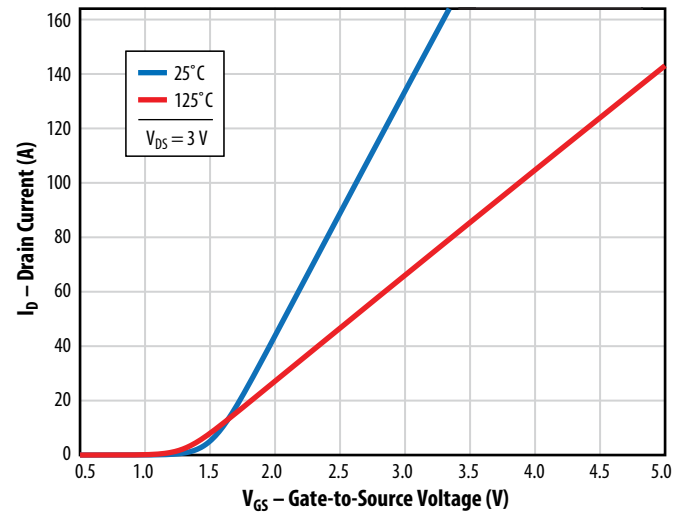
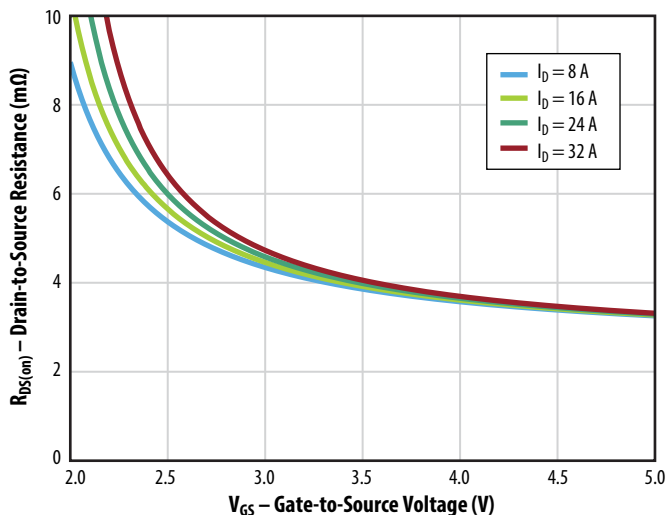
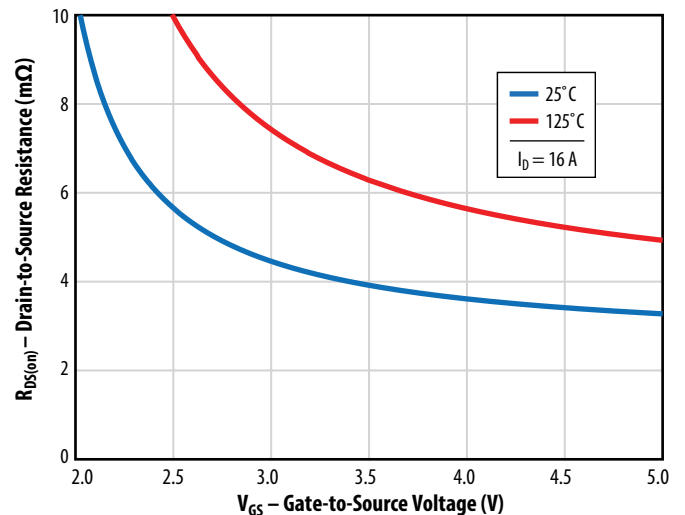
Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

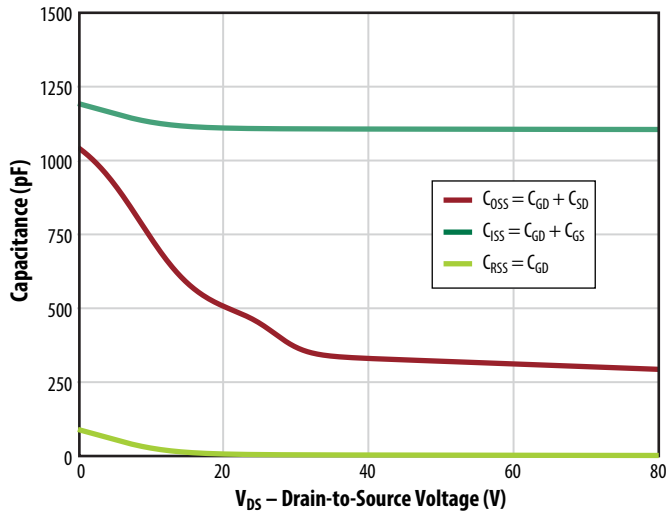


Figure 5b: Typical Capacitance (Log Scale)

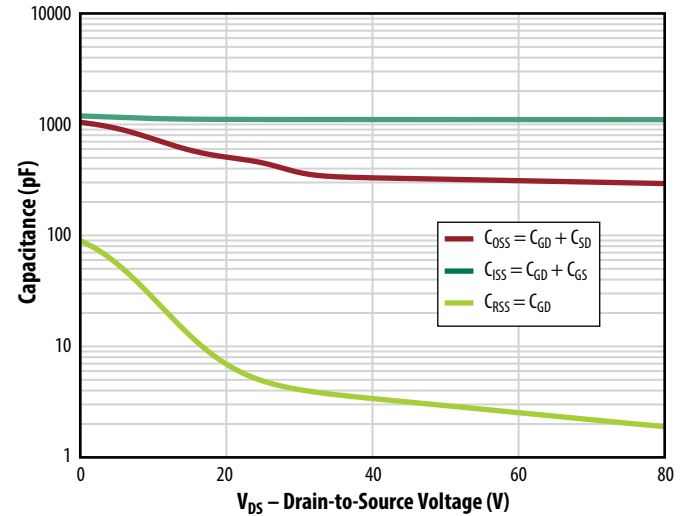
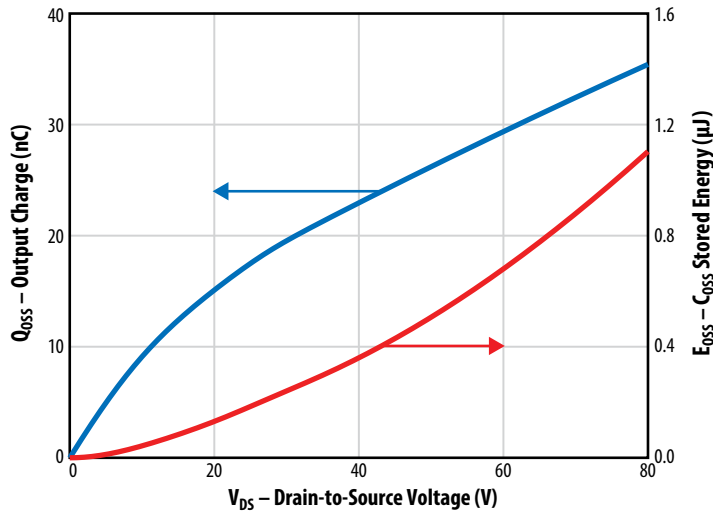
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

Figure 7: Typical Gate Charge

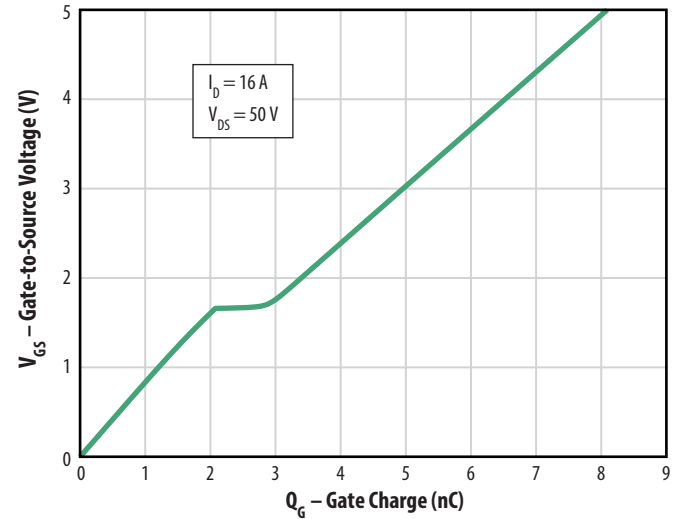
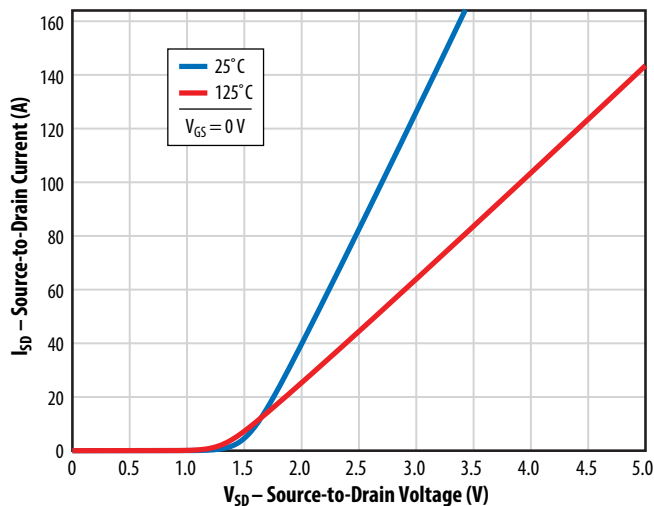


Figure 8: Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9: Normalized On-State Resistance vs. Temperature

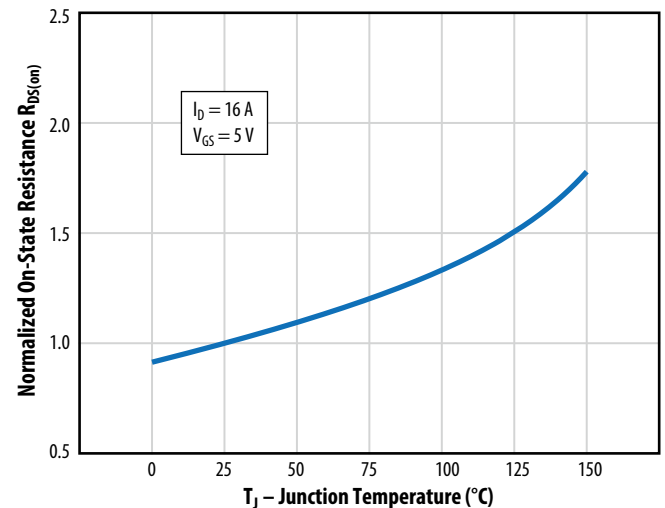


Figure 10: Normalized Threshold Voltage vs. Temperature

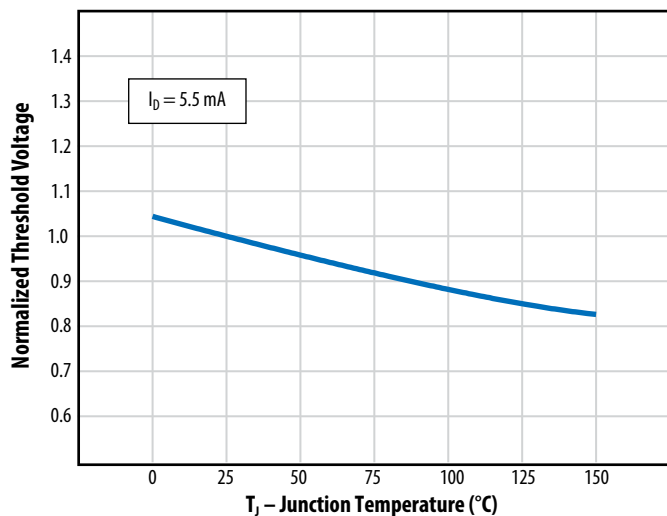


Figure 11: Safe Operating Area

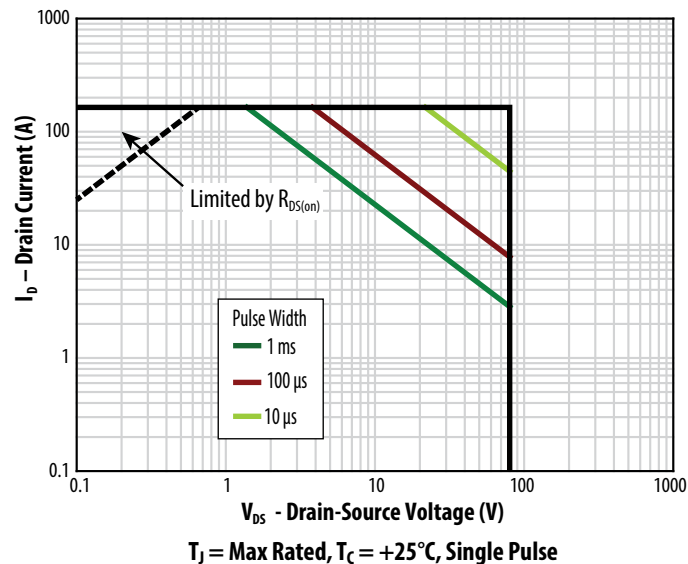
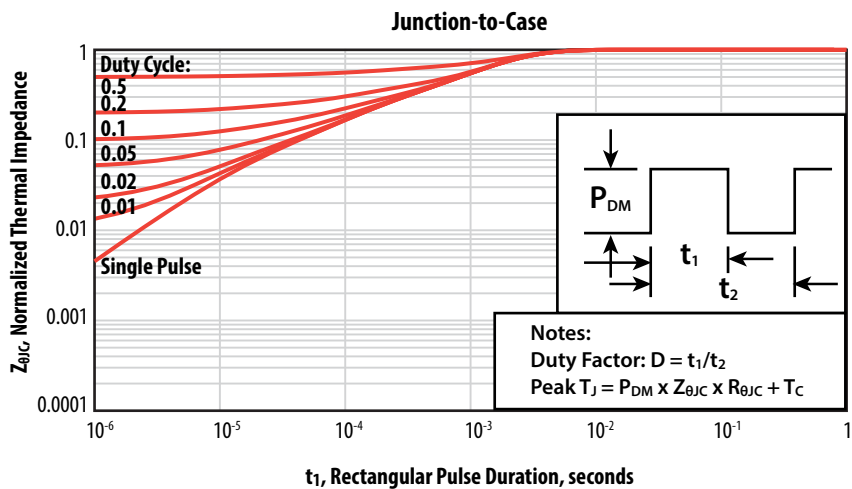
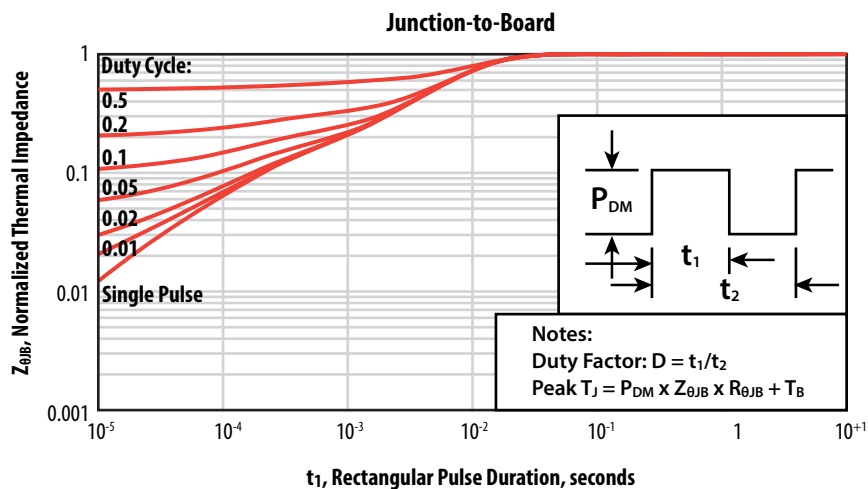
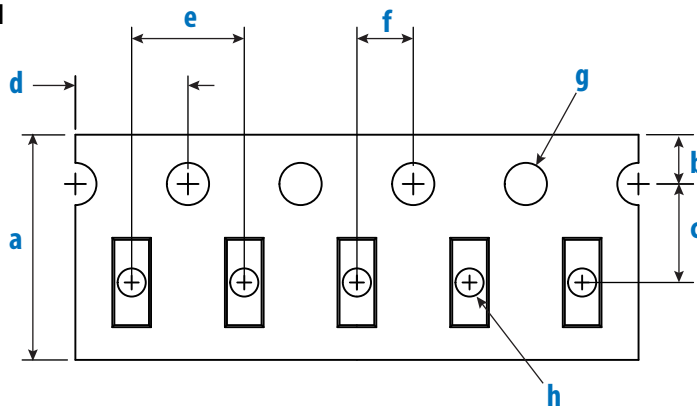
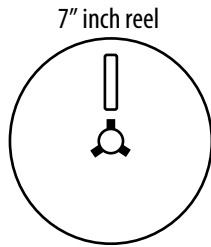


Figure 12: Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel



Loaded Tape Feed Direction →



Die orientation dot
Gate solder bar is under this corner

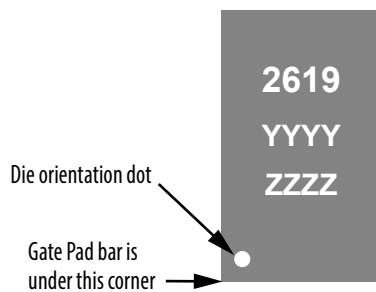
Die is placed into pocket
solder bar side down
(face side down)

EPC2619 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

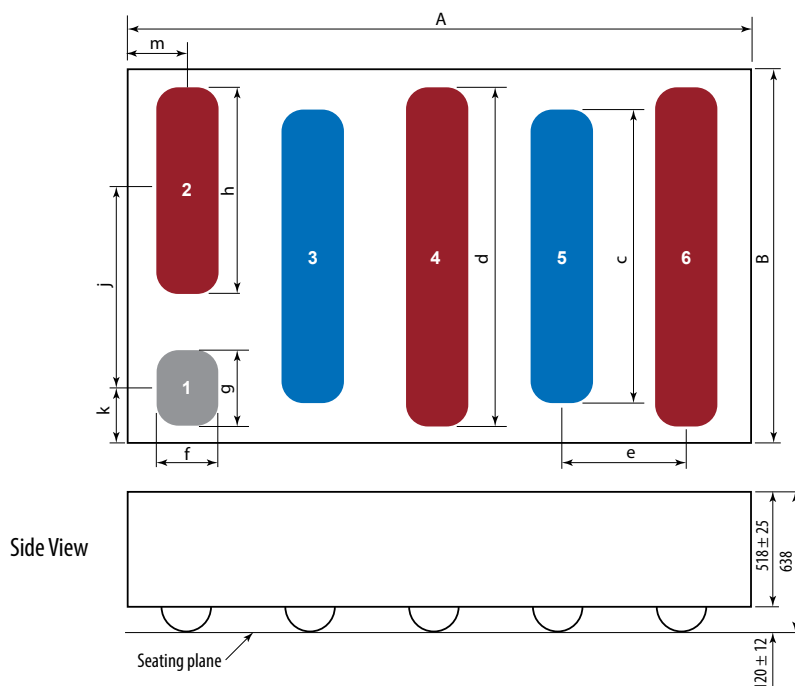
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot _Date Code Marking Line 2	Lot _Date Code Marking Line 3
EPC2619	2619	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	2470	2500	2530
B	1470	1500	1530
c		1175	
d		1350	
e		500	
f		250	
g		300	
h		825	
j		787.5	
k		225	
m		250	

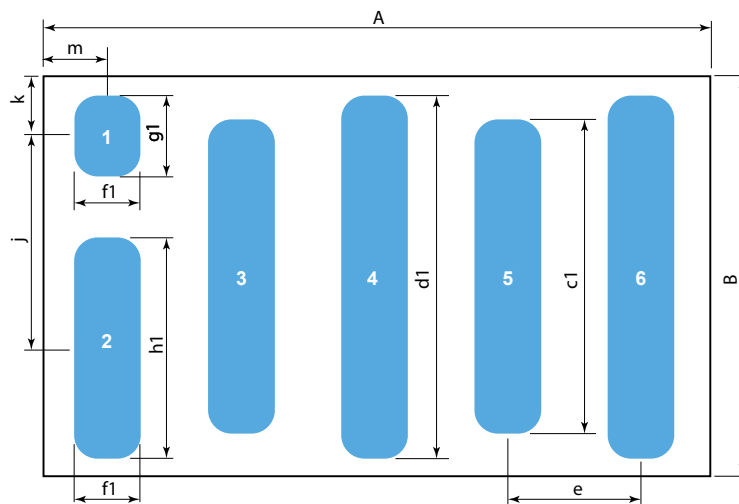
Pad 1 is Gate;

Pads 2, 4, 6 are Source;

Pads 3, 5 are Drain

RECOMMENDED LAND PATTERN

(units in μm)



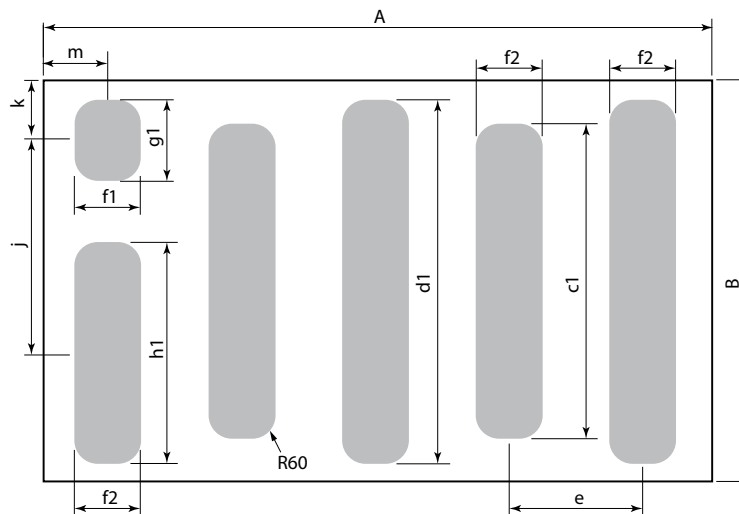
Land pattern is solder mask defined

DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
g1	280
h1	805
j	787.5
k	225
m	250

Pad 1 is Gate;
Pads 2, 4, 6 are Source;
Pads 3, 5 are Drain

RECOMMENDED STENCIL DRAWING

(units in μm)



DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
f2	210
g1	280
h1	805
j	787.5
k	225
m	250

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional Resources Available:

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>
(for preliminary device Altium footprints, contact EPC)

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EPC Patent Listing: epc-co.com/epc/AboutEPC/Patents.aspx

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change without notice.

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