ISLVERSALDEMO2Z

The ISLVERSALDEMO2Z evaluation board provides the power management for the AMD Xilinx Space Grade Versal ACAP AI Core VC1902 using Renesas' Radiation Hardened Power Management devices. The Versal ACAP system requires various supply rails, including the core, digital, analog and DDR memory. The ISLVERSALDEMO2Z provides all these rails for the user to evaluate the performance against the Versal ACAP DC and AC electrical specifications.

Features

- Radiation hardened QMLV power solution by Renesas (MIL-PRF-38538)
- Designed to power AMD Xilinx Space Grade Versal ACAP AI Core VC1902
- Includes regulators for all VC1902 rails, DDR4 Memory and general +5V/+3.3V bus
- Power Supply Sequencing up and down on all rails

Power Supply Specifications

- +12V_{DC} ±10% (Banana Jack Connectors)

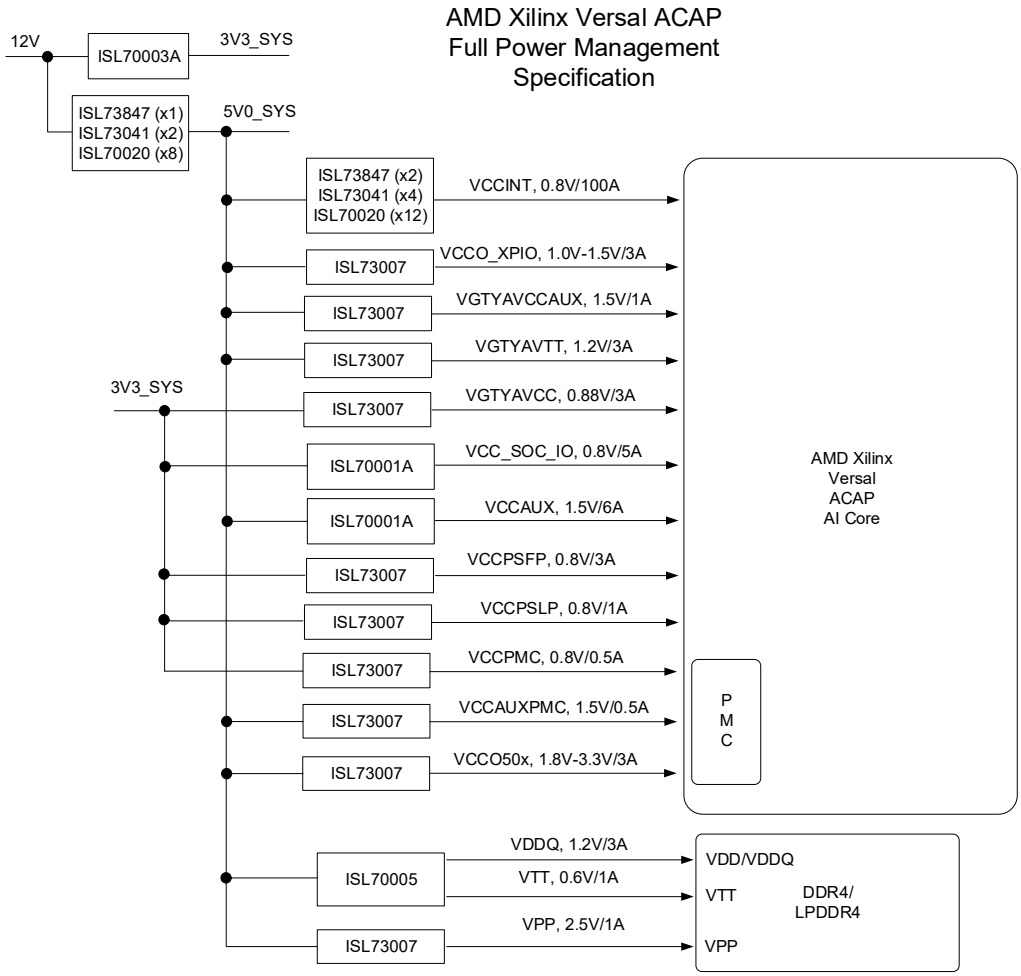

Figure 1. Power Management Block Diagram

Contents

1. Functional Description

1.1 Power Tree

The power tree diagram and AMD Xilinx Versal ACAP supply rail requirements table is shown below. The power management solution is developed for the Full Power Management application of the AMD Xilinx Versal ACAP which requires individual supplies for most of the rails and a specific power sequencing.

The ISLVERSALDEMO2Z evaluation board operates on a +12V DC power supply. Two front end DC-DC regulators provide +5.0V and +3.3V system rails that powers all the other POL DC-DC regulators.

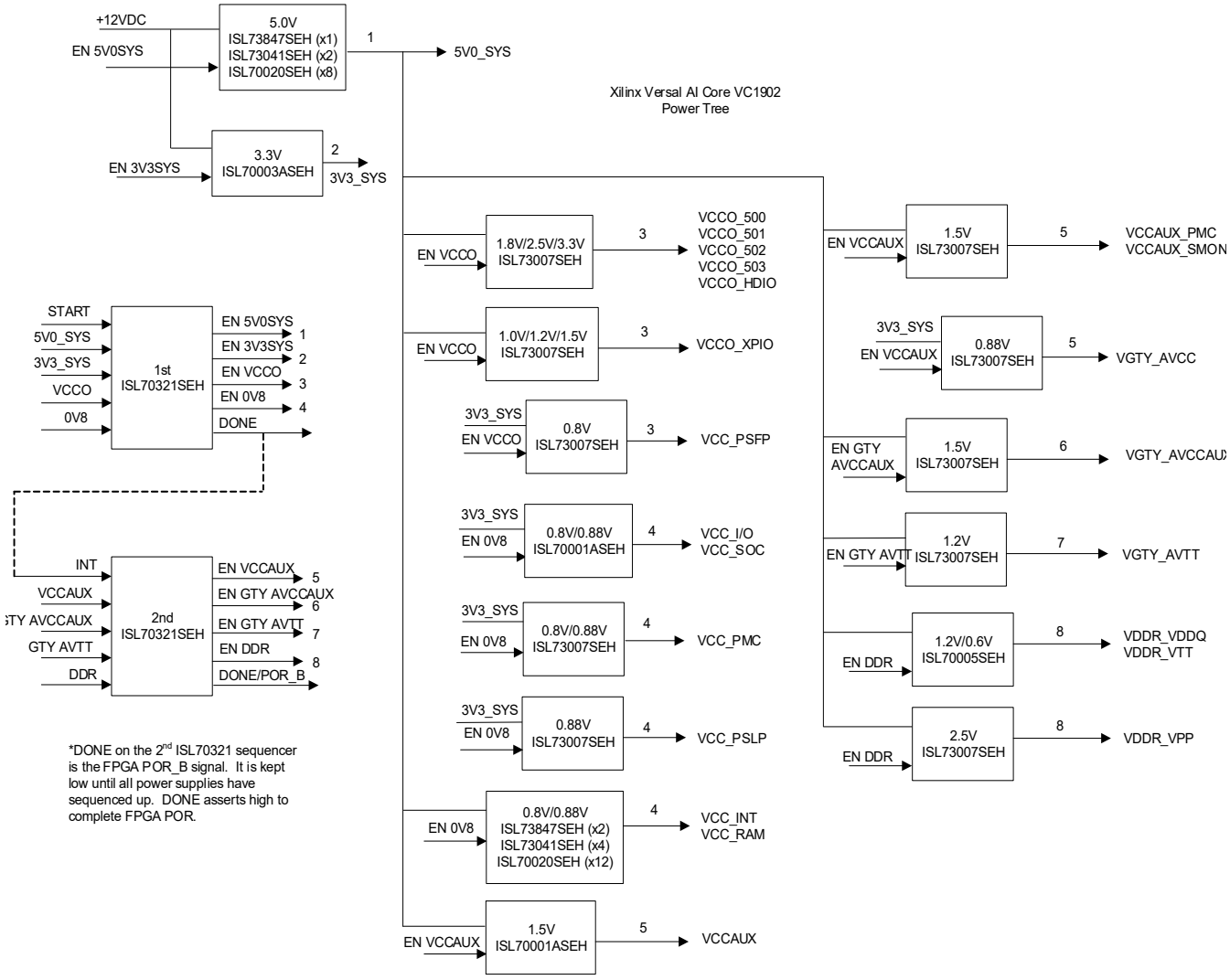

Figure 2. Renesas Radiation Hardened Power Tree for AMD Xilinx Versal ACAP

Table 1. AMD Xilinx Versal ACAP AI Core VC1902 Power Management Specifications

Power Sequencing	Rail Voltage	Rail Name	Current Demand	DC Tol	AC Tol	Renesas Solution
1	5.0V	5V0_SYS	35A	±5%		(1) ISL73847SEH + (2) ISL73041SEH + (8) ISL70020SEH
	3.3V	3V3_SYS	3A	±3%		ISL70003ASEH
2	1.8V, 2.5V or 3.3V	VCCO_500, VCCO_501, VCCO_502, VCCO_503, VCCO_HDIO	3A	±1%	+3%/-5% for 3.3V ±5% otherwise	ISL73007SEH
	1.0V to 1.5V	VCCO_XPIO	3A	±1%	±5%	ISL73007SEH
	0.8V or 0.88V	VCC_PSFP	1.5A	±1%	±17mV	ISL73007SEH
3	0.8V or 0.88V	VCC_SOC, VCC_IO	3.5A	±1%	±17mV	ISL70001ASEH
	0.8V or 0.88V	VCC_PMC	0.35A	±1%	±17mV	ISL73007SEH
	0.8V or 0.88V	VCC_PSLP	0.3A	±1%	±17mV	ISL73007SEH
	0.8V or 0.88V	VCCINT, VCC_RAM	100A	±1%	±17mV	(2) ISL73847SEH + (4) ISL73041SEH + (12) ISL70020SEH
4	1.5V	VCCAUX	4.2A	±1%	±2%	ISL70001ASEH
	1.5V	VCCAUX_SMON, VCCAUX_PMC	0.35A	±1%	±2%	ISL73007SEH
	0.88V	VGTY_AVCC	1.7A	±2%	10mVpp	ISL73007SEH
5	1.5V	VGTY_AVCCAUX	0.1A	±2%	10mVpp	ISL73007SEH
6	1.2V	VGTY_AVTT	2.8A	±2%	10mVpp	ISL73007SEH
7	1.2V/0.6V	DDR_VDDQ, DDR_VTT	3A/1A	±5%		ISL73005SEH
7	2.5V	DDR_VPP	1A	±5%		ISL73007SEH

1.2 Renesas Power Management Solution

The most prominent power supply rail for the AMD Xilinx Versal ACAP is the VCC_INT core rail which consumes up to 100A while delivering 0.8V. This is provided by the Renesas Radiation Hardened Point of Load Regulator that consist of: (2) ISL73847SEH PWM Controllers, (4) ISL73041SEH GaN FET Drivers, and a ISL70020SEH 40V, 65A, 3.5mΩ GaN FET.

Note: On the ISLVERSALDEMO2Z a 4 phase solution is implemented to deliver 100A with a 25A/phase design. However, the design can be revised to provide 35A/phase for 140A total by changing components to handle a larger per phase current. See 0.8V/100A Core Rail Design for changing the design to handle 140A.

The other digital and analog rails for the Versal ACAP are provided by the ISL70001ASEH and ISL73007SEH Integrated FET Synchronous Buck Regulators. The DDR4 memory VDDQ and VTT rails external to the Versal ACAP is powered with the ISL70005SEH Synchronous Buck Regulator + Source/Sink LDO.

The power sequencing, which is critical for the Full Power Management operation of the AMD Xilinx Versal ACAP, is handled by the ISL70321SEH quad sequencer. Table 2 shows the full list of Renesas Radiation Hardened Power Management parts used in the ISLVERSALDEMO2Z.

Table 2. Renesas Radiation Hardened parts used on ISLVERSALDEMO2Z

Device Name	Description	Used For
ISL73847SEH	12V PWM Dual Phase Controller	5V System Rail 0.8V VCC_INT Core Rail
ISL73041SEH	12V GaN Half Bridge Driver	
ISL70020SEH	40V, 65A, 3.5mΩ GaN FET	
ISL70001ASEH	5V, 6A Integrated FET Synchronous Buck	VCC SOC I/O Rail, VCC Aux Rail
ISL70003ASEH	12V, 9A Integrated FET Synchronous Buck	3.3V System Rail
ISL73007SEH	12V, 3A Integrated FET Synchronous Buck	Various Digital and Analog Rails
ISL70005SEH	5V, 3A Synchronous Buck + 1A Source and Sink LDO	DDR4 Memory Supply Rails
ISL70321SEH	Quad Channel Supply Sequencer	Supply Rail Sequencing and Monitoring
ISL70218SEH	Dual 36V Precision Rail to Rail Output Operational Amplifier	Buffer for DDR VREF

1.3 Adjustable Output Voltages

The AMD Xilinx Versal ACAP specifies different operating voltage on certain digital rails; for example at different Versal speed grades certain 0.8V rails must be operated at 0.88V. Also, the VCCO_XPIO and VCCO_50x rails can be set for different digital logic I/O levels required by the user.

The ISLVERSALDEMO2Z includes the necessary jumpers to change the feedback resistors to set the different output voltage.

The VCCO 50x rail can be adjusted for 1.8V, 2.5V or 3.3V. See Table 3.

Table 3. VCCO_50x Adjustments

V_{OUT}	Jumper Status
1.8V	Both Open
2.5V	Jumper JP1051
3.3V	Jumper JP1052

The VCCO XPIO rail can be adjusted for 1.0V, 1.2V, or 1.5V. See Table 4.

Table 4. VCCO_XPIO Adjustments

V_{OUT}	Jumper Status
1.0V	Both Open
1.2V	Jumper JP1101
1.5V	Jumper JP1102

The VCC PSFP, VCC SOC I/O, VCC PMC and VCC PSLP rails can be adjusted for 0.8V or 0.88V. See Table 5.

Table 5. VCC PSFP, VCC SOC I/O, VCC PMC and VCC PSLP Rail Adjustments

VOUT	Jumper Status	VCC PSFP	VCC SOC I/O	VCC PMC	VCC PSLP
0.8V	Jumper Open	JP452	JP1002	JP551	JP351
0.88V	Jumper Short				

1.4 Output Voltage Monitor Test Points and Load Transient Generators

The ISLVERSALDEMO2Z provides test points for monitoring the output voltage and terminals to apply an external load current. Certain output rails also provide an onboard transient load generator for a step load. Table 6 summarizes output rail monitoring, test points, and load transient generator input control for the supply rails.

Table 6. Output Rail Test Points and Transient Load Control Input Connection

ISLVERSALDEMO2Z Node Name	Oscilloscope Test Point (2pin jumper)	DC Test Point/External Load Access (VOUT/GND)	Transient Load Generator Control
ISL73847_5V0_SYS	TP701		
ISL70003A_3V3_SYS	TP501	P501/P502	
ISL73007_VCCO_50x	TP1051	P1051/P1052	
ISL73007_VCCO_XPIO	TP1101	P1101/P1102	JP1104
ISL73007_VCC_PSFP	TP451	P451/P452	JP453
ISL70001A_VCC_SOC/IO	TP1001	P1001/P1002	JP1003
ISL73006_VCC_PMC	TP551	P551/P552	
ISL73006_VCC_PSLP	TP351	P351/P352	
ISL73847_VCCINT	TP1	TERM1/TERM2	TP22
ISL70001A_VCCAUX	TP901	P901/P902	JP902
ISL73006_VCCAUX_SMON/PMC	TP951	P951/P952	
ISL73007_GTY_AVCC	TP251	P251/P252	
ISL73006_GTY_AVCCAUX	TP401	P401/P402	
ISL73007_GTY_AVTT	TP201	P201/P202	JP201
ISL73005_DDR_VDD	TP801	P801/P802	
ISL73005_DDR_VTT	TP802	P803/P804	
ISL73006_DDR_VPP	TP851	P851/P852	

The transient load generator comprises a FET driver controlling a common source NFET that pulls a load resistor to GND to provide a transient load to the supply rail. The ISL73847_VCCINT 0.8V core rail uses an ISL71040MRTZ GaN FET driver, while all other load generators use the HIP2211FBZ half-bridge driver. In both cases, a 0V-5V logic control signal is used to switch the transient load where 0V turns the load off, and 5V turns the load on. Figure 3 through Figure 8 show the input connection to the transient load generator control. The load comprises multiple parallel 2W-rated, 2512-sized resistors. The transient load generator is intended for pulse load operation only where the frequency and duty cycle of the load do not exceed the power dissipation of the resistors.

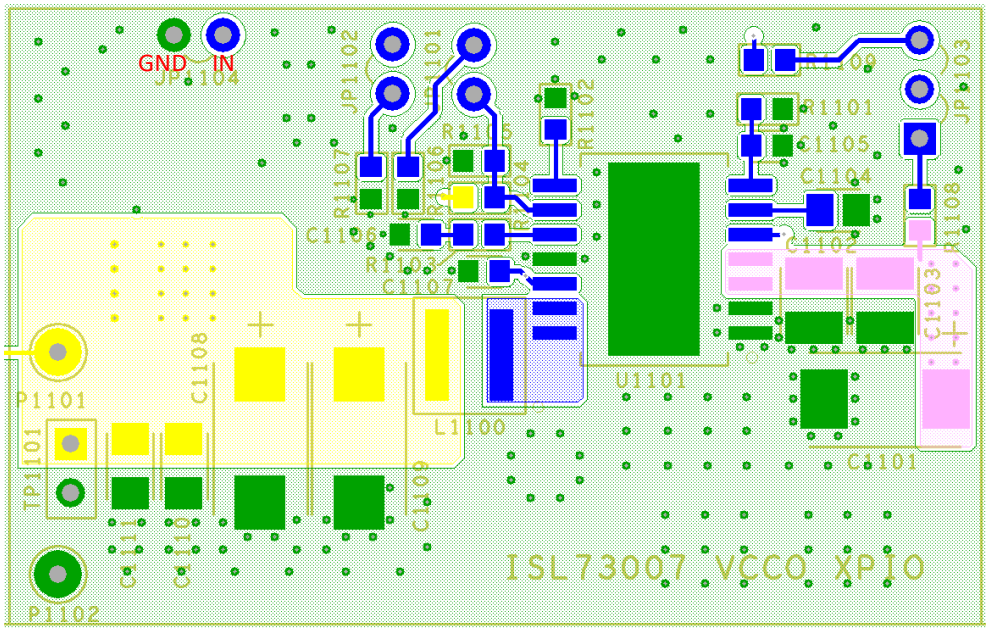

Figure 3. ISL73007_VCCO_XPIO Load Generator Input Orientation

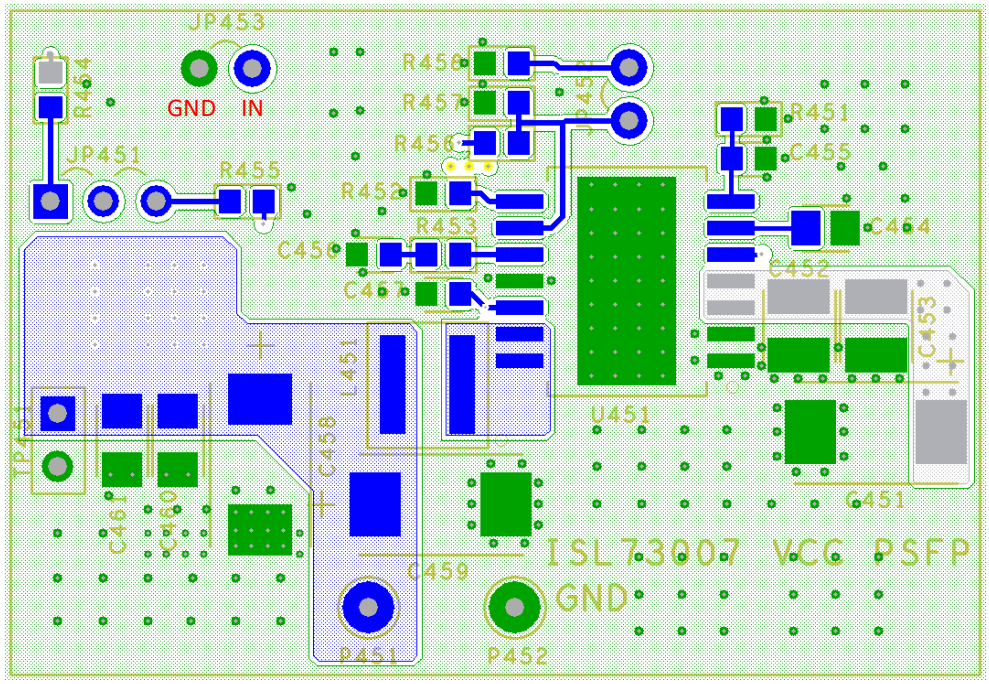

Figure 4. ISL73007_VCC_PSFP Load Generator Input Orientation

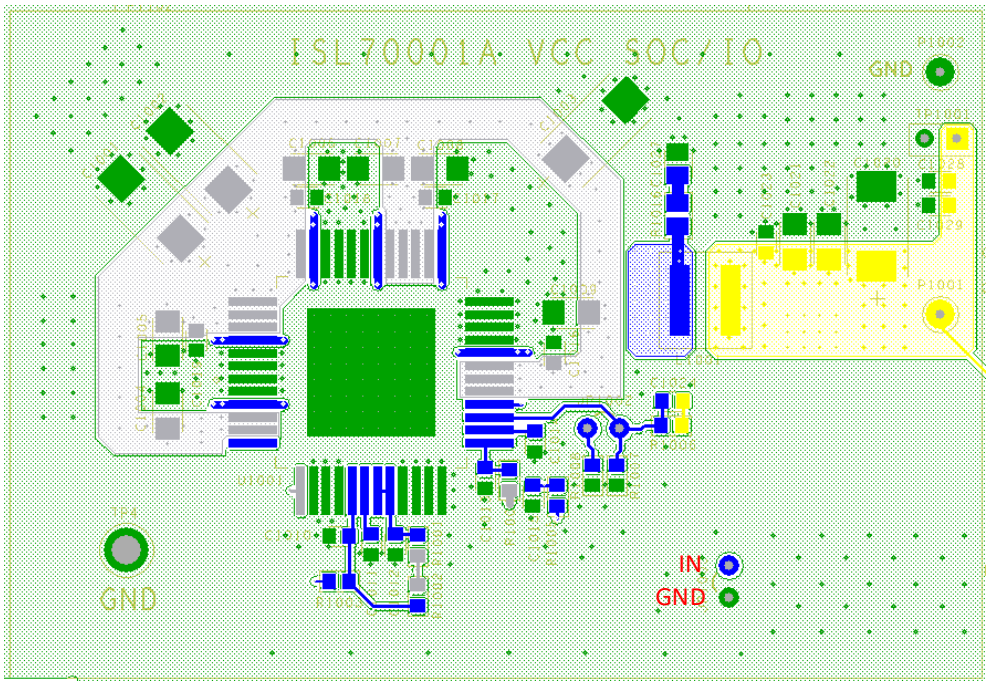

Figure 5. ISL70001A_VCC_SOC_IO Load Generator Input Orientation

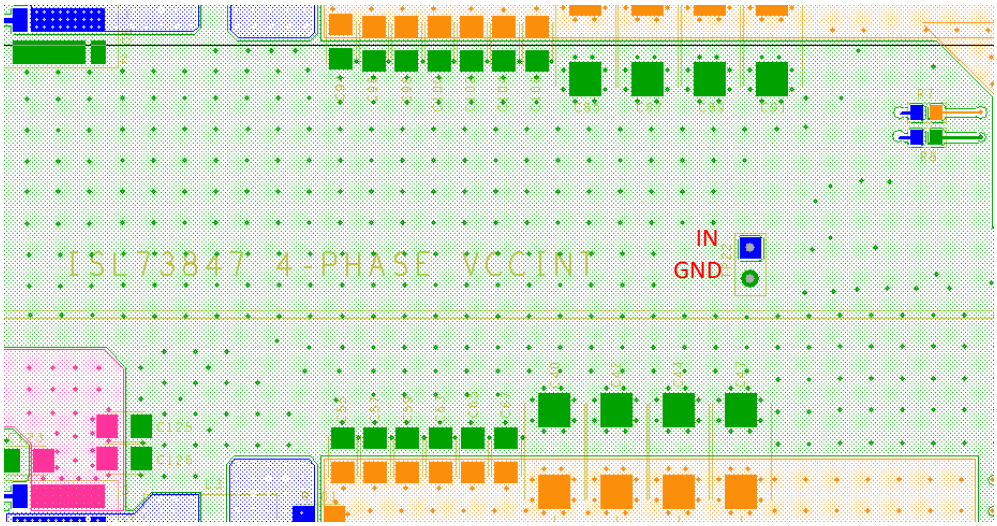

Figure 6. ISL73847_VCC_INT Load Generator Input Orientation

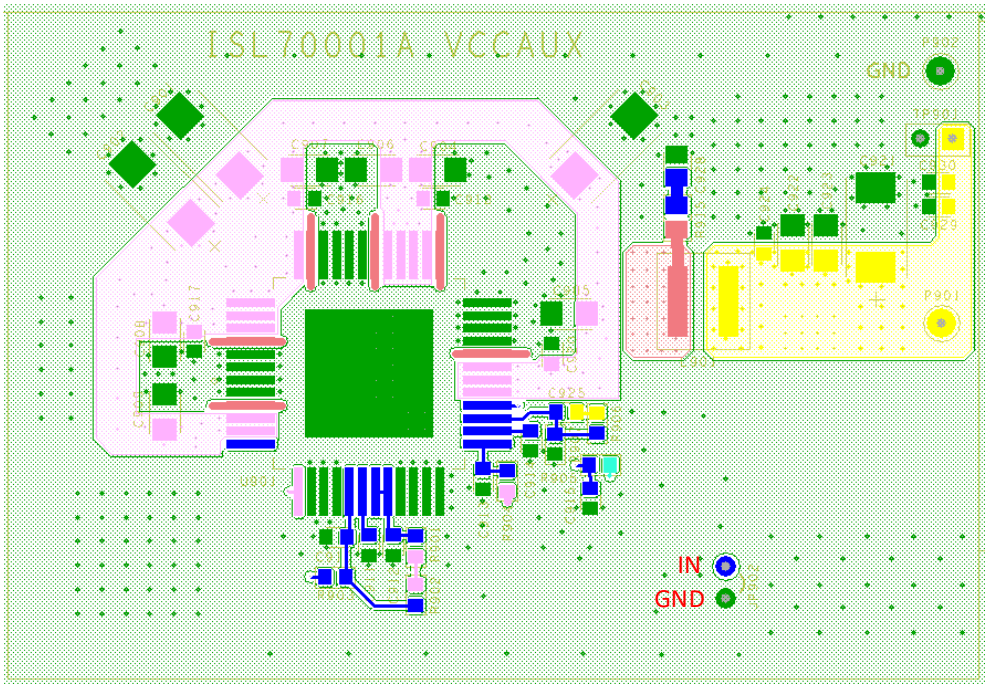

Figure 7. ISL70001A_VCC_AUX Load Generator Input Orientation

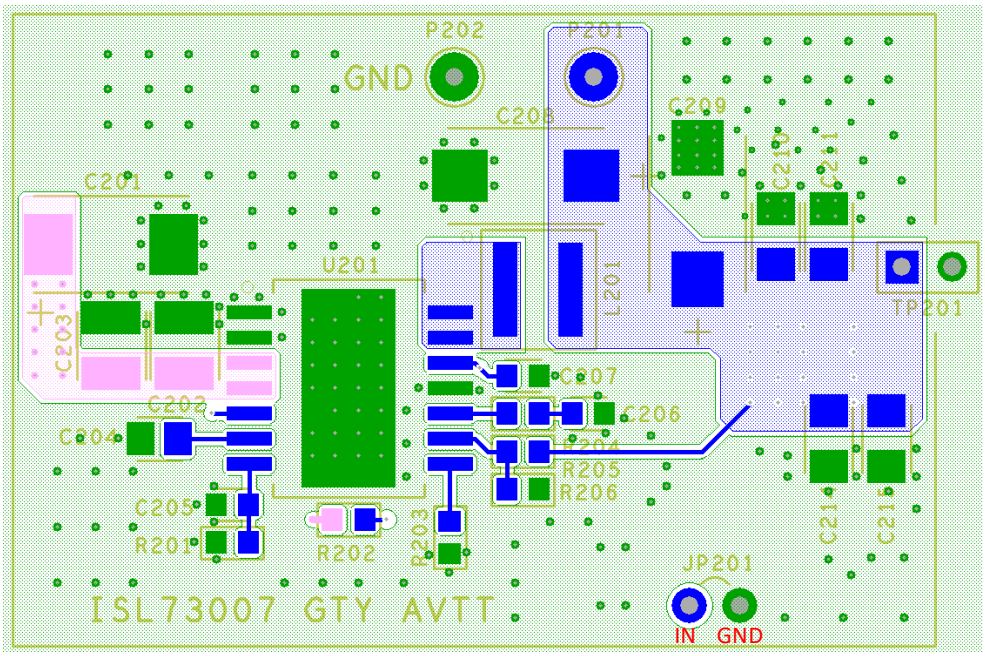

Figure 8. ISL73007_GTY_AVTT Load Generator Input Orientation

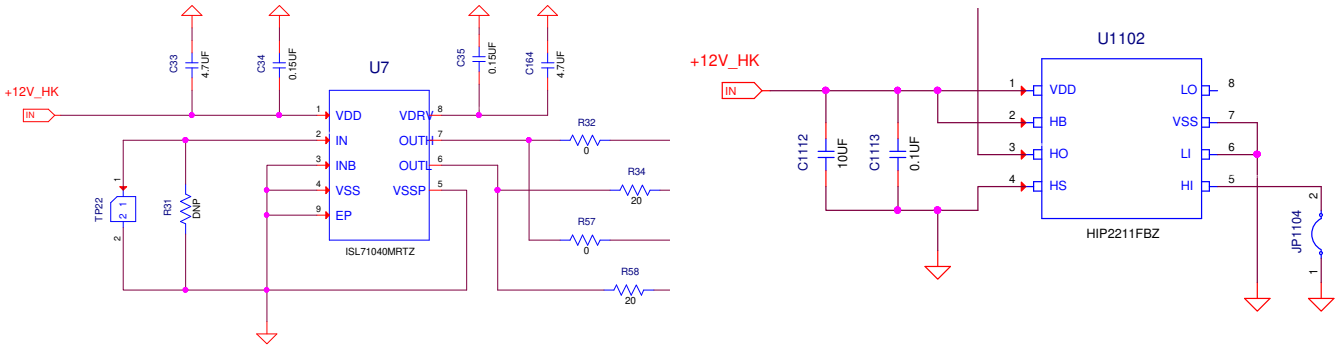

Figure 9. Schematic of Transient Load Generator FET Drivers

1.5 0.8V/100A Core Rail Design

The 0.8V/100A core rail is delivered by the discrete design of (2) ISL73847SEH PWM Controllers, (4) ISL73041SEH GaN FET Drivers, and (12) ISL70020SEH 40V GaN FETs. Each PWM Controller is a dual-phase IC; therefore, the design is a 4-phase solution. Each ISL73847SEH controller operates its two phases at 180 degrees phase shift. Using an external clock with a 50% duty cycle and an inverted and non-inverted input to the SYNC-I pins of the ISL73847SEH provides the 90 degrees phase shift needed for 4-phase operation. Each phase delivers 25A RMS for a total 100A solution.

The external clock solution is implemented with an ISL71041MRTZ Current Mode PWM Controller. Timing is made through the RTCT pin, which provides a square wave clock signal at the OUT pin. The inverted clock output is generated by putting the clock signal into the ISL71040MRTZ GaN FET Driver, which offers an INB input that provides the inverted clock signal at OUTH/OUTL. While the 2MHz clock generated by the ISL71041MRTZ works under a nominal case, it cannot be guaranteed over full operational range. Renesas recommends using a dedicated clock generator instead. The ISL71040MRTZ GaN FET Driver can still be used to generate the inverted clock signal.

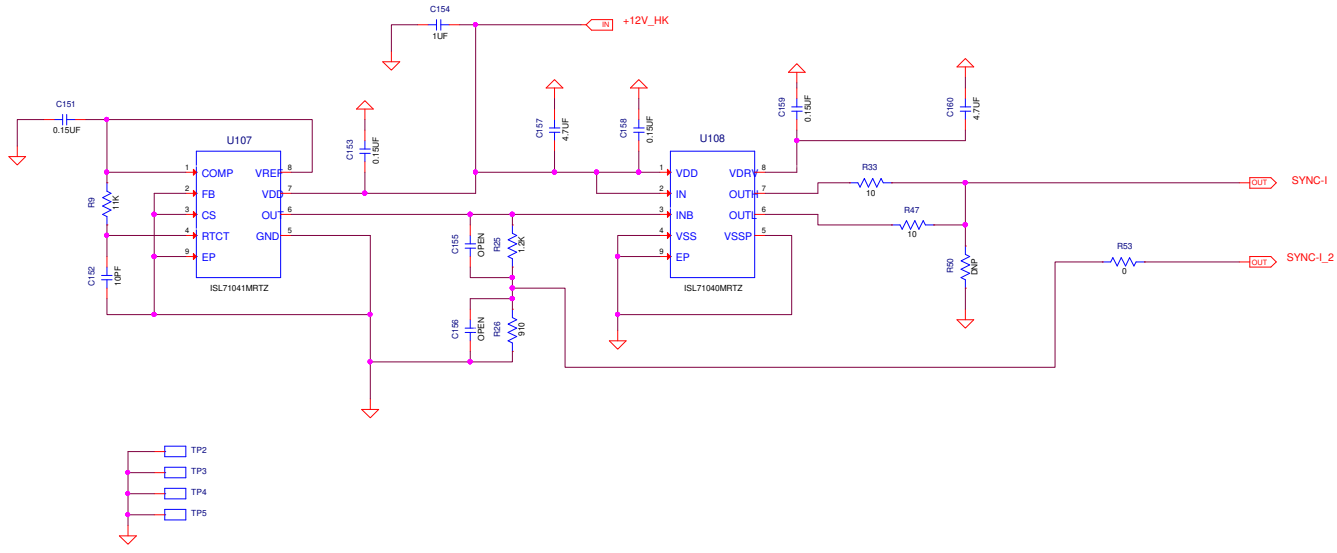

Figure 10. External Synchronized Clock Generator Circuit

If the full 135A specified by the AMD Xilinx Versal ACAP specification is required, modify the design to increase the per-phase current to 35A for a total 140A solution. Make the following changes to the ISLVERSALDEMO2Z board:

Note: The dissipative elements in the power stage (GaN FETs and inductor) see a higher temperature rise due to the increased load current.

1. Operation of 140A on the ISLVERSALDEMO2Z is recommended only for low duty cycle transient durations. If the customer requires to evaluate 140A continuous operation, Renesas recommends using a separate PCB design to accommodate more GaN FETs in parallel and increase the number of PCB layers to handle the extra current.
2. Decrease the Rsense resistor from 2mΩ down to 1.43mΩ so that a 50mV full-scale input to the ISENSE+/ISENSE- pins of the ISL73847SEH is developed with 35A RMS of load current. The Susumu resistors have a 3mΩ available, so two in parallel can be used for 1.5mΩ.
3. Reduce the inductor value. The inductor used is a Coilcraft SLR1070 120nH. There is no smaller inductance in this family. However, the Coilcraft SLC1049 offers a 75nH inductor with adequate saturation and RMS current ratings that can be substituted. The SLC1049 recommended PCB land pattern is slightly different but can be reasonably mounted onto the PCB board.
4. Use the additional DNP placeholders for tantalum capacitors on the 0.8V rail to add the needed capacitance, add 8×220µF.
5. Change the slope compensation, error amp compensation, and droop compensation per the loop design calculator. At minimum, change C_comp from 4.7nF to 3.9nF.
6. Adjust the timing circuit on ISL71041MRTZ U107 from ~1MHz to 875kHz to comply with the maximum inductor value recommended in the loop design calculator. Change C152 from 10pF to 22pF and R9 from 11kΩ to 30.9kΩ.
7. It is not necessary to change the single ISL70020SEH GaN FET on the high side and two ISL70020SEH GaN FET on the low side per phase. The high side operates at ~16% duty cycle, and the increase in per-phase current does not necessitate changing the FETs for evaluating 140A transient load steps.

1.6 Power Sequence and Monitoring

The two ISL70321SEH quad rail sequencers handle the power sequencing and monitor all supply rails. When a sequence up or down is initiated, the supply rails are enabled or disabled in a sequence, shown in Figure 11.

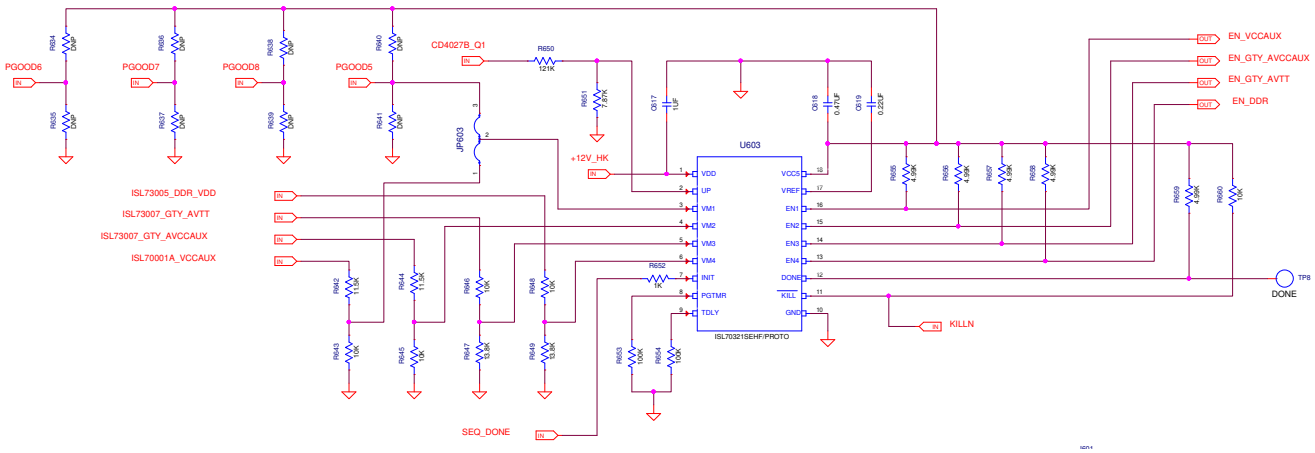

Figure 11. Using Power Sequencer DONE signal for Versal POR_B Control

U603, the second sequencer's DONE pin, signifies the completion of the entire power-up sequence. As described in the AMD Xilinx Power Estimator (XPE) design tool for the Versal ACAP, the POR_B signal for the ACAP must be asserted low during the power-up of the PMC domains. After the PMC domains have powered up, the POR_B signal must be asserted high to complete the Power On Reset (POR). Therefore the DONE signal of the second sequencer can be used for the POR_B of the Versal ACAP. Access to the DONE signal is provided on TP8.

1.7 Power LED Indicators

LED indicators are provided for a visual detection of when certain rails have powered up. The 12V LED is always on when +12V power is applied to the board. All other LEDs are on when the PGOOD signal for that rail pulls high.

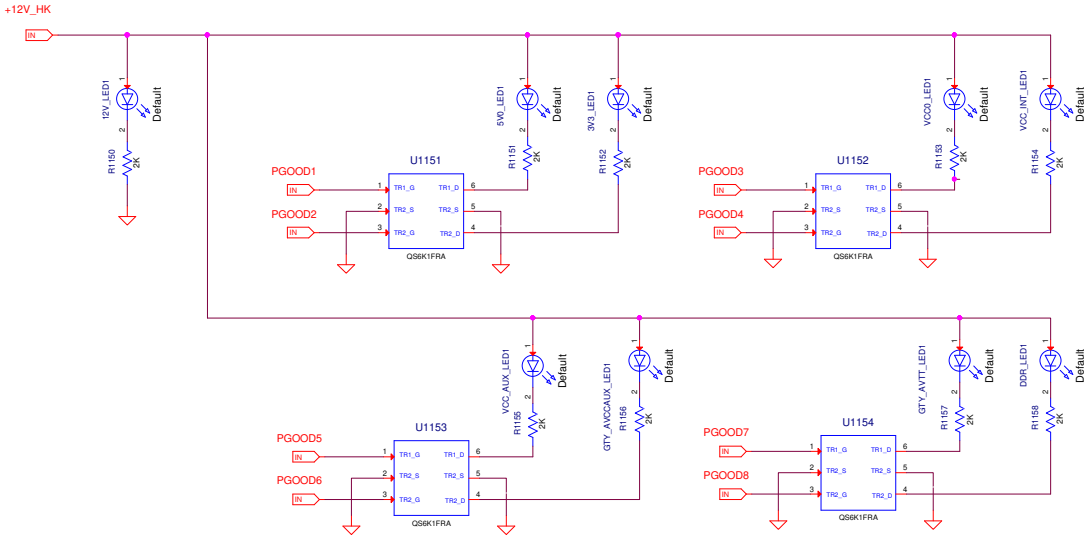

Figure 12. Power LED Indicator

1.8 12V Power Supply and Sequencing Initialization

The +12VDC power supply to the ISLVERSALDEMO2Z is provided by banana jack inputs to the board. Back-to-back PMOS FETs prevent reverse current flow back to the power supply. Mechanical switch SW601 turns power on and off to the board.

Power sequence initialization is provided by push button switch SW602 and the CD4027B JK flip flop. Pushing the button switch provides one pulse, which latches the JK flip flop high and low, alternatively with every push. The main power switch SW601 also controls the RESET pin of the JK flip flop. When the power switch is thrown off, the RESET signal triggers a power-down sequence of the two ISL70321SEH sequencers instead of an uncontrolled shutdown of the power rails. At the same time, a large RC time constant to the gate of Q602 PMOS delays the turn-off of the 12V supply to the board for the power-down sequence to complete.

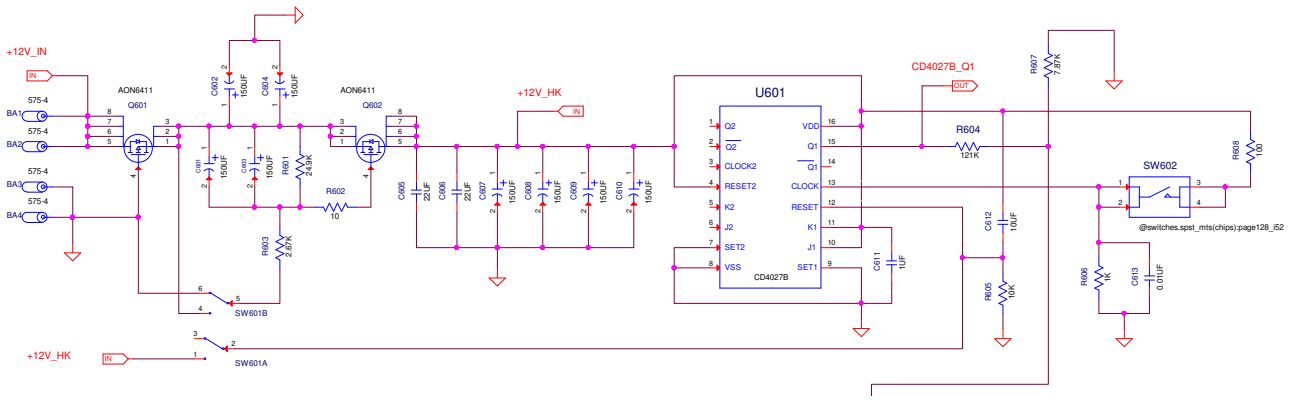

Figure 13. Power Sequence Initialization Circuit

Note: The turn-off latching of the push-button switch occasionally causes a non-sequence simultaneous shutdown of all rails. There is no issue with this other than all rails power down simultaneously.

The VCCO_LED stays on for the longest duration during a power sequence off. This happens because the previous rail being sequenced down that the ISL70321SEH monitors is the ISL73847_VCCINT rail, which has a very large output capacitance to slowly discharge the output voltage. Until the sensed voltage on ISL73847_VCCINT falls below the 600mV internal reference, the sequencer does not power down the next rail, which is driven by the EN_VCCO signal and its PGOOD3 signal is driving the VCCO_LED.

1.9 5V Circuit Breaker Protection

The ISLVERSALDEMO2Z evaluation board includes a circuit breaker to disconnect the 5V rail powering the 0.8V/100A VCC INT core rail. This provides additional protection to the VC1902 under an overcurrent condition. The circuit breaker function is implemented with (5) ISL70061SEH NMOS load switches connected in parallel that is triggered to shut off during an overcurrent, as shown in the Figure 5 application circuit of the ISL70061SEH datasheet.

The ISL70218SRHM 36V Precision Operational Amplifier is configured as a comparator to detect an overcurrent condition. The current monitoring is done on the IMON pin of the ISL73847SEH PWM Controller used for the +12V to +5V DC-DC converter. The reference into the comparator is set by the R301/R302 resistors with 0.316V. The IMON pin outputs a current that represents the summed sensed voltage across the ISENSE+/ISENSE- pins in the two phases of the DC-DC regulator with a transconductance gm of 0.39uA/mV. Given Rsense=2mΩ used in the design and a termination resistor of 10kΩ for IMON, when an RMS current of ~38.6A is detected, the comparator drives the (5) NMOS load switches off to isolate the +5V rail from biasing the power stage of the 5V to 0.8V DC-DC converter that provides bias for the VCC INT rail. As shown in the schematic below, +5V_POST goes to the power stage of the 4-phase 0.8V/100A rail and is isolated from +5V_PRE during an overcurrent condition.

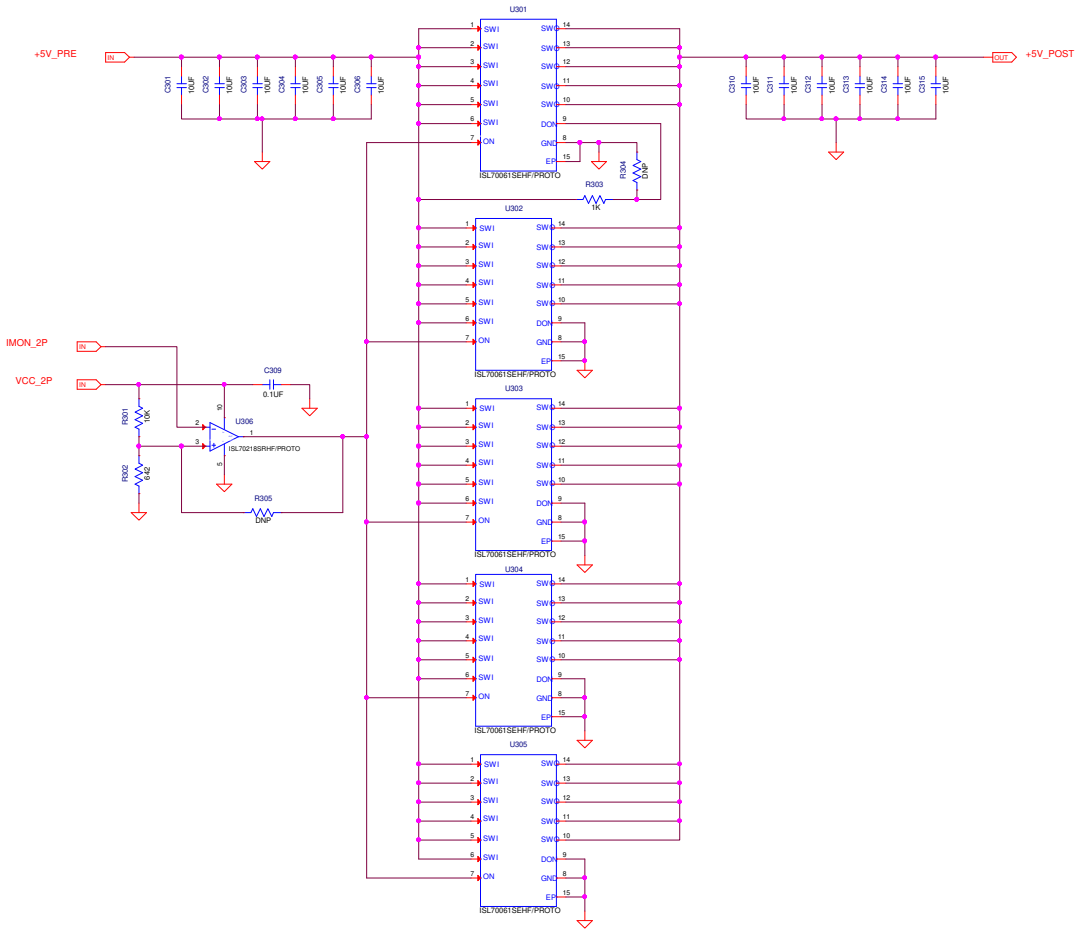

Figure 14. 5V Circuit Breaker

1.10 All Voltage Rail Monitoring

J601 40 Pin header provides a convenient access point to monitor all the DC rails generated by the Renesas Radiation Hardened Point of Load Regulators. Figure 15 shows the pinout of the voltage rails.

Note: Only use J601 for DC voltage monitoring. Attempting to measure the rail voltages for steady state ripple or transient load step for meeting AMD Xilinx Versal power management rail requirements is not recommended because J601 is routed a long distance away from the output capacitors for those rails and will not provide accurate voltages at this measurement point.

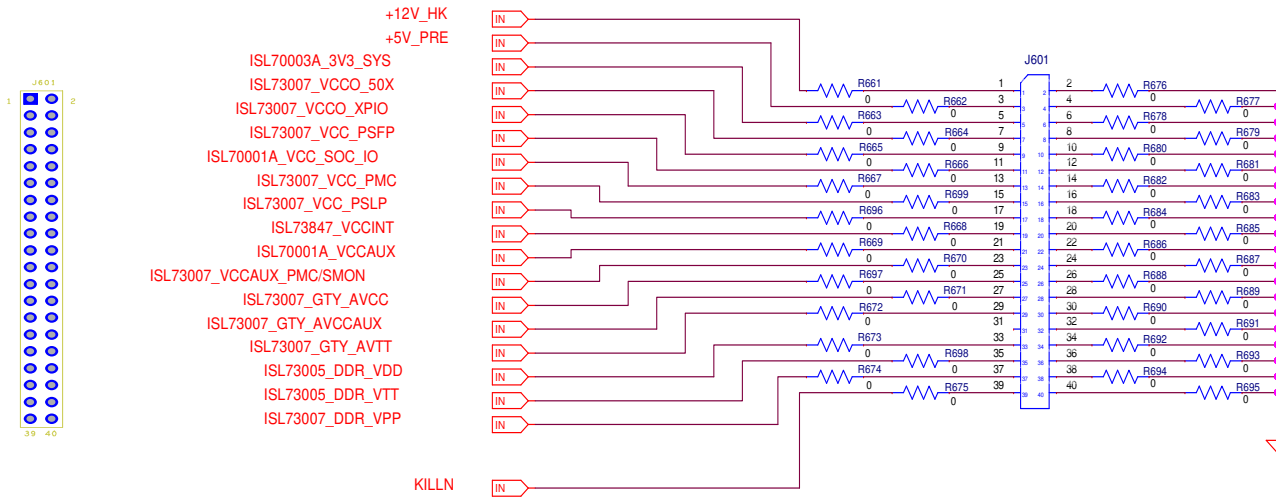

Figure 15. Voltage Rail Pinout

2. Board Design

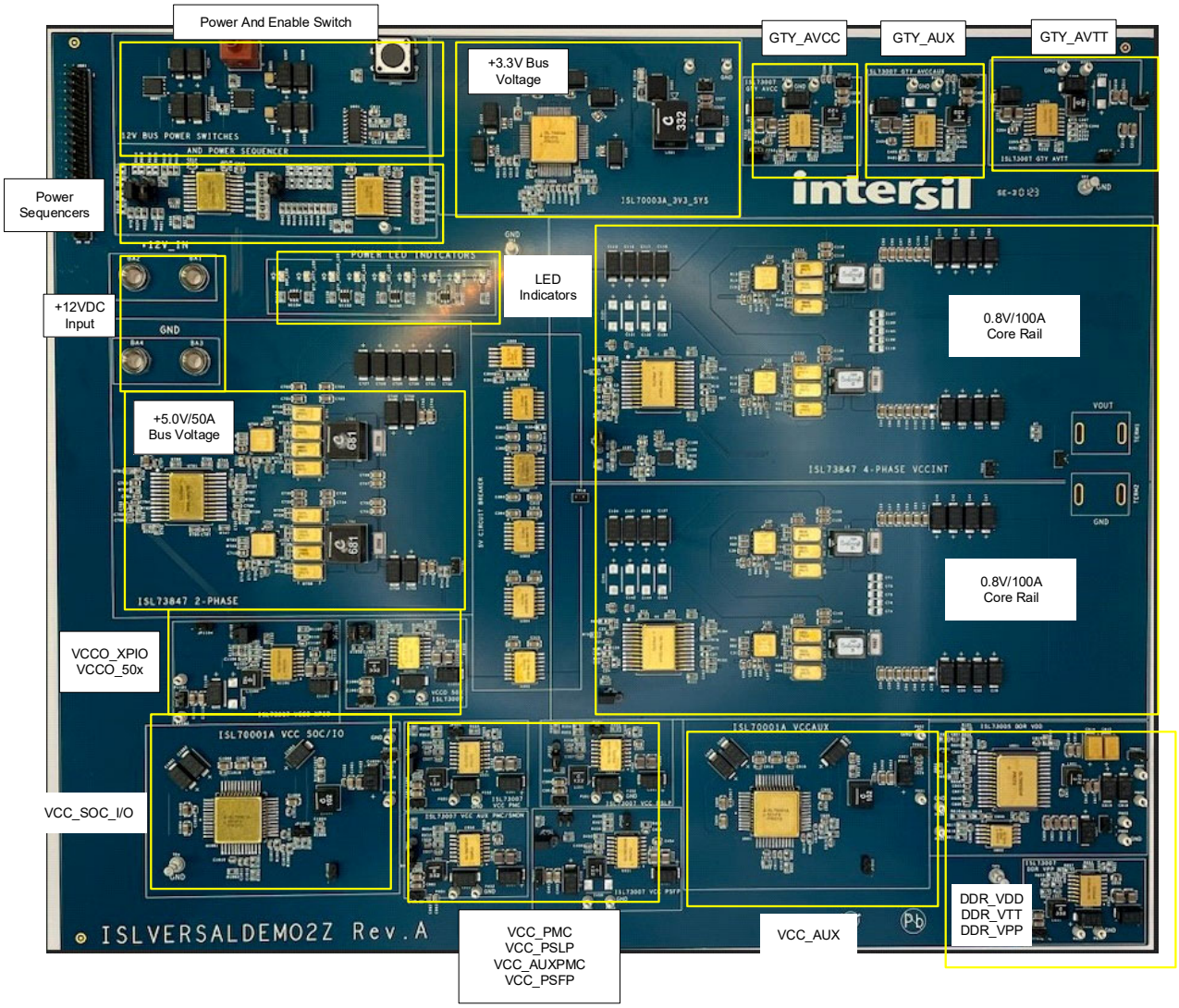

Figure 16. ISLVERSALDEMO2Z Evaluation Board

2.1 Layout Guidelines

The general layout of the ISLVERSALDEMO2Z board is shown below. In the middle right of the board is the 0.8V/100A rail for the Versal ACAP core rail. The bottom half of the board contains the digital and DDR4 supply rails. The upper right section of the board contains the analog supply rails. Along the upper-middle and left-middle side of the board are the regulators to generate the +5.0V and +3.3V systems rails, along with the power sequencers and LED indicators for each supply rail.

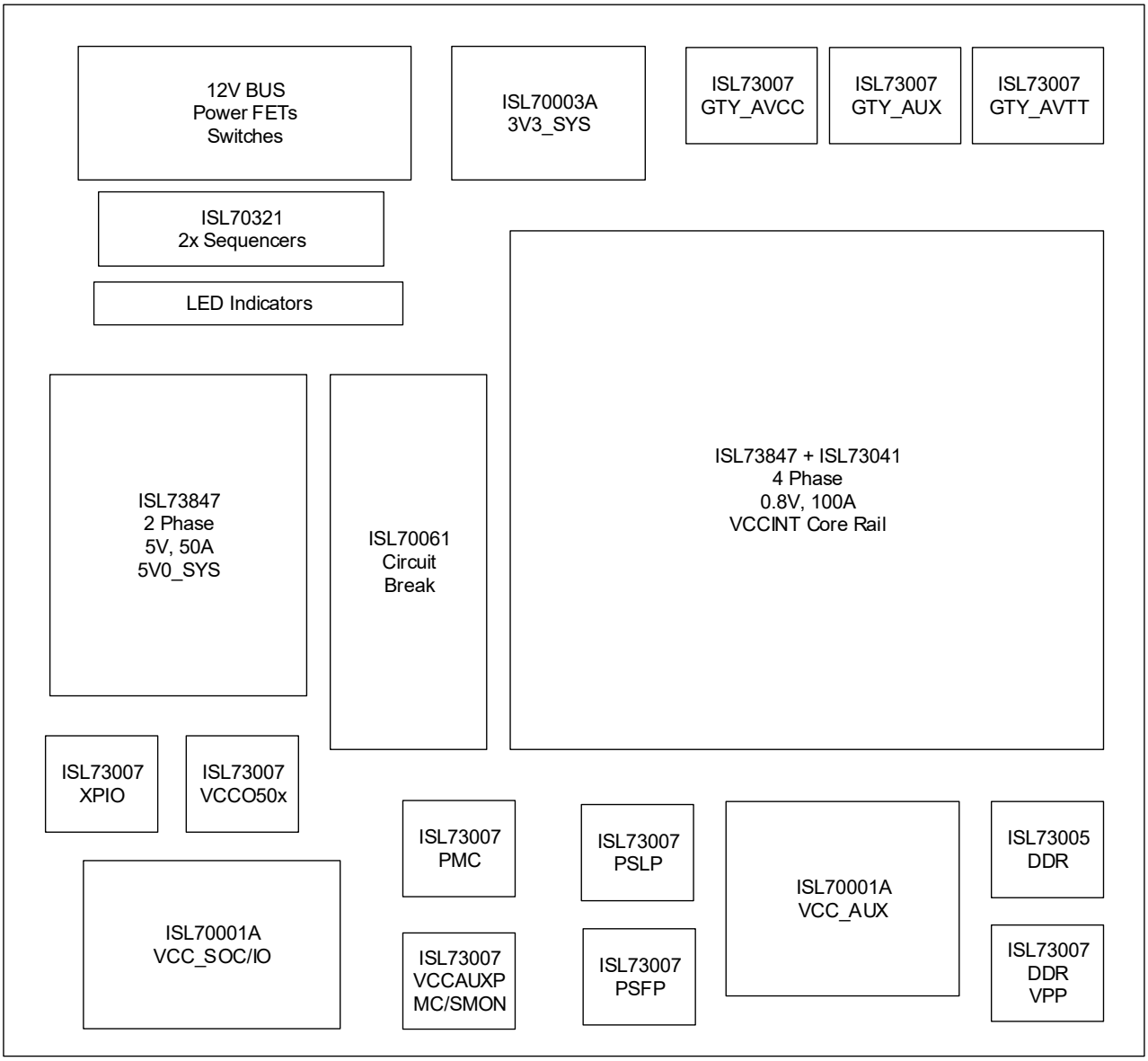

Figure 17. ISLVERSALDEMO2Z Board Layout

For the ISLVERSALDEMO2Z schematic diagram, bill of materials, and board layout files, download the design files from the website.

3. Typical Performance Graphs

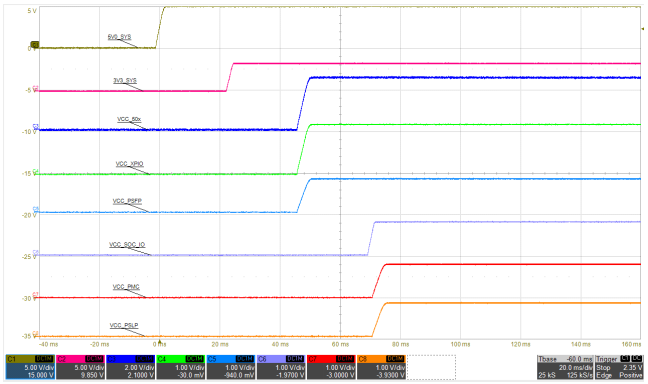

Figure 18. Power-Up Sequencing, Ch1-8

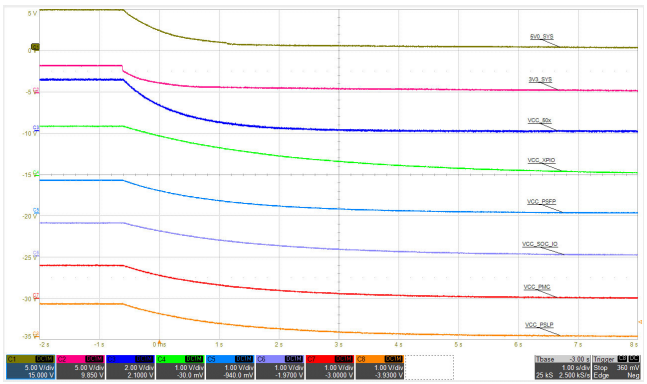

Figure 19. Power-Down Sequencing, Ch1-8

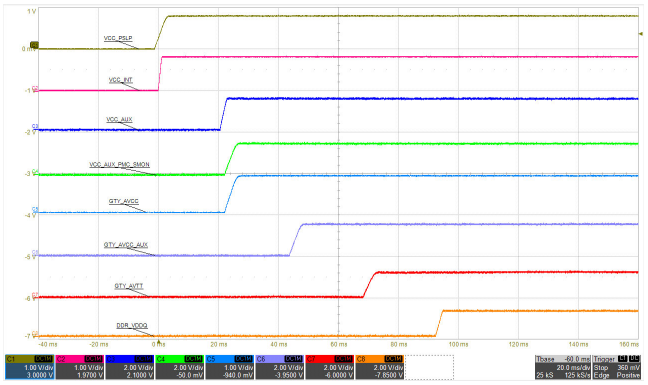

Figure 20. Power-Up Sequencing, Ch9-16

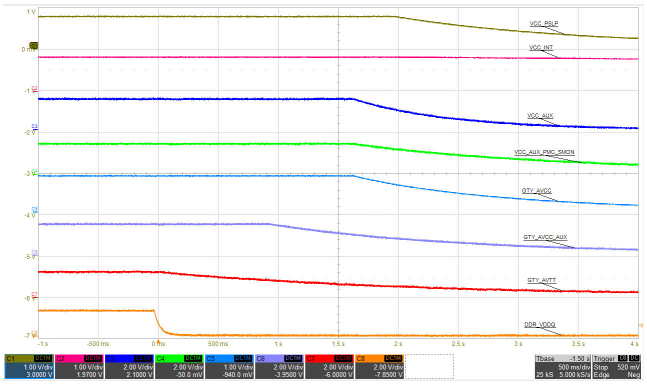

Figure 21. Power-Down Sequencing, Ch9-16

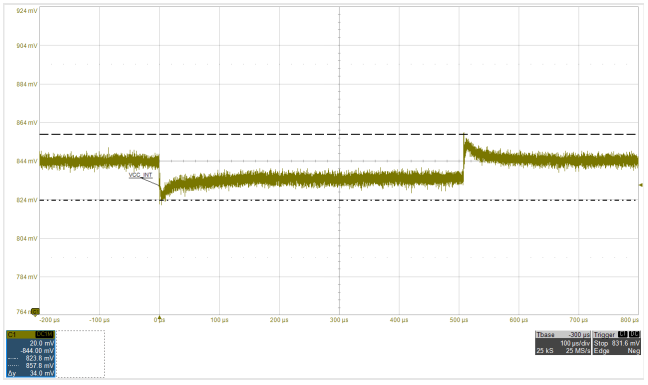

Figure 22. ISL73847_VCCINT Rail 46A Load Step Transient with ±17mV Compliance Window

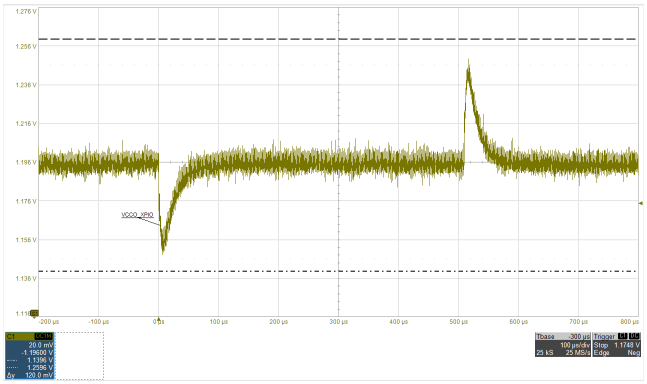

Figure 23. ISL73007_VCCO_XPIO Rail 3A load step with ±60mV Compliance Window

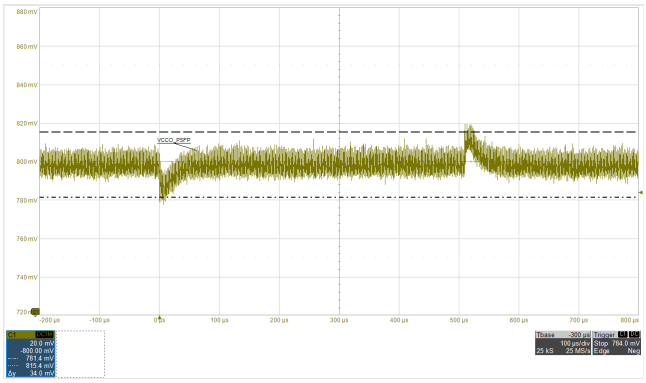

Figure 24. ISL73007_VCC_PSFP Rail 1.33A load step with ±17mV Compliance Window

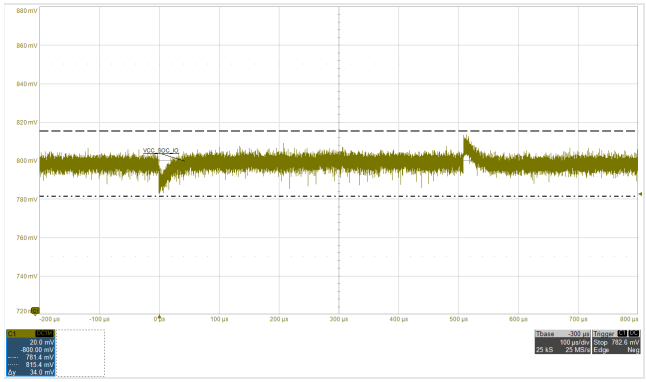

Figure 25. ISL70001A_VCC_SOC_IO Rail 1.6A load step with ±17mV Compliance Window Shown

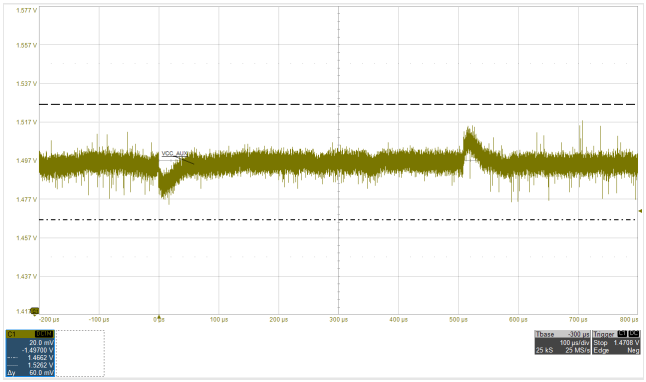

Figure 26. ISL70001A_VCC_AUX Rail 1.5A load step with ±30mV Compliance Window Shown

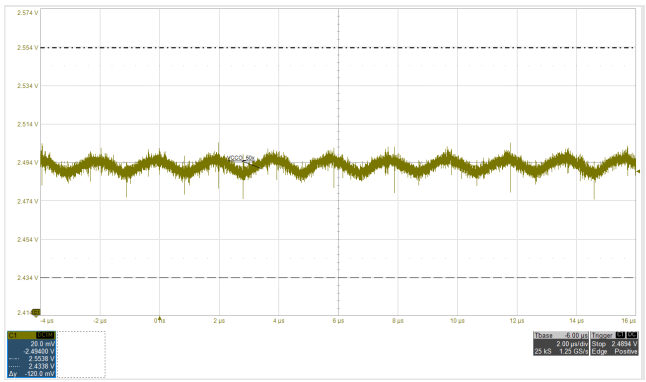

Figure 27. ISL73007_VCCO_50x Rail Steady State Ripple at 3A with ±60mV Compliance Window Shown

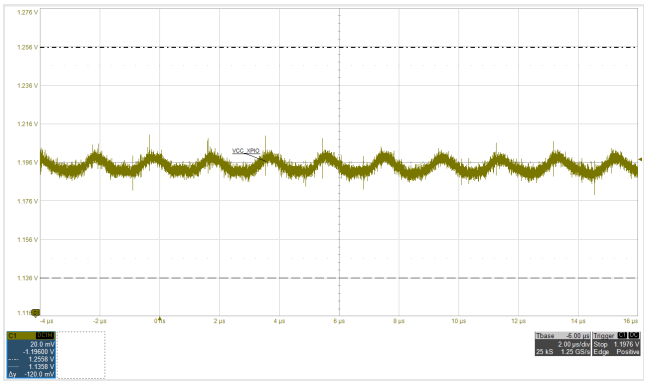

Figure 28. ISL73007_VCCO_XPIO Rail Steady State Ripple at 3A with ±60mV Compliance Window Shown

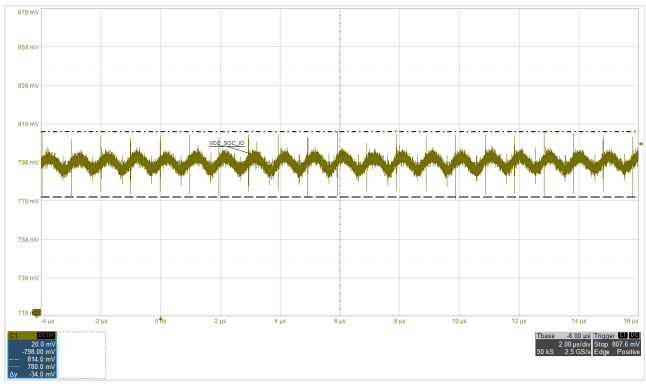

Figure 29. ISL70001A_VCC_SOC_IO Rail Steady State Ripple at 3.5A with ±17mV Compliance Window Shown

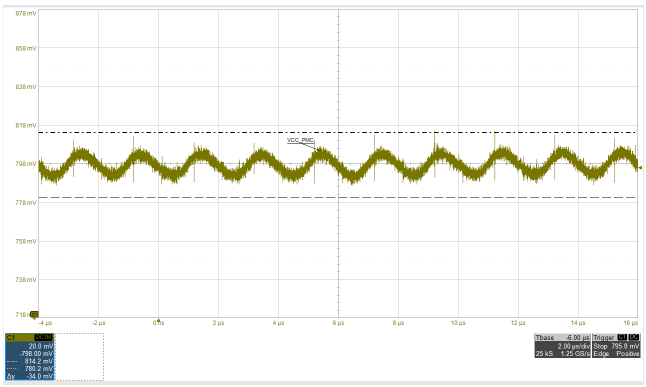

Figure 30. ISL73007_VCC_PMC Rail Steady State Ripple at 0.5A with ±17mV Compliance Window Shown

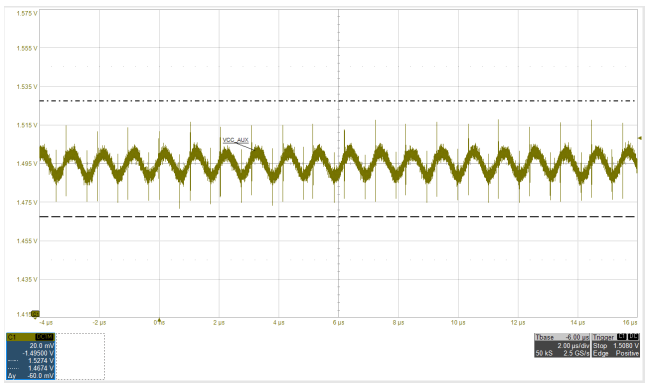

Figure 31. ISL70001A_VCC_AUX Rail Steady State Ripple at 4.2A with ±30mV Compliance Window Shown

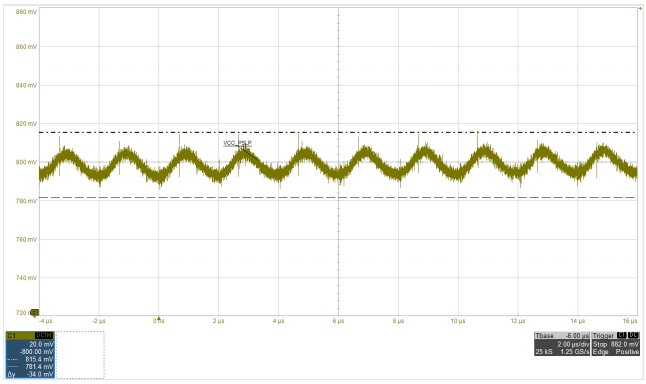

Figure 32. ISL73007_VCC_PSLP Rail Steady State Ripple at 0.5A with ±17mV Compliance Window Shown

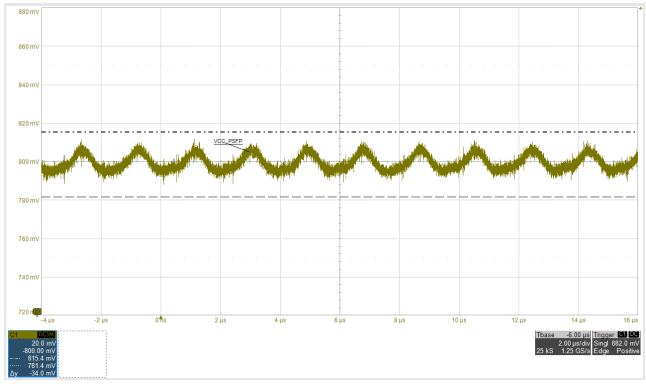

Figure 33. ISL73007_VCC_PSFP Rail Steady State Ripple at 1.5A with ±-17mV Compliance Window Shown

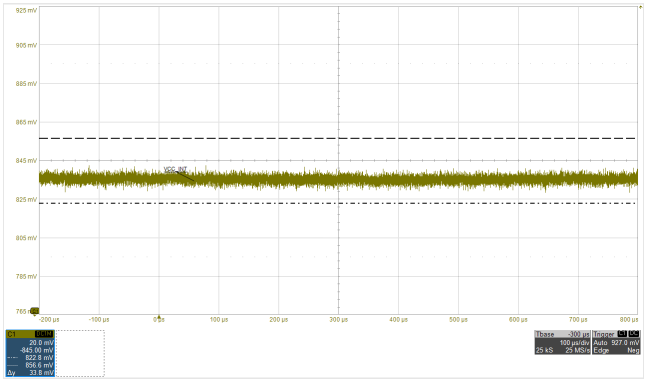

Figure 34. ISL73847_VCCINT Rail Steady State Ripple at 50A with ±17mV Compliance Window Shown

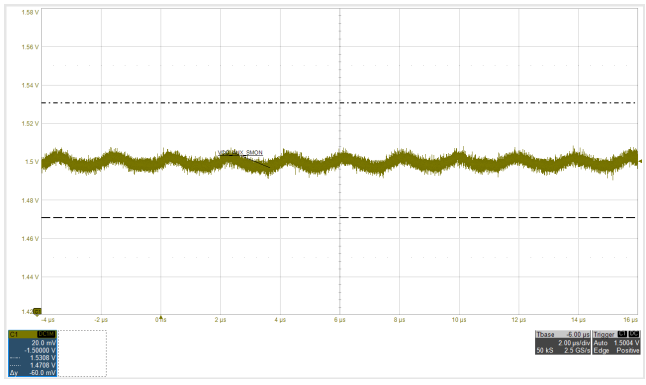

Figure 35. ISL73007_VCC_AUX_SMON_PMC Rail Steady State Ripple at 0.5A with ±30mV Compliance Window Shown

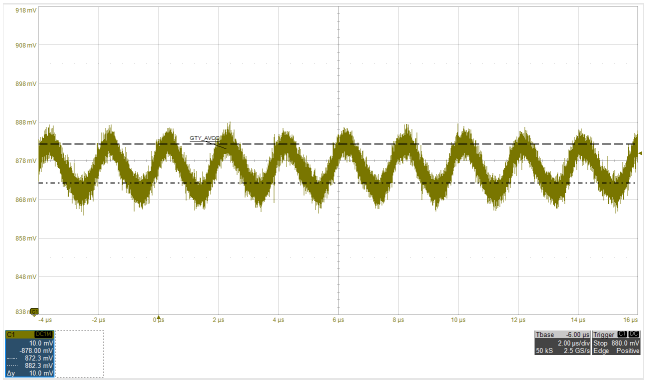

Figure 36. ISL73007_GTY_AVCC Rail Steady State Ripple at 1.7A with 10mVpp Compliance Window Shown

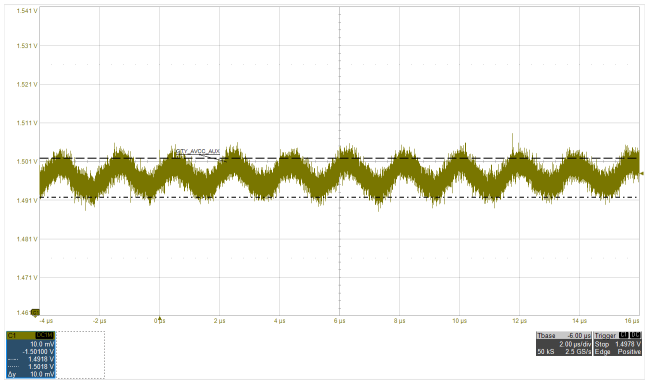

Figure 37. ISL73007_GTY_AVCC_AUX Rail Steady State Ripple at 0.5A with 10mVpp Compliance Window Shown

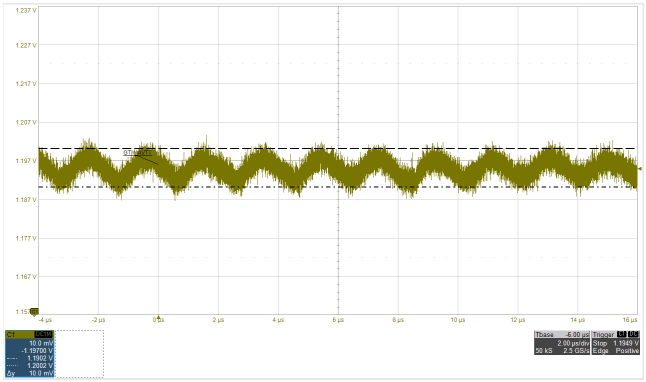

Figure 38. ISL73007_GTY_AVTT Rail Steady State Ripple at 2.8A with 10mVpp Compliance Window Shown

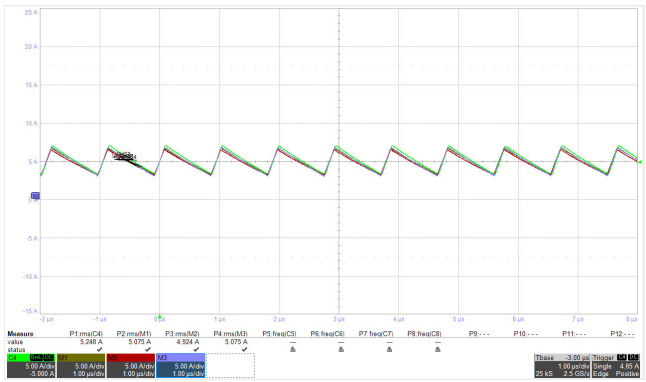

Figure 39. Current Sharing Accuracy of 4-Phase ISL73847_VCCINT Rail at 20A Load

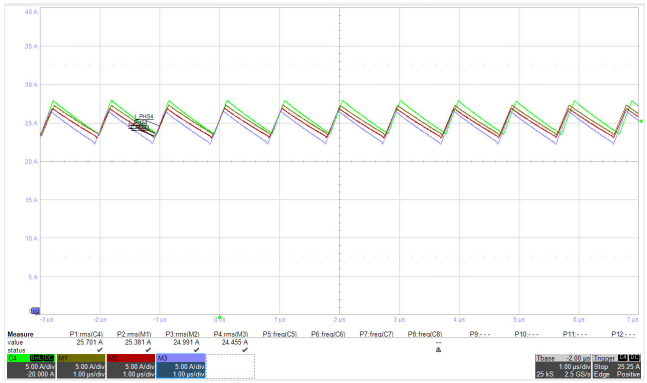

Figure 40. Current Sharing Accuracy of 4-Phase ISL73847_VCCINT Rail at 100A Load

4. Ordering Information

Part Number	Description
ISLVERSALDEMO2Z	Power Management Demonstration Board

5. Revision History

Revision	Date	Description
1.00	Jun 13, 2023	Initial release

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